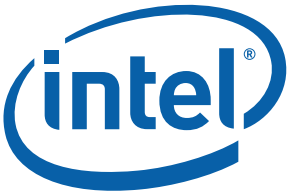

Intel® I/O Controller Hub 10 (Intel® ICH 10) Family

Specification Update

September 2013

Document Number: 319974-017US

Contents

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Revision History

Revision	Description	Date
-017	Added Items: - Specification Change: 2 - The Intel® ICH 10 product wire bond material is changing from Gold (Au) to Copper Palladium (Cu-Pd). - Identification information (Marking) due to new SSPEC update	September 2013
-016	Added Item: - Errata: 19- Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled - Specification Change: 1- ROAEI options removal for OCW2	May 2012
-015	Added Items: - Document Changes: 20- Correct OUTSTRMPAY Register information - Document Changes: 21 - Correct INSTRMPAY Register information	December 2011
-014	Added Items: - Errata: 18 Intel® ICH10 SATA GEN3 Device Detection - Errata: 16 Intel® I/O Controller Hub 10 (ICH10) Family HPET Write Timing	February 2011
-013	Added Items: - Document Changes: 19-Update Section 8.2 in the Datasheet - Errata: 18 Intel® ICH10 SATA GEN3 Device Detection	December 2010
-012	Added Items: - Errata: 17 Intel® ICH10 Corporate May Not Detect Unsolicited SATA COMINITs - Document Changes: 18 - Correct A20M# Signal Description	November 2010
-011	Added Items: - Document Changes: 17-Correct Section 13.1.23 Bits 15:2 definition	May 2010
-010	Added Items: - Errata: 16 Intel® I/O Controller Hub 10 (ICH10) Family HPET Write Timing - Document Changes: 16- Correct Section 10.1.45 Bit 0 definition	February 2010
-009	Added Items: - Errata 15 Intel® I/O Controller Hub 10 (ICH10) Family SATA SYNC Escape	December 2009
-008	Added Items: - Errata: 14- Intel® I/O Controller Hub 10 (ICH10) Family PCI Express Function Disable -Document Changes: 15- Correct Section 5.13.6.5 Sx-G3-Sx, Handling Power Failures regarding wake events following a power failure	August 2009
-007	Added Items: - Errata: 13- Intel® I/O Controller Hub 10 (ICH10) Family SATA Low Power Device Detection -Document Changes: 13 -Correct SMBCLK_CTL bit default value 14 - Correct Table 2-24 Strap selection for Boot BIOS Destination	July 2009
-006	Added Items: Corrected Device ID for D30:F0 in Table 2-27 ICH10 Consumer Device and Rev ID Table Document Changes: 9- Remove GPIO58 from Figure 2-1 Intel® ICH10 Interface Signals Block Diagram. 10- Add 1.1v for VccDMI in Table 2-24. 11-Correct Bit Types for PCI Express UnCorrectable Error Severity register (UEV) Corporate ICH10. 12- Correct PCI Express DSTS register definition for bit 1 (NFED)	April 2009
-005	Added Items: Document Change: 8- Add foot note for all references to SPI Flash descriptors ICHSTRP0 and MCHSTRP0	February 2009
-004	Added Items: Document Changes: 6- Make correction to Table 5-40 Causes of Host and Global Resets 7- Update bit definition for SECOND_TO_STS	January 2009

Revision	Description	Date
-003	Added Items: Document Changes: 1-Add GPIO Reset Notes, 2- Correct EOIFD bit definition, 3- Correct GPI_INV -GPIO Signal Invert register definition 4- Update TBD defaults. 5 Update GPIO Note #4 in Section 3.2 Output and I/O Signals Planes and States	December 2008
-002	Added Intel ICH10 Corporate components - Intel 82801JD ICH10 Corporate Base (ICH10D) - Intel 82801JDO ICH10 Digital Office (ICH10DO) Added Errata 7-12.	September 2008
-001	Initial Release.	June 2008

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel ® I/O Controller Hub 10 (ICH10) Family Datasheet	319973

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of Intel® ICH 10 to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® ICH 10 product family. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping		Status	ERRATA
	A0 Consumer	B0 Corporate		
1	X		No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family UHCI Hang with USB Reset
2	X		No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family THRM Polarity on SMBus
3	X		No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family High Speed (HS) USB 2.0 D+ and D- Maximum Driven Signal Level
4	X		No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family PET Alerts on SMBus
5	X		No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family SMBus Host Controller May Hang
6	X		No Fix (Consumer) Fixed (Corporate)	Intel® I/O Controller Hub 10 (Intel® ICH 10) Family LAN_PHY_PWR_CTRL Functionality
7	X		No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Family High-speed USB 2.0 VHSOH
8	X		No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Family 1.5 Gb/s SATA Signal Voltage Level
9		X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family System Reset with Intel® Anti-Theft Technology
10		X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family LAN_RST# Assertion on Sx/MOff Entry
11		X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family Power Button Override
12		X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family ME SMBus/SMLink Clock Frequency
13	X	X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Family SATA Low Power Device Detection
14	X	X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Family PCI Express Function Disable
15	X	X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Family SATA SYNC Escape
16	X	X	No Fix	Intel® I/O Controller Hub 10 (Intel® ICH 10) Family HPET Write Timing
17		X	No Fix	Intel® ICH 10 Corporate May Not Detect Unsolicited SATA COMINITs
18	X	X	No Fix	Intel® ICH 10 SATA 6.0 Gbps Device Detection
19	X	X	No Fix	Incorrect IRQ(x) Vect3or Returned for 8259 Interrupts With RAEOI Enabled

Specification Changes

Spec Change Number	SPECIFICATION CHANGES
1	"ROAEI options removal for OCW2 "
2	"The Intel® ICH 10 product wire bond material is changing from Gold (Au) to Copper Palladium (Cu-Pd)."

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in the revision of the Specification Update

Documentation Changes

No.	DOCUMENTATION CHANGES
1	Add GPIO Signal Reset Notes
2	Corrected EOIFD Bit Definition
3	Correct GPI_INV - GPIO Signal Invert Register Definition
4	Update TBD defaults
5	Update GPIO Note #4 in Section 3.2, Output and I/O Signals and States
6	Make Correction to Table 5-40
7	Update bit definition for Second_TO_STS
8	Add Foot Notes For All References to SPI Flash Descriptors ICHSTRP0 and MCHSTRP0
9	Remove GPIO58 from Figure 2-1, Intel® ICH 10 Interface Signals Block Diagram
10	Add 1.1v for VccDMI in Table 2-24
11	Correct Bit Types for PCI Express* UnCorrectable Error Severity register (UEV) Corporate Intel® ICH 10
12	Correct PCI Express* DSTS register definition for bit 1 (NFED)
13	Correct SMBCLK_CTL bit default value
14	Correct Table 2-24, Strap selection for Boot BIOS Destination
15	Correct Section 5.13.6.5, Sx-G3-Sx, Handling Power Failures, regarding possible wake events following a power failure
16	Correct Section 10.1.45, Bit 0 definition
17	Correct Section 13.1.23, Bits 15:2 definition
18	Correct A20M# Signal Description
19	Update Section 8.2 in the Datasheet
20	Correct OUTSTRMPAY Register information
21	Correct INSTRMPAY Register information

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Identification Information

Markings

Intel® ICH 10 Stepping	S-Spec	Top Marking	Notes
Consumer			
A0	SLB8R	AF82801JIB	82801JIB ICH10 (Base)
A0	SLB8S	AF82801JIR	82801JIR ICH10R
Corporate			
B0	SLG8T	AF82801JD	82801JD ICH10D
B0	SLG8U	AF82801JDO	82801JDO ICH10DO
B0	SLJZA	AF82801JDO	D82801JDO ICH10DO

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Intel® ICH 10 Device and Revision Identification

Intel® ICH 10 Corporate Device and Revision ID Table

Device Function	Description	Intel® ICH 10 Dev ID	Intel® ICH 10 B0 Rev ID	Comments
D31:F0	LPC	3A14h	02h	ICH10DO
		3A1Ah	02h	ICH10D
D31:F21	SATA	3A00h	02h	Non-AHCI and Non-RAID Mode (Ports 0,1, 2 and 3)
		3A02h	02h	AHCI Mode (Ports 0-5)
		3A05h[3]	02h	RAID 0/1/5/10 Mode
D31:F51	SATA	3A06h	02h	Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	3A60h	02h	
D31:F6	Thermal	3A62h	02h	
D30:F0	DMI to PCI Bridge	244Eh	A2h	
D29:F0	USB UHCI #1	3A64h	02h	
D29:F1	USB UHCI #2	3A65h	02h	
D29:F2	USB UHCI #3	3A66h	02h	
D29:F3	USB UHCI #6	3A69h	02h	Note: Device and Revision ID is always the same as D26:F2.
D29:F7	USB EHCI #1	3A6Ah	02h	
D26:F0	USB UHCI #4	3A67h	02h	
D26:F1	USB UHCI #5	3A68h	02h	
D26:F2	USB UHCI #6	3A69h	02h	
D26:F7	USB EHCI #2	3A6Ch	02h	
D27:F0	Intel® High Definition Audio	3A6Eh	02h	
D28:F0	PCI Express* Port 1	3A70h	02h	
D28:F1	PCI Express Port 2	3A72h	02h	
D28:F2	PCI Express Port 3	3A74h	02h	
D28:F3	PCI Express Port 4	3A76h	02h	
D28:F4	PCI Express Port 5	3A78h	02h	
D28:F5	PCI Express Port 6	3A7Ah	02h	
D25:F0	LAN	3A7Ch[2]	02h	
D23:F0	VECI	3A51h	02h	ICH10DO Only
D22:F01	SATA	3A55h	02h	Virtualized SATA controller for use by Intel® Anti-Theft Technology

Notes:

1. ICH10 contains multiple SATA devices. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 3A7Ch is used. Refer to the 82567 GbE Physical Layer Transceiver (PHY) Datasheet for LAN Device IDs.
3. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch

Intel® ICH 10 Consumer Device and Revision ID Table

Device Function	Description	Intel® ICH 10 Dev ID	Intel® ICH 10 A0 Rev ID	Comments
D31:F0	LPC	3A16h	00h	ICH10R
		3A18h	00h	ICH10 (Consumer Base)
D31:F21	SATA	3A20h	00h	Non-AHCI and Non-RAID Mode (Ports 0,1, 2 and 3)
		3A22h	00h	AHCI Mode (Ports 0-5)
		3A25h3	00h	RAID 0/1/5/10 mode
D31:F51	SATA	3A26h	00h	Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	3A30h	00h	
D31:F6	Thermal	3A32h	00h	
D30:F0	DMI to PCI Bridge	244Eh	90h	
D29:F0	USB UHCI #1	3A34h	00h	
D29:F1	USB UHCI #2	3A35h	00h	
D29:F2	USB UHCI #3	3A36h	00h	
D29:F3	USB UHCI #6	3A39h	00h	Note: Device and Revision ID is always the same as D26:F2.
D29:F7	USB EHCI #1	3A3Ah	00h	
D26:F0	USB UHCI #4	3A37h	00h	
D26:F1	USB UHCI #5	3A38h	00h	
D26:F2	USB UHCI #6	3A39h	00h	
D26:F7	USB EHCI #2	3A3Ch	00h	
D27:F0	Intel® High Definition Audio	3A3Eh	00h	
D28:F0	PCI Express* Port 1	3A40h	00h	
D28:F1	PCI Express Port 2	3A42h	00h	
D28:F2	PCI Express Port 3	3A44h	00h	
D28:F3	PCI Express Port 4	3A46h	00h	
D28:F4	PCI Express Port 5	3A48h	00h	
D28:F5	PCI Express Port 6	3A4Ah	00h	
D25:F0	LAN	3A4Ch2	00h	

NOTES:

1. Intel® ICH 10 contains two SATA devices. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 3A4Ch is used. Refer to the 82567 GbE Physical Layer Transceiver (PHY) Datasheet for LAN Device IDs.
3. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.

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Errata

1. Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family UHCI Hang with USB Reset

Problem: When SW initiates a Host Controller Reset or a USB Global Reset while concurrent traffic occurs on at least three UHCI controllers, the UHCI controller(s) may hang.

Note: The issue has only been replicated in a synthetic reset test environment.

Implication: System may hang.

Workaround: BIOS workaround available. Contact your Intel field representative for the latest BIOS information.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

2. Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family THRM Polarity on SMBus

Problem: When THRM#_POL (PMBASE+42h:bit0) is set to high, the THRM# pin state as reported to the SMBus TCO unit is logically inverted.

Implication: If the THRM#_POL bit is set to high, an external SMBus master reading the BTI Temperature Event status will not receive the correct state of the THRM# pin. The value will be logically inverted. If THRM#_POL is set to low, value is correct.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

3. Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family High Speed (HS) USB 2.0 D+ and D- Maximum Driven Signal Level

Problem: During Start-of-Packet (SOP)/End-of-Packet (EOP), the ICH10 Consumer may drive D+ and D- lines to a level greater than USB 2.0 spec +/-200mV max.

Implication: May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

Note: Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or Low Speed (LS) and Full Speed (FS) devices

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

4. Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family PET Alerts on SMBus

Problem: When using the ICH Consumer SMBus for Platform Event Trap (PET) alerts on a system with the Intel® Management Engine (ME) enabled, the SMBus packet headers may be corrupted if all of the following conditions are met:

- SMBus slave is the target of an external PET generating master on SMBus/SMLink
- The ME is in the middle of M0-M1 transitions
- SMBus slave receives back-to-back PET alerts of which some PET alerts are incomplete (i.e. the packet is truncated to less than 6 bytes)

Note: This issue has only been observed under a synthetic test environment.

Implication: ME firmware may stop functioning, which could cause a system hang.

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

5. Intel® I/O Controller Hub 10 (Intel® ICH 10) Consumer Family SMBus Host Controller May Hang

Problem: During heavy SMBus traffic utilization, the ICH10 Consumer SMBus host controller may attempt to start a transaction while the bus is busy.

Note: This issue has only been observed under a synthetic test environment.

Implication: May cause the SMBus host controller to hang.

- After boot:
  - — SMBus host controller transaction may not complete.
  - — External master transaction in progress targeting ICH10 Consumer SMBus slave may get NACK or timeout.
  - — There is no impact to any other transaction that was in progress by an external master.
- This issue has not been observed during boot as SMBus utilization tends to be light.

Workaround: BIOS workaround available. Contact your Intel field representative for the latest BIOS information.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

6. Intel® I/O Controller Hub 10 (Intel® ICH 10) Family LAN_PHY_PWR_CTRL Functionality

Problem: LAN_PHY_PWR_CTRL output is driven low by the ICH10 during a host reset with or without power cycle for up to 3 RTC clock cycles due to the pin momentarily being configured as an output GPIO.

- LAN_PHY_PWR_CTRL functionality requires a soft strap setting in the SPI descriptor and use of the integrated LAN controller in ICH10 with the Intel® 82567 PHY.

Implication: Functional failures such as system hangs or link loss with dropped packets have been observed when LAN_PHY_PWR_CTRL is tied to the LAN_DISABLE_N pin on the Intel 82567.

Note: There are no functional implications if the pin is configured as GPIO12.

For ICH10 Consumer based platforms:

- Intel ME-Enabled Platforms: An Intel ME FW workaround will be provided in the PC FW release.
  - Both the Intel ME Disable bits in the SPI flash descriptor (ICHSTRP0* bit 0 & MCHSTRP0* bit 0) must be set to 0 to enable the ME FW workaround.
  - MCHSTRP0* bit 7 in the SPI flash descriptor can be set to disable all other ME FW based features while keeping the Intel ME FW workaround enabled.
- Non Intel ME-Enabled Platforms: Remove LAN_PHY_PWR_CTRL Support on the Platform.
  - Isolate the LAN_PHY_PWR_CTRL signal from the LAN_DISABLE_N pin.
  - LAN_DISABLE_N has a weak integrated pull-up resistor and the Intel 82567 PHY will always remained enabled with this implementation.

Note: ICHSTRP0* and MCHSTRP0* are in the SPI flash descriptor and programmed by Original Equipment Manufactures.

For ICH10 Corporate based platforms:

- None.

Status: ICH10 Corporate: Fixed. For steppings affected, see the *Summary Table of Changes*.

ICH10 Consumer: No Fix. One of the proposed workarounds must be implemented. For steppings affected, see the *Summary Table of Changes*.

7. Intel® I/O Controller Hub 10 (Intel® ICH 10) Family High-speed USB 2.0 V_{HSOH}

Problem: ICH10 High-speed USB 2.0 VHSOH may not meet the USB 2.0 specification

- The maximum expected VHSOH is 460 mV.

Implication: None known. No Fix

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

8. Intel® I/O Controller Hub 10 (Intel® ICH 10) Family 1.5 Gb/s SATA Signal Voltage Level

Problem: The ICH10 1.5 Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the ICH10 SATA 1.5 Gb/s (Gen1i and Gen1m) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (Section 7.2.1 of Serial ATA Specification, rev 2.5).

Implication: None Known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

9. Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family System Reset with Intel® Anti-Theft Technology

Problem: If Intel Anti-Theft Technology is enabled on a platform, a CF9h write of 06h or 0Eh when the CF9h Global Reset bit is clear (D31:F0:ACh:bit 20) will cause the ICH10 to not complete the reset sequence properly.

Implication: The ICH10 will complete a global reset after 4 seconds instead of an immediate host partition reset.

Workaround: For ICH10 Corporate A0/A1 silicon none. For ICH10 Corporate B0 silicon a BIOS workaround must be implemented. See the ICH10 BIOS specification for details.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

10. Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family LAN_RST# Assertion on Sx/MOff Entry

Problem: If the integrated LAN controller is powered down (LAN_RST# is asserted) in Sx/Moff, the SPI controller may not reset completely.

— Platforms that do not support the integrated LAN controller (LAN_RST# is always asserted) are not impacted.

— Platforms that always power VccLAN3_3 in S0-S5 are also not impacted.

Implication: Upon platform wake, the integrated LAN Controller and Intel Management Engine may be unable to initialize or respond to PCI configuration space accesses which can cause the platform to hang with IERR# asserted by the CPU.

Workaround: For platforms without Intel ME FW, one of the following options maybe be implemented:

1. Motherboard design must ensure LAN_RST# asserts within 500 nanoseconds of SLP_M# asserting on Sx/Moff entry or
2. VccLAN3_3 must always be powered in S0-S5

Note: ICHSTRP0* Bits 29:27 must be set to 000b if using one of the hardware based workarounds above.

For platforms with Intel ME FW:

This issue is resolved with Intel ME FW 1079 or later and requires ICHSTRP0* bits 29:27 to be set correctly. See table below for platform configuration specific settings.

Table 1. ICHSTRP0 Bits 29:27 Setting Recommendations

Motherboard LAN Power Configuration	ICHSTRP0* Bits 29:27 Settings
VccLAN3_3 is tied to VccSus3_3	000b
Design ensures LAN_RST# asserts within 500 nanoseconds of SLP_M# assertion on Sx/MOff entry	
VccLAN3_3 is tied to Vcc3_3	001b
VccLAN3_3 is powered of VccSus3_3 using WOL_EN and SLP_M# Or gate	010b
Reserved	011b-111b

Note: ICHSTRP0* is in the SPI flash descriptor and programmed by Original Equipment Manufactures.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

11. Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family Power Button Override

Problem: When in S0/1 after waking from a sleep state (S3-S5), triggering a power button override event will require the ICH10 PWRBTN# pin to be driven low for up to 9-10 seconds.

Note: ICH10 Corporate based platforms always require PWRBTN# to assert for 9-10 seconds to trigger a power button override event when the platform is in S3 or S4. This desired behavior ensures a wake event that is delayed by SLP_S3# and/or SLP_S4# stretching can be observed before unintentionally triggering a power button override event.

Implication: Instead of taking 4-5 seconds to initiate a power button override event from S0/1, ICH10 corporate based platforms may require PWRBTN# to assert for up to 9-10 seconds.

Workaround: The Intel® Management Engine's capability allows for a FW workaround which ensures a power button override event is triggered when PWRBTN# is asserted for 4-5 seconds in S0/1. This workaround has been included in the Intel® Management Engine Firmware 5.0 McCreary Production Candidate release.

Note: As long as ME FW (PC or later release) is included in the ME region on the SPI device the FW workaround will always be enabled, even if ME is disabled in the flash descriptor.

A workaround is not available for platforms that do not support ME FW.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

12. Intel® I/O Controller Hub 10 (Intel® ICH 10) Corporate Family ME SMBus/SMLink Clock Frequency

Problem: When ICHSTRP0* bits 15:14 for ME SMBus Controller 2 and/or 13:12 for ME SMBus Controller 1 are set to 01 (EDS recommended value), the ME SMBus Controllers will drive the bus at 125 kHz instead of the expected 100 kHz.

— The host SMBus controller is not impacted by this issue. The host SMBus controller when acting as the bus master will drive the SMBus clock at 100 kHz.

Implication: No known functional failures have been observed or reported to Intel.

Motherboard designers should evaluate the ability of all slave devices on the same interface as the ME SMBus controller to reliable received a 125 kHz clock input to determine impact to their platform.

Workaround: Configure the ME SMBus Controllers to run at 80 kHz by setting ICHSTRP0* bits 15:14 and/or 13:12 to 00 in the flash descriptor.

Note: ICHSTRP0* is in the SPI flash descriptor and programmed by Original Equipment Manufactures.

Status: No Plan Fix. For steppings affected, see the *Summary Table of Changes*.

13. Intel® I/O Controller Hub 10 (Intel® ICH 10) Family SATA Low Power Device Detection

Problem: Intel® ICH10 Family SATA Low Power Device Detection (SLPD) may not recognize, or may falsely detect, a SATA hot-plug event during a Partial or Slumber Link Power Management (LPM) state.

Implication: This issue affects ICH10, ICH10R, ICH10D, and ICH10DO

On systems which enable LPM, when a SATA device attached to the ICH10 is configured as External or Hot Plug capable, one of the following symptoms may occur:

- Symptom #1: A Hot-Plug or External SATA device removal which is not detected results in the OS and Intel® Matrix Storage Manager console falsely reporting the device present, or incorrectly identifying an eSATA device.
- Symptom #2: A false hot-plug removal detection may occur resulting in OS boot hang or ODD media playback hang.

Workaround: A driver workaround is available.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

14. Intel® I/O Controller Hub 10 (Intel® ICH 10) Family PCI Express Function Disable

Problem: Intel® ICH10 Family PCI Express [1:16] Disable bit in Function Disable Register may not put the PCI Express Port into a link down state if a PCI Express Device is attached.

Implication: ICH10, ICH10R, ICH10D and ICH10D0:

PCI Express Port [1:6] with a PCI Express device attached may remain in L0 State and DMI may not be able to go into L1 State.

Workaround: A BIOS workaround has been identified

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

15. Intel® I/O Controller Hub 10 (Intel® ICH 10) Family SATA SYNC Escape

Problem: When a SYNC Escape by a SATA device occurs on a D2H FIS, the ICH10 does not set the PxIS.IFS bit to '1.' This deviates from Section 6.1.9 of the Rev 1.3 Serial ATA Advanced Host Controller Interface (AHCI)

Implication: There is no known observable impact. Instead of detecting the IFS bit, software will detect a timeout error caused by the SYNC escape and then respond

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.§

16. Intel® I/O Controller Hub 10 (Intel® ICH 10) Family HPET Write Timing

Problem: A read transaction that immediately follows a write transaction to the HPET space may return an incorrect value

Implication: Implementation is dependent on the usage model as noted below:

For the HPET TIMn_COMP Timer 0 Comparator Value Register and HPET MAIN_CNT—Main Counter Value Register the issue could result in the software receiving stale data. This may result in undetermined system behavior.

Note: Timers [1:7] are not affected by this issue

For TIMERn_VAL_SET_CNF bit 6 in the TIMn_CONF—Timer n Configuration there is no known usage model for reading this bit and there are no known functional implications.

A write to a High Precision Timer Configuration (HPTC) register followed by a read to HPET register space may return all 0xFFFF_FFFFh

Workaround: A workaround is available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

17. Intel® ICH 10 Corporate May Not Detect Unsolicited SATA COMINITs

Problem: Intel® ICH10 Corporate (ICH10D and ICH10DO) may not detect an unsolicited COMINIT from a SATA device.

Implication: The SATA device may not be properly detected and configured resulting in the device not functioning as expected

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

18. Intel® ICH 10 SATA 6.0 Gbps Device Detection

Problem: Intel® ICH10 may not be able to complete SATA Out Of Band (OOB) Signaling with SATA 6.0 Gbps Devices and down shift to SATA 3.0 Gbps speed.

Implication: ICH10 may not detect SATA 6.0 Gbps Devices upon power up or resume from S3, S4 or S5 State.

Workaround: None.

Status: No Plan to Fix.

19. Incorrect IRQ(x) Vect3or Returned for 8259 Interrupts With RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0-7), an incorrect IRQ(x) vector may be returned to the CPU.

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

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Specification Changes

1. ROAEI options removal for OCW2

Remove bit setting "000" and "100" for Operational Control Word 2 Register bits [7:5] in section 13.4.8.

13.4.8 OCW2—Operational Control Word 2 Register (LPC I/F-D31:F0)

Offset Address:	Master Controller – 020h	Attribute:W	O
	Slave Controller – 0A0h	Size:	8 bits
Default Value:	Bit[4:0]=undefined, Bit[7:5]=001		

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes** (R, SL, EOI) —WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = ~~Rotate in Auto EOI Mode (Clear)~~ Reserved 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = ~~Rotate in Auto EOI Mode (Set)~~ Reserved 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used

2. The Intel® ICH 10 product wire bond material is changing from Gold (Au) to Copper Palladium (Cu-Pd).

Specifics of the change are:

- With recent advancements made in copper bonding, most of the assembly suppliers are switching to Cu-Pd as mainstream bonding process. Intel is following the High Volume Manufacturing (HVM) trend.
- Cu-Pd products are one-to-one pin compatible with Au products and there is no form, fit, function change.
- Refer to the Markings table in the "Identification Information" section of this document for new product codes, s-spec and MM#s.
  - The products with the new marking have identical quality and reliability as the current products.

Customer Impact of Change and Recommended Action:

- Intel is moving with the rest of the industry per JEDEC standards.
- There are no changes to form, fit or function.
- The Cu-Pd and Au parts are totally compatible with each other.
- Customers do not need to do anything different in the receipt and use of the Cu-Pd products in their manufacturing process.
- Customers could receive gold wire or copper palladium wire products until inventory is depleted.

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Specification Clarifications

There are no Specification Clarifications in the revision of the Specification Update.

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Documentation Changes

1. Add GPIO Signal Reset Notes

Add the following notes above Table 2-23 in Section 2.23 of the Datasheet.

Note:

1. GPIO Configurations registers within the Core Well are reset whenever PWROK is de-asserted.

2. GPIO Configuration registers within the Suspend Well are reset when RSMRST# is asserted, CF9 reset (06h or 0Eh) event occurs, or SYS_RST# is asserted.

3. GPIO24 is an exception to the other GPIO Signals in the Suspend Well and is not reset by CF9 reset (06h or 0Eh).

2. Corrected EOIFD Bit Definition

Update the EOIFD bit definition in Section 20.1.48 of the Datasheet as follows:

Bit	Description
1	**EOI Forwarding Disable (EOIFD)** — R/W. When set, EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe link. 0 = Broadcast EOI messages that are sent on the backbone are claimed by this port and fowarded across the PCIe link. 1 = Broadcast EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe Link.

3. Correct GPI_INV - GPIO Signal Invert Register Definition

Section 13.10.8 of the Datasheet is updated as follows:

GPI_INV—GPIO Signal Invert Register

Offset Address: GPIOBASE +2Ch Attribute: R/W
Default Value: 00000000h Size: 32-bit
Lockable: No Power Well: Core for 17, 16, 7:0

Bit	Description
31:16	0000h - Reserved
15:0	**Input Inversion (GP_INV[n])** — R/W. This bit only has effect if the corresponding GPIO is used as an input and used by the GPE logic, where the polarity matters. When set to '1', then the GPI is inverted as it is sent to the GPE logic that is using it. This bit has no effect on the value that is reported in the GP_LVL register. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the ICH10. In the S3, S4 or S5 states the input signal must be active for at least 2 RTC clocks to ensure detection. The setting of these bits has no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPI that are in the resume well, and will be reset to their default values by RSMRST# or by a write to the CF9h register. 0 = The corresponding GPI_STS bit is set when the ICH10 detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the ICH10 detects the state of the input pin to be low.

4. Update TBD defaults

Update the TBD defaults in Section 23, Thermal Sensor Registers

Table 23-1

Offset	Mnemonic	Register Name	Default	Type
02h-03h	DID	Device Identification	3A62h	RO
3Dh	INTPN	Interrupt Pin	03h	RO

Section 23.1.2

DID—Device Identification

Offset Address: 02h–03h Attribute: RO
Default Value: 3A62h Size: 16 bit

Section 23.1.18

INTPN—Interrupt Pin

Address Offset: 3Dh Attribute: RO
Default Value: 03h Size: 8 bits

5. Update GPIO Note #4 in Section 3.2, Output and I/O Signals and States

Make the following update to Section 3.2, Note #4 for Table 3-2 of the Datasheet

Notes:(Update for Table 3-3)

4. The states of Core and processor signals are evaluated at the times During PLTRST# and Immediately after PLTRST#. The states of the LAN and GLAN signals is are evaluated at the times During LAN_RST# and Immediately after LAN_RST#. The states of the Controller Link signals are evaluated at the times During CL_RST# and Immediately after CL_RST#. The states of the Suspend signals are evaluated at the times During RSMRST# and Immediately after RSMRST#, with an exception to GPIO signals; refer to Section 2.22, General Purpose I/O Signals, for more details on GPIO state after reset. The states of the HDA signals are evaluated at the times During HDA_RST# and Immediately after HDA_RST#.

6. Make Correction to Table 5-40

Make the following correction to Table 5-40 in Section 5.13.13, Reset Behavior, in the Datasheet.

Table 5-40. Causes of Host and Global Resets

Trigger	Host Reset without Power Cycle	Host Reset with Power Cycle	Global Reset with Power Cycle
Power Failure: PWROK signal or VRMPWRGD signal goes inactive or RSMRST# asserts	No	Yes	Yes (Note 2)

7. Update bit definition for Second_TO_STS

Update the following bit definition for Second_TO_STS in Section 13.9.5, TCO2_STS - TCO2 Status Register, in the Datasheet.

Bit	Description
1	**SECOND_TO_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it, or by a RSMRST#. 1 = ICH10 sets this bit to 1 to indicate that the TIMEOUT bit is set and a second timeout occurred. If this bit is set and the NO_REBOOT config bit is 0, then the ICH10 will reboot the system after the second timeout. The reboot is done by asserting PLTRST#.

8. Add Foot Notes For All References to SPI Flash Descriptors ICHSTRP0 and MCHSTRP0

Add the below note to all references to SPI Flash descriptor MCHSTRP0 in Sections 5.27.2, Enabling Integrated TPM, and 22.2.5.1, FLUMAP1 - Flash Upper MAP 1 (Flash Descriptor)

***Note:** MCHSTRP0 is in the SPI flash descriptor and programmed by Original Equipment Manufacturers.

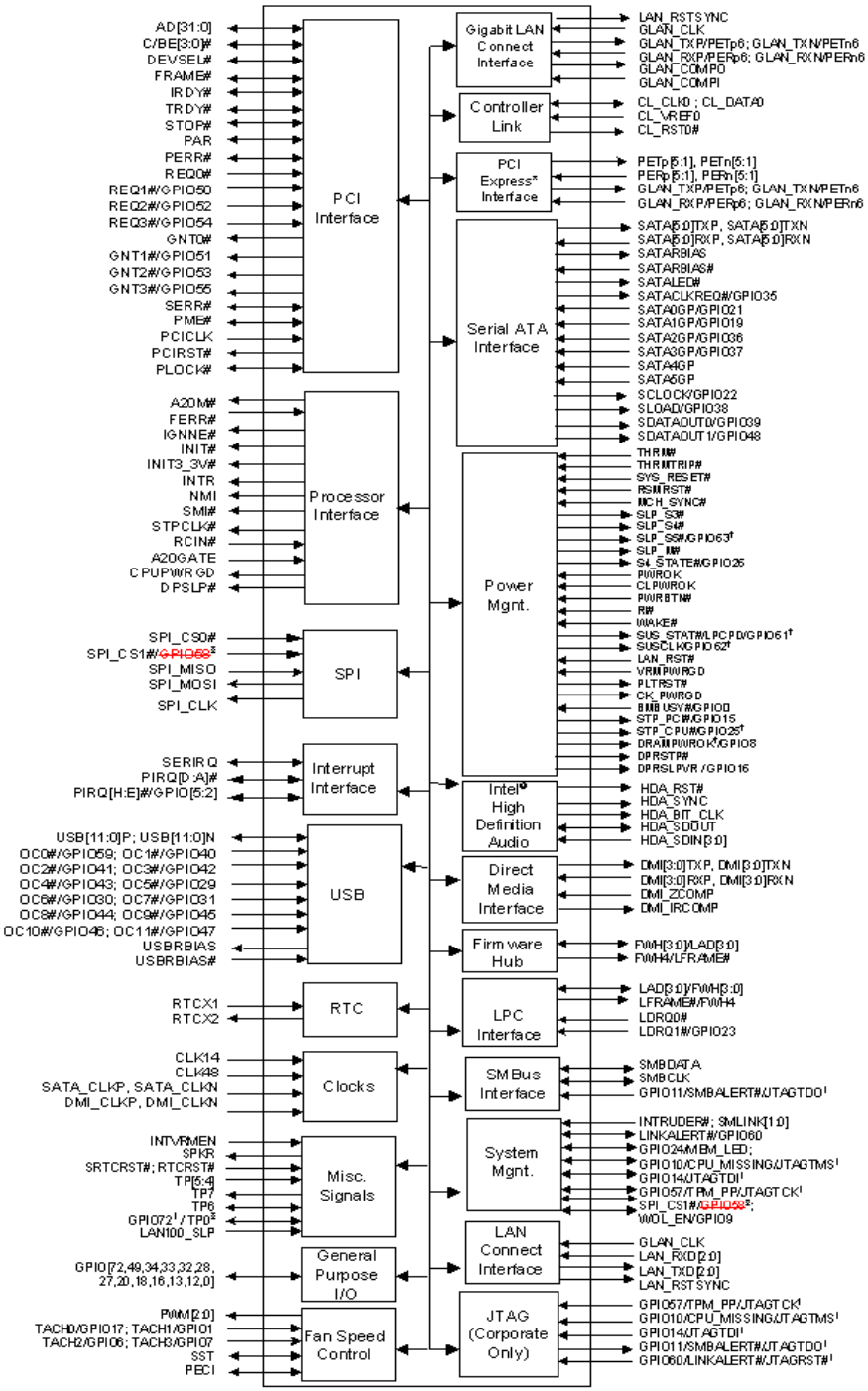
Add the below note to all references to SPI Flash descriptor ICHSTRP0 in Sections 2.20 Controller Link Signals, 3.3 Power Planes for Input Signals, 5.14.2.1, TCO Legacy/Compatible Mode, 5.14.2.2, Advanced TCO Mode, and 5.14.2.2.1, Advanced TCO Intel Manageability Engine Mode.

***Note:** ICHSTRP0 is in the SPI flash descriptor and programmed by Original Equipment Manufactures.

9. Remove GPIO58 from Figure 2-1, Intel® ICH 10 Interface Signals Block Diagram

Update the following block diagram in Section 2, Signal Description, in the Datasheet.

Figure 2-1. Intel® ICH 10 Interface Signals Block Diagram



10. Add 1.1v for VccDMI in Table 2-24

Add 1.1v support for VccDMI in Section 2.4 in Table 2-4, Power and Ground Signals, in the Datasheet.

Table 2-24. Power and Ground Signals

Name	Description
VccDMI	Power supply for DMI. 1.05V, 1.1v, 1.25V or 1.5V depending on (G)MCH's DMI voltage.

11. Correct Bit Types for PCI Express* UnCorrectable Error Severity register (UEV) Corporate Intel® ICH 10

Update the bit types for as follows in Section 20.1.62, UEV - UnCorrectable Error Severity Register Description, in the Datasheet.

20.1.62 UEV — Uncorrectable Error Severity (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 14Ch–14Fh Attribute: RO (Consumer), RW (Corporate)
Default Value: 00060011h Size: 32 bits

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Severity (URE)** — RO (Consumer), RW (Corporate). Error considered non-fatal. (Default) 1 = Error is fatal.
19	ECRC Error Severity (EE) — RO. ECRC is not supported.
18	**Malformed TLP Severity (MT)** — RO (Consumer), RW (Corporate). Error considered non-fatal. 1 = Error is fatal. (Default)
17	**Receiver Overflow Severity (RO)** — RO (Consumer), RW (Corporate). Error considered non-fatal. 1 = Error is fatal. (Default)
16	**Unexpected Completion Severity (UC)** — RO (Consumer), RW (Corporate). 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
15	**Completion Abort Severity (CA)** — RO (Consumer), RW (Corporate). 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
14	**Completion Timeout Severity (CT)** — RO (Consumer), RW (Corporate). 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
13	Flow Control Protocol Error Severity (FCPE) — RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Severity (PT)** — RO (Consumer), RW (Corporate). 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
11:5	Reserved
4	**Data Link Protocol Error Severity (DLPE)** — RO (Consumer), RW (Corporate). 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:1	Reserved
0	Training Error Severity (TE) — RO. TE is not supported.

12. Correct PCI Express* DSTS register definition for bit 1 (NFED)

Update the bit definition for bit 2(NFED) in Section 20.1.27, DTST- Device Status Register Description, in the Datasheet to match PCI Express* Base Specification Revision 1.1.

Section 20.1.27 DSTS—Device Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 4Ah–4Bh
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
1	**Non-Fatal Error Detected (NFED)** — R/WC. Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred.

13. Correct SMBCLK_CTL bit default value

Correct SMBCLK_CTL bit 2 default value defined in Section 19.2.14, SMBus_PIN_CTL—SMBus Pin Control Register (SMBus—D31:F3), in the Datasheet.

Bit	Description
2	**SMBCLK_CTL** — R/W. 1 = The SMBCLK pin is **not** overdriven low. The other SMBus logic controls the state of the pin. (Default) 0 = ICH10 drives the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin.

14. Correct Table 2-24, Strap selection for Boot BIOS Destination

Correct Boot BIOS Destination strap selection definition in Table 2-24, Functional Strap Definitions (Sheet 2 of 3), in the Datasheet.

<table>
<tr><th>Signal</th><th>Usage</th><th>When Sampled</th><th>Comment</th></tr>
<tr><td>GNT0#</td><td>Boot BIOS Destination Selection 1</td><td>Rising Edge of PWROK</td><td>This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 1strap.
Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination
0 / X / SPI
1 / 0 / PCI
1 / 1 / LPC

Note: If option 11 LPC is selected, BIOS may still be placed on LPC, but all platforms with ICH10 (Corporate Only) require SPI flash connected directly to the ICH's SPI bus with a valid descriptor in order to boot.
NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel Management Engine or Integrated GbE LAN.</td></tr>
<tr><td>SPI_CS1#</td><td>Boot BIOS Destination Selection 0</td><td>Rising Edge of CLPWROK</td><td>This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination
0 / X / SPI
1 / 0 / PCI
1 / 1 / LPC

Note: If option 11 LPC is selected, BIOS may still be placed on LPC, but all platforms with ICH10 (Corporate Only) require SPI flash connected directly to the ICH's SPI bus with a valid descriptor in order to boot.
NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel Management Engine or Integrated GbE LAN.</td></tr>
</table>

15. Correct Section 5.13.6.5, Sx-G3-Sx, Handling Power Failures, regarding possible wake events following a power failure

Correct selection 5.13.6.5, Sx-G3-Sx, Handling Power Failures, in the Datasheet

Section 5.13.6.5, Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). The following wake events can wake the system following a power loss by either RSMRST# going low and enabling by default, the enable bits reside in the RTC well or the wake event is always enabled.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the ICH10 exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because V_{CC}-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.
2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit is set and the system interprets that as a wake event.
3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.
4. PCI Express Wake# Signal: The PCIEXPWAK_DIS bit is cleared by RSMRST# going low enabling PCI Express Ports to wake the platform after a power loss. The PCIEXPWAK_STS bit is also cleared when RSMRST# goes low.
5. PME_B0: PME_B0_EN is in the RTC Well and is preserved after a power loss. The PME_B0_STS bit is also cleared when RSMRST# goes low.
6. PME: PME_EN: is in the RTC Well and is preserved after a power loss. The PME_STS bit is also cleared when RSMRST# goes low.
7. Host SMBUS: SMBUSALERT# or Slave Wake message is always enabled as Wake Event
8. ME Non-Maskable Wake: Always enabled as Wake Event.
9. WOL Enable Override (Corporate only): is in the RTC Well and is preserved after a power loss. The WOL_OVR_WK_STS bit is cleared by software.

The ICH10 monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

16. Correct Section 10.1.45, Bit 0 definition

Correct selection 10.1.45 CIR5—Chipset Initialization Register 5 in the Datasheet

10.1.45 CIR5—Chipset Initialization Register 5

Offset Address:	1D40h–1D47h	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64-bit

Bit	Description
63:0	Reserved

17. Correct Section 13.1.23, Bits 15:2 definition

Correct Section 13.1.23, GEN1_DEC-LPC I/F Generic Decode Range 1 Register, in the Datasheet.

13.1.23 GEN1_DEC-LPC I/F Generic Decode Range 1 Register (LPC I/F-D31:F0)

Offset Address: 84h–87h
Default Value: 00000000h
Attribute: R/W
Size: 32 bit
Power Well: Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask** — R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 1 Base Address (GEN1_BASE)** — R/W. **NOTE:** The ICH Does not provide decode down to the word or byte level.
1	Reserved
0	**Generic Decode Range 1 Enable (GEN1_EN)** — R/W. 0 = Disable. 1 = Enable the GEN1 I/O range to be forwarded to the LPC I/F.

18. Correct A20M# Signal Description

Correct A20M# signal description in Table 2-12, Processor Interface Signals, in the ICH10 Datasheet.

Name	Type	Description
A20M#	O	**Mask A20**: A20M# will go ~~active~~ inactive based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.

19. Update Section 8.2 in the Datasheet

The title of Section 8.2 of the ICH10 Datasheet is changed as follows.

8.2 Absolute Maximum and Minimum Ratings

The following paragraphs are added to Section 8.2:

Table 8-1 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to

conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the ICH10 contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

20. Correct OUTSTRMPAY Register information

Section 18.2.10 of the Datasheet is updated as follows:

OUTSTRMPAY—Output Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	HDBAR + 18h	Attribute:	RO
Default Value:	0030h	Size:	16 bits

Bit	Description
15:8 ~~15:14~~	Reserved ~~Output FIFO Padding Type (OPADTYPE) — RO. This field indicates how the controller pads the samples in the controller's buffer (FIFO). Controllers may not pad at all or may pad to byte or memory container sizes.~~ ~~0h = Controller pads all samples to bytes~~ ~~1h = Reserved~~ ~~2h = Controller pads to memory container size~~ ~~3h = Controller does not pad and uses samples directly~~
7:0 ~~13:0~~	**Output Stream Payload Capability (OUTSTRMPAY)** — RO. This field indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. The maximum supported is 48 Words (96B); therefore, a value of 30h is reported in this register. ~~The value does not specify the number of words actually transmitted in the frame, but is the size of the data in the controller buffer (FIFO) after the samples are padded as specified by OPADTYPE. Thus, to compute the supported streams, each sample is padded according to OPADTYPE and then multiplied by the number of channels and samples per frame. If this computed value is larger than OUTSTRMPAY, then that stream is not supported. The value specified is not affected by striping.~~ Software must ensure that a format that would cause more Words per frame than indicated is not programmed into the Output Stream Descriptor Register. 00h = 0 words 01h = 1 word payload … FFh = 255h word payload ~~The value may be larger than the OUTPAY register value in some cases.~~

21. Correct INSTRMPAY Register information

Section 18.2.11 of the Datasheet is updated as follows:

INSTRMPAY—Input Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	HDBAR + 1Ah	Attribute:	RO
Default Value:	0018h	Size:	16 bits

Bit	Description
15:8 ~~15:14~~	Reserved ~~**Input FIFO Padding Type (IPADTYPE)** — RO. This field indicates how the controller pads the samples in the controller's buffer (FIFO). Controllers may not pad at all or may pad to byte or memory container sizes.~~ ~~0h = Controller pads all samples to bytes~~ ~~1h = Reserved~~ ~~2h = Controller pads to memory container size~~ ~~3h = Controller does not pad and uses samples directly~~
7:0 ~~13:0~~	**Input Stream Payload Capability (INSTRMPAY)** — RO. This field indicates the maximum number of Words per frame for any single input stream. This measurement is in 16-bit Word quantities per 48-kHz frame. The maximum supported is 24 Words (48B); therefore, a value of 18h is reported in this register. ~~The value does not specify the number of words actually transmitted in the frame, but is the size of the data as it will be placed into the controller's buffer (FIFO). Thus, samples will be padded according to IPADTYPE before being stored into controller buffer. To compute the supported streams, each sample is padded according to IPADTYPE and then multiplied by the number of channels and samples per frame. If this computed value is larger than INSTRMPAY, then that stream is not supported. As the inbound stream tag is not stored with the samples it is not included in the word count.~~ ~~The value may be larger than INPAY register value in some cases, although values less than INPAY may also be invalid due to overhead.~~ Software must ensure that a format that would cause more Words per frame than indicated is not programmed into the Input Stream Descriptor Register. 00h = 0 words 01h = 1 word payload … FFh = 255h word payload

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