Intel® Stratix® 10 NX FPGA (AI Optimized) Product Table

	PRODUCT LINE	NX 2100	NX 2100
Resources	Logic elements (LEs)[1]	2,073,000	2,073,000
	Adaptive logic modules (ALMs)	702,720	702,720
	ALM registers	2,810,880	2,810,880
	Hyper-Registers from Intel® Hyperflex™ FPGA Architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric	
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees	
	HBM2 high-bandwidth DRAM memory gigabytes (GB)	8	16
	eSRAM memory blocks	2	2
	eSRAM memory size (Mb)	94.5	94.5
	M20K memory blocks	6,847	6,847
	M20K memory size (Mb)	134	134
	MLAB memory size (Mb)	11	11
	AI Tensor Block	3,960	3,960
	Peak INT4 or BFP12 TOPS/TFLOPS[2]	286	286
	Peak INT8 or BFP16 TOPS/TFLOPS[2]	143	143
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection	
	Hard processor system[3]	–	–
	Maximum user I/O pins	656	584
	LVDS pairs 1.6 Gbps (RX or TX)	312	288
	Total full duplex transceiver count	96	96
	GXE transceiver count - PAM4 (up to 57.8 Gbps) or non return to zero (NRZ) (up to 28.9 Gbps)	0	36 PAM-4 72 NRZ
	GXT transceiver count - NRZ (up to 28.3 Gbps)	64	16
	GX transceiver count - NRZ (up to 17.4 Gbps)	32	8
	PCI Expressa* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)	4	1
	100G Ethernet MAC (no FEC) hard IP blocks	4	1
	100G Ethernet MAC + FEC hard IP blocks	0	12
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys	
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, E-Tile Transceiver Count and H-Tile Transceiver Count[4, 5]			
F2597 pin (52.5 mm x 52.5 mm, 1.0 mm pitch)		656, 32, 312, 0, 96	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	584, 8, 288, 72, 24

Notes:
1. LE counts valid in comparing across Intel devices, and are conservative vs. competing FPGAs.
2. Derived from benchmarking an example design using f_{MAX} of AI Tensor Block in -1 speed grade device.
3. Quad-core Arm* Cortex*-A53 hard processor system not available in Intel Stratix® 10 NX devices.
4. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
5. All data is preliminary and subject to change without prior notice.

656,32,312,0,96 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, E-Tile transceiver count and H-Tile transceiver count.