

Combined with enhanced DSP blocks, the logic structure of Altera's Stratix® series and Arria® series FPGAs offer a flexible way to implement the key elements of the Quadrature Amplitude Modulation (QAM) signal-processing path in any region. With their innovative logic structure, enhanced dedicated DSP blocks, and the revolutionary memory blocks, Stratix series and Arria series FPGAs are perfect for cable head-end system designers who want flexibility and speedy time to market. In addition to these advanced features, Altera also provides an extensive set of IP cores and EDA tools to help simplify the design process.

## Introduction

With the advancement of digital entertainment and broadband technology, there are various ways to send digital information to end users such as cable and satellite subscribers. The current digital cable systems deployed around the world use the QAM standard, which defines the input data framing structure, channel forward error encoding, filtering, and QAM mapping. With digital television (DTV), the typical downstream signal uses either a 64- or 256-QAM scheme. The data source is either ATM packets or MPEG2 transport packets (used for DTV applications). The differences in the QAM standards are in the error coding section, which is broken down by Annex A, B, or C. The North American standard uses Annex B for encoding. Combined with enhanced DSP blocks, the logic structure of Stratix series and Arria series FPGAs offer a flexible way to implement the key elements of the QAM signal-processing path in any region. [Table 1](#) lists the different digital cable standards deployed in key areas of the world.

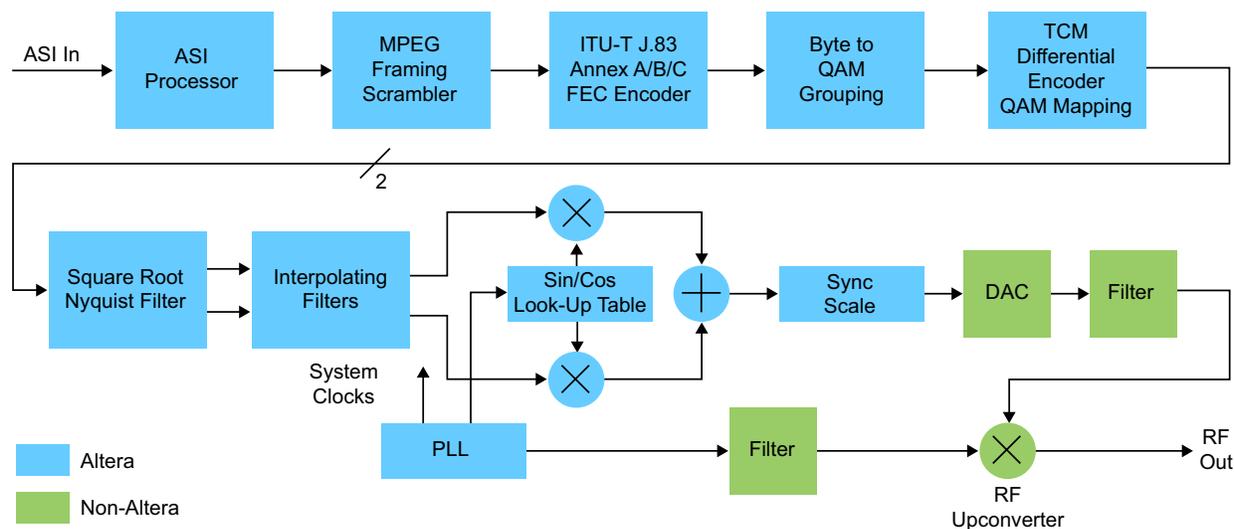
**Table 1. Digital Cable Standards**

Location	QAM Standard	Annex
North America	ITU-T/J.83B	B
Europe	DVB-C	A
China	DVB-C, DTV-C	A
Japan	ITU-T/J.83B	C

## QAM Application Requirements

Because manufacturers market and adapt their products to different geographical locations that have different standards, it is impractical to use ASSPs or custom ASICs to design a cable system. Stratix series and Arria series FPGAs can help design a system that can adapt to a wide variety of standards within DTV standards. Designers can implement the entire baseband signal processing in Stratix series and Arria series FPGAs, and can configure the FPGA while cable systems are operating. Multiple QAM encoder channels can also be implemented with a single FPGA to provide the flexibility of hardware upgrades and cost savings. Figure 1 shows the major blocks of a typical 1-channel QAM.

**Figure 1. 1-Channel QAM**



## Data Source

The data input format for a DTV modulator is either a parallel or a serial MPEG2 transport interface. Most head-end equipment uses the DVB-ASI serial interface. The Stratix series and Arria series FPGAs' dedicated LVDS I/O pins, capable of up to 1-Gbps performance, are ideal for the multiple DVB-ASI channel inputs implementation. Different video streams can be multiplexed onto the FPGA QAM design for transmission. In Annex A/C, the MPEG2 transport stream is synchronized with a synchronized byte of 0x07 hex. The synchronized data is then scrambled per DVB/DAVIC standards. In Annex B, the input logic searches the MPEG2 transport stream for the synchronized byte and then replaces it with a checksum byte to improve error detection capability.

Handling the data stream requires a lot of common logic functions. The logic structure of Stratix series and Arria series FPGAs goes beyond the simple, fixed-size four-input look-up table (LUT) structure and extends its logic capacity to efficiently construct any logical functions with five or six inputs in one entity. The adaptive logic module (ALM) of Stratix series and Arria series FPGAs can also implement many seven-input functions. By supporting logical functions with more than four variables per ALM, the logic structure of Stratix series and Arria series FPGAs increases the performance of a design by:

- Reducing the number of logic levels required for the overall combinational logic

- Reducing the extra programmable routing needed in the simple, fixed-size four-input LUT implementation
- Reducing the stress on the demand for general routing resources

Research has shown that wider LUTs provide better performance, while narrower LUTs provide better logic efficiency. The ALMs of Stratix series and Arria series FPGAs offer not only the desired performance, but also adaptively accommodate the logic functions with different numbers of inputs to provide exceptional logic efficiency that is 25% better than prior FPGAs. The ALMs of Stratix series and Arria series FPGAs can effectively reduce the logic resource requirements of a design by:

- Optimally creating functions with larger input counts and packing together functions with smaller input counts (for example, in Stratix series and Arria series FPGAs, a five-input and a three-input function can be placed together in one ALM)
- Reducing the need for logic duplication by sharing logic resources for different combinational logic with common inputs
- Implementing complex arithmetic functions and combining logic and arithmetic operations such as data selection before summation and subtraction
- Implementing high-input-count arithmetic functions such as an adder tree
- Allowing register packing
- Using a register chain

## Memory and Multiplexer for Channel Encoding

To improve the performance of a communication channel, forward error correction (FEC) channel coding corrects errors during transmission. The FEC acts as an overhead to the actual data payload. The most common FEC is Reed-Solomon encoding, which calculates the checksum appended to the data packet at the source. At the receiving end of the transmission, any discrepancy in the checksum indicates an error in transmission. Reed-Solomon corrects for block errors, which are typically caused by burst errors across the transmission channel. Furthermore, words in error can be corrected up to one correction for every two checksum words. The Reed-Solomon encoder is already a proven Altera® MegaCore® function.

The ITU J.83 Annex B FEC has an additional powerful channel coding scheme called trellis coding. Because trellis coding is embedded in the modulation process, it often carries the name trellis coded modulation (TCM). For further information, refer to [“Trellis Coded Modulation” on page 5](#).

## Interleaving

Data interleaving spreads data over a variable period of time in order to combat adjacent burst errors that the Reed-Solomon decoder cannot handle. Without data interleaving, many adjacent errors cannot be corrected. With data interleaving, data is transmitted by spacing the content of consecutive packets. Therefore, burst errors are distributed over many data packets, so that the FEC has fewer errors to correct in each packet.

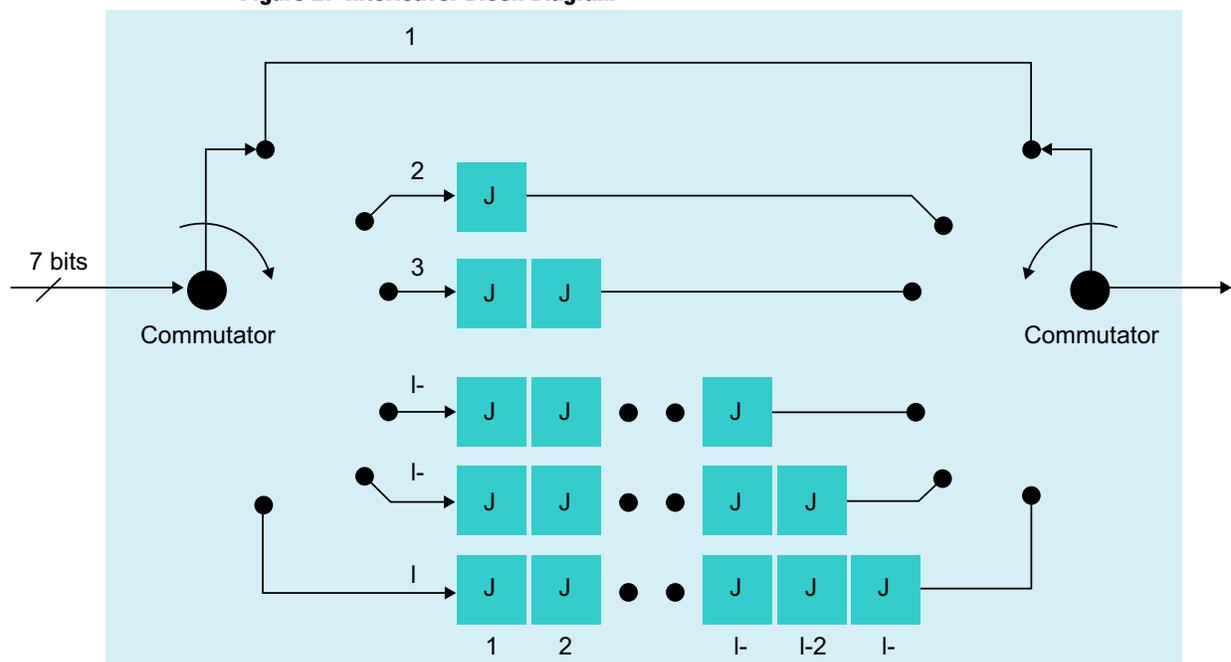
Data interleaving transmits the first word of the current packet, then the first word of the previous packet, then the first word of the second previous packet, and so on, until all first words of all packets are transmitted. It then starts again with the second words of the set of packets, and then the third words, and so on, until all the data is transmitted.

Data interleaving requires many memory and multiplexing operations. The logic structure of Stratix series and Arria series FPGAs is ideal for building multiplexer and demultiplexer structures, and can efficiently implement large multiplexers, barrel shifters, crossbar switches, and state machines. Stratix series and Arria series FPGAs offer up to 9 Mb of dedicated memory blocks that can be used for data interleaving.

If required, external memory interfaces are also available for deeper interleaving. Stratix series and Arria series FPGAs are available in advanced pin packages that provide board area savings as well as high pin-counts. These high-pin-count packages offer easy access to I/O pins for implementing with external memory chips and other support devices in the system.

Interleaving is defined by two parameters,  $I$  and  $J$ .  $I \times J =$  packet size or multiples of packet size. A typical interleaver is shown in Figure 2.

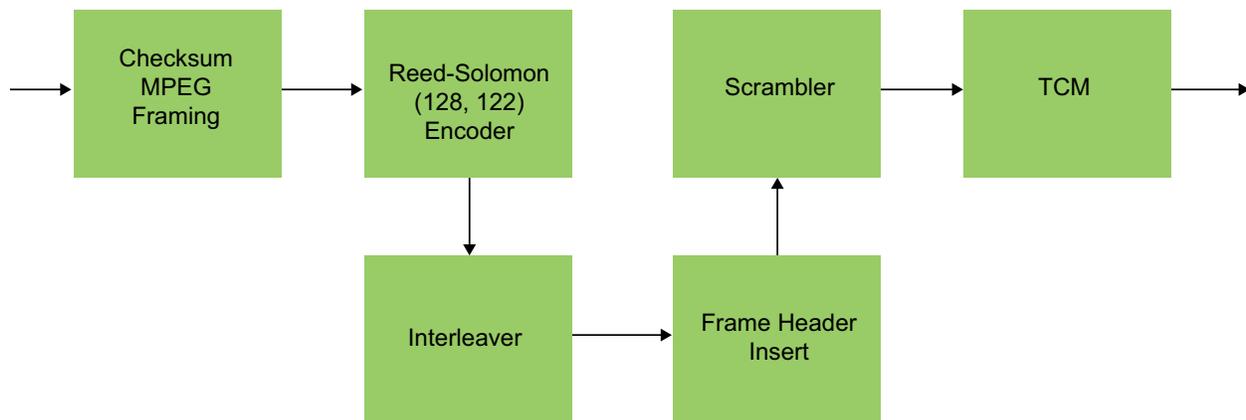
**Figure 2. Interleaver Block Diagram**



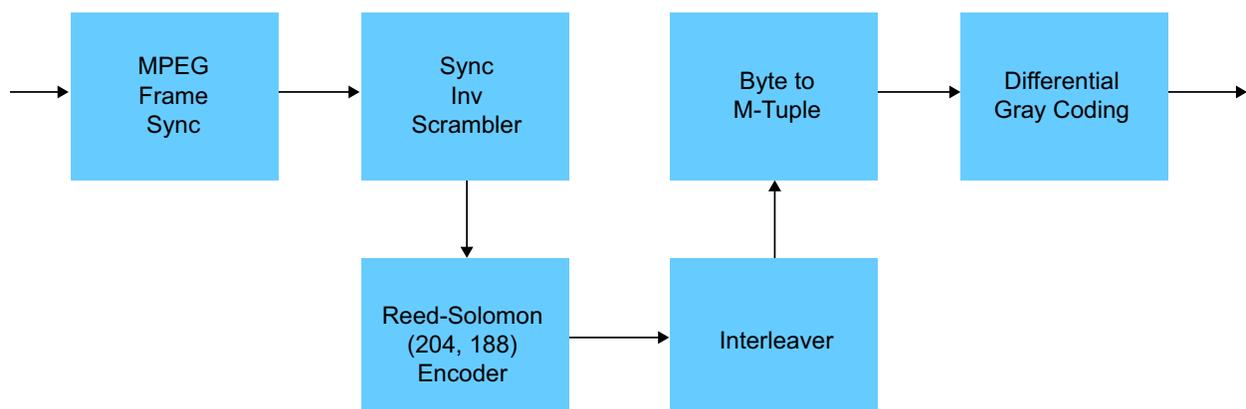
In Annex B, the packet size is 128 words (122 data words and 6 Reed-Solomon checksum words), so the available interleaves are  $I = 128 \times J = 1$ , or  $I = 64 \times J = 2$ , or  $I = 32 \times J = 4$ . Or the enhanced interleaves are  $I = 128 \times J = 2$ , or  $I = 128 \times J = 3$ , up to  $I = 128 \times J = 8$ .

In  $I = 128 \times J = 1$ , there is a set of 128 packets. In  $I = 128 \times J = n$ , there are  $n$  sets of 128 packets. In  $I = m \times J = n$ , there are  $n$  sets of  $m$  packets such that  $m \times n = 128$ .

Figure 3 shows the block diagram of an Annex B channel encoder. The interleaver depth can be 8, 12, 16, 32, 64, or 128 for DOCSIS, or 12 for EuroDOCSIS. The default value is 8 for DOCSIS.

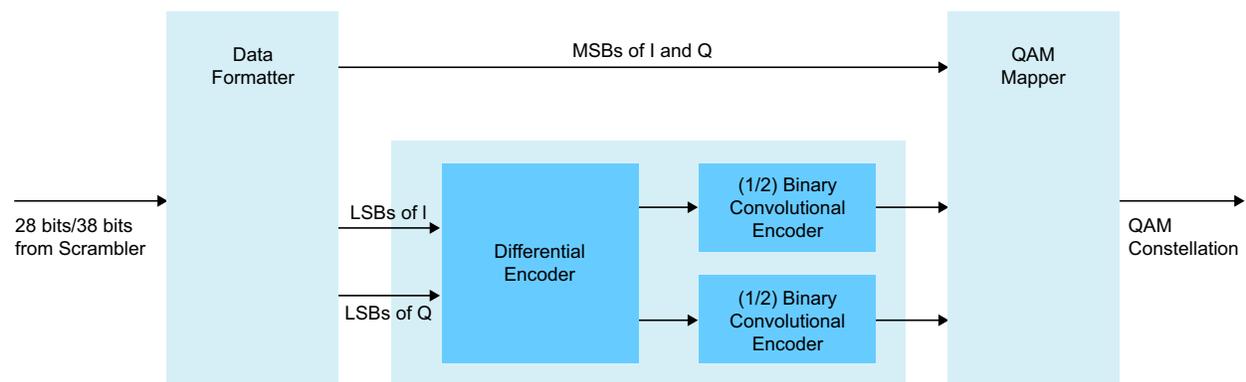
**Figure 3. ITU J.83 Annex B Channel Encoder**

In Annex A/C, packet sizes are 204 words, and the interleaving is fixed at  $I = 12 \times J = 17$ . Figure 4 shows the block diagram of an Annex A/C channel encoder.

**Figure 4. ITU J.83 Annex A/C Channel Encoder**

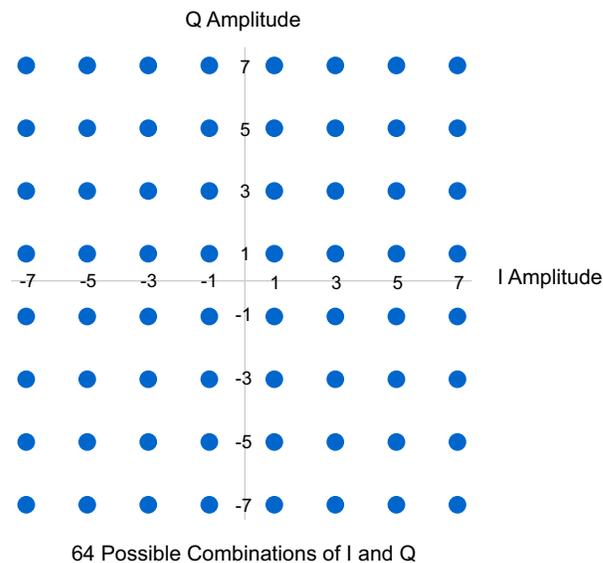
## Trellis Coded Modulation

TCM uses an encoder to select an optimal sequence from the data stream and a map of the QAM constellation. The constellation in TCM is usually larger than that required for the data stream, and the encoder generates a sequence of wider words mapped such that the transition distances in the constellation are maximized. Figure 5 shows the generic block diagram for typical TCM.

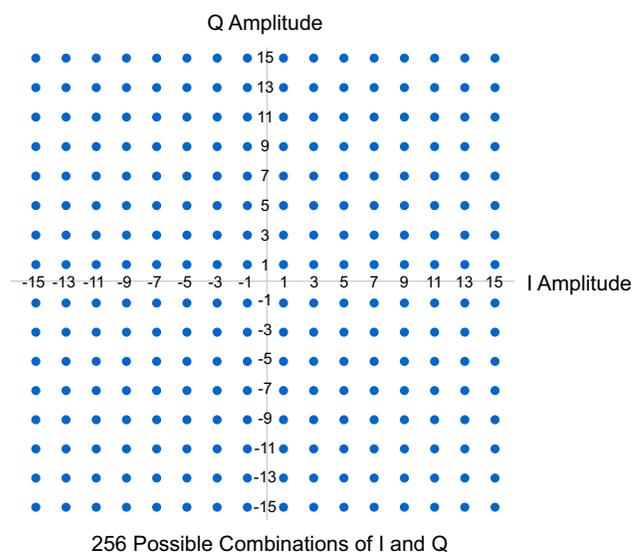
**Figure 5. TCM Block Diagram**

The purpose of increasing the constellation size is to implement coding rules where transitions from a constellation point are allowed to go to only some specific other points (not all combinations are allowed), depending on the previous data. The objective is to increase the distance of transitions over that data-stream sequence. TCM reduces the probability of error for a given signal-to-noise ratio (SNR). Therefore, for a given error rate, the SNR can be reduced by  $x$  dB, known as the coding gain. The TCM coding gain for the ITU J.83 Annex B is around 4.5 dB for 64-QAM and 256-QAM. The TCM block includes the differential encoder, binary convolutional encoder, and QAM mapper. Figure 6 maps a 64-QAM constellation diagram, and Figure 7 maps a 256-QAM constellation diagram.

**Figure 6. 64-QAM Constellation**

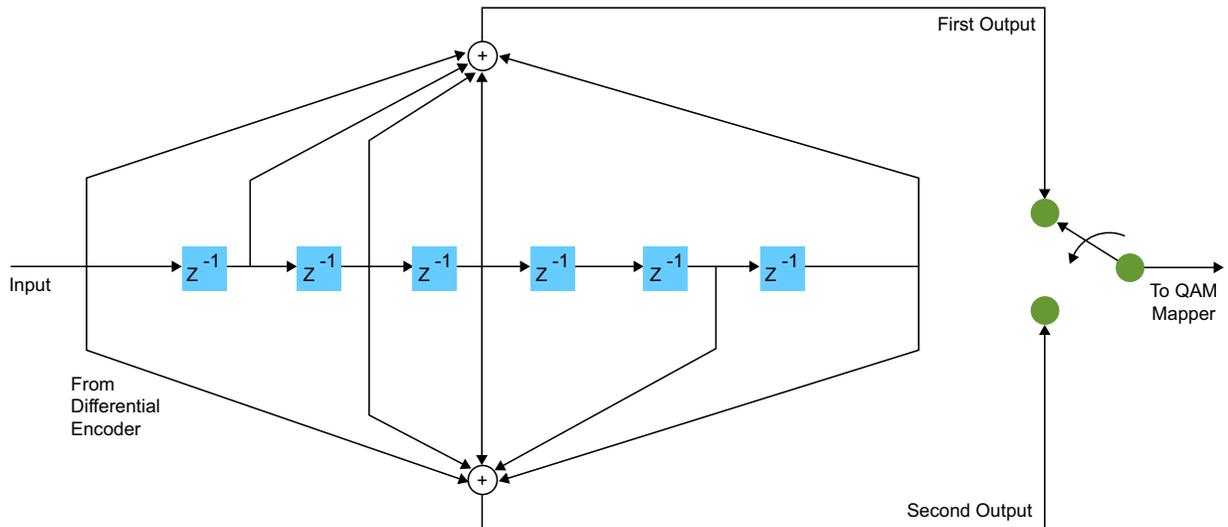


**Figure 7. 256-QAM Constellation**



Designers can use the DSP blocks in Stratix series and Arria series FPGAs to implement a binary convolutional coder. The structure of a convolutional coder is similar to a digital filter. Figure 8 shows the convolutional encoder block diagram.

Figure 8. Binary Convolutional Encoder



## Raised Cosine Filter

Transmitting video data over a band-limited channel requires a filter to shape the digital pulses so that intersymbol interference (ISI) can be controlled or eliminated. Typically, a programmable square-root raised cosine filter (a finite impulse response (FIR) filter) is used for pulse shaping in a cable transmission facility, with the following transfer function:

$$H(f) = \left( \frac{\sin\left(\frac{\pi f}{2}\right)}{\frac{\pi f}{T}} \right) \left( \frac{\cos\left(\frac{\alpha \pi f}{T}\right)}{1 - \left(\frac{2\alpha f}{T}\right)^2} \right)$$

The excess bandwidth factor's alpha value is 12%, 15%, or 18%, depending on the standard used. The enhanced DSP blocks of Stratix series and Arria series FPGAs can be used to efficiently implement a programmable filter for cable modulation.

 A FIR MegaCore function is available to ease the implementation of the filter. For further information, refer to the [FIR Compiler II MegaCore Function User Guide](#).

## Digital Upconverter

A numerically controlled oscillator (NCO) is a logic block that outputs a digital frequency based on a numerical input. The output waveform can be any type of waveform, but is typically a sawtooth (ramp), sine, or both sine and cosine. The output frequency is limited to one half of the master clock frequency.

An NCO is composed of a programmable counter and a waveform LUT. The counter, or phase accumulator, counts based on the frequency input. This frequency input is added to the value of the current count on each clock edge. The higher the input value, the faster the counter reaches its maximum value and rolls over. The counter value is used as the index to a LUT. The LUT output determines the waveform output.

- Altera provides a NCO MegaCore function that allows the designer to implement a NCO graphically, while Altera's IP Toolbench interface helps designers create a variety of NCO architectures. For further information, refer to the *NCO MegaCore Function User Guide*.

## Conclusion

A cable system using the QAM standard is signal-processing intensive. With their innovative logic structure, enhanced dedicated DSP blocks, and the revolutionary memory blocks, Stratix series and Arria series FPGAs are perfect for cable head-end system designers who want flexibility and speedy time to market. In addition to the advanced features that Stratix series and Arria series FPGAs offer, Altera also provides an extensive set of IP cores and EDA tools to help simplify the design process.

## Further Information

- *FIR Compiler II MegaCore Function User Guide*:  
[www.altera.com/literature/ug/ug\\_fir\\_compiler\\_ii.pdf](http://www.altera.com/literature/ug/ug_fir_compiler_ii.pdf)
- *NCO MegaCore Function User Guide*:  
[www.altera.com/literature/ug/ug\\_nco.pdf](http://www.altera.com/literature/ug/ug_nco.pdf)

## Document Revision History

Table 2 shows the revision history for this document.

**Table 2. Document Revision History**

Date	Version	Changes
December 2010	2.0	<ul style="list-style-type: none"> <li>■ Minor text edits.</li> <li>■ Added Abstract.</li> <li>■ Removed Table 2, Figure 9, and Table 3</li> </ul>
January 2006	1.1	Minor text edits.
February 2004	1.0	Initial release.