White Paper

MAX II Logic Element to Macrocell Conversion Methodology

Introduction

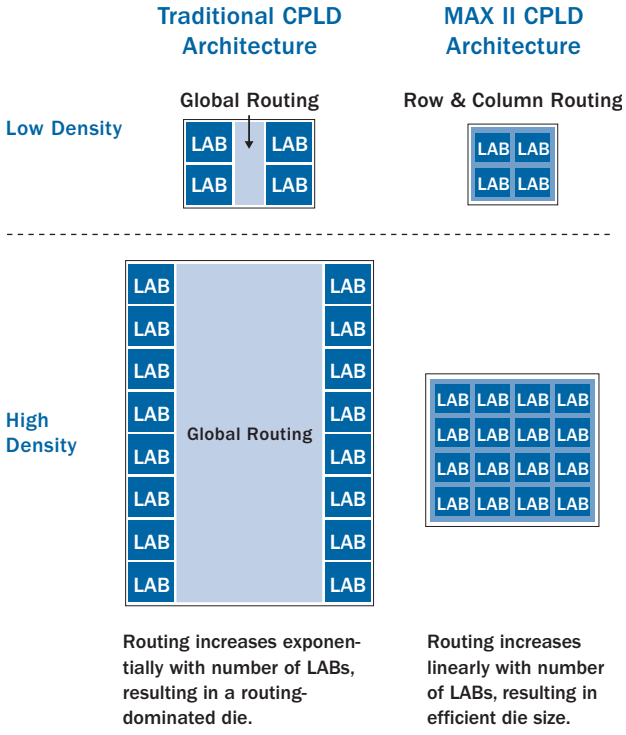
This white paper describes the methodology used to develop Altera's device density conversion guidelines for CPLDs, and is intended to assist customers converting from a product-term-based CPLD to a look-up table (LUT) CPLD when estimating density requirements.

Technology Background

The product-term based CPLD has an architecture based on AND-OR planes building macrocells with global routing. LUT-based CPLDs and FPGAs are based on LUTs with row-and-column routing. Given the differences in logic and routing there is no direct method to convert logic capacity between one architecture and the other.

The global routing of product-term-based CPLDs is not efficiently scalable to higher densities beyond several thousand gates (see Figure 1). Also, as process geometries shrink, the high-voltage transistors required for the product-term architecture do not scale. LUTs and row-and-column routing become more area efficient as processes shrink.

Figure 1. Comparison of Routing Advantages at Higher Densities



Product-term and LUT architectures are fundamentally different, as shown in Figures 2 and 3. LUT architectures are measured in logic elements (LEs) which include one, 4-input LUT plus a register (see Figure 3).

Figure 2. Product-Term AND-OR Plane

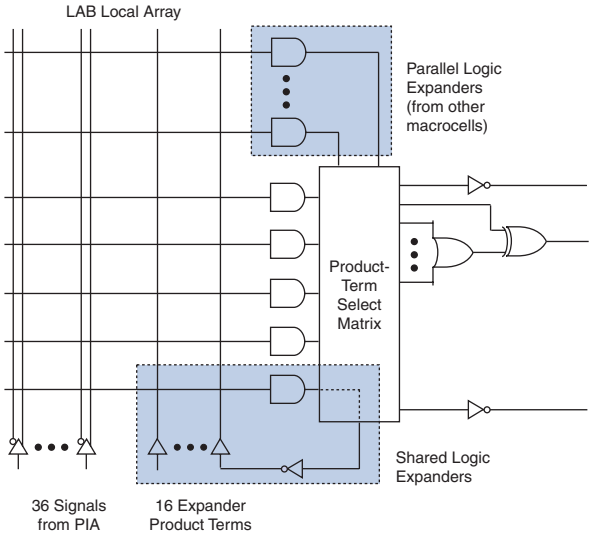
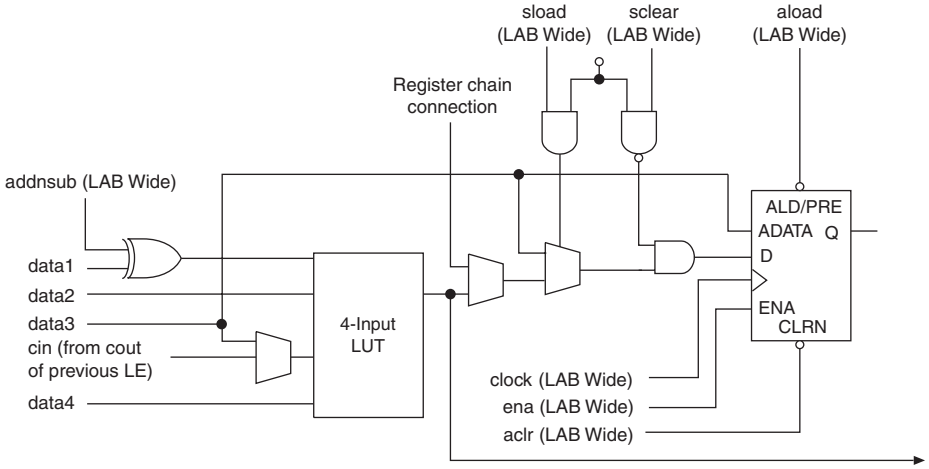


Figure 3. MAX II LE with a 4-Input LUT



Conversion Methodology & Results

Altera compiled approximately 400 designs in MAX® 7000AE and MAX II devices. From those designs, the logic utilization was compared. These designs provided an average comparison of 1.3 LEs for each macrocell.

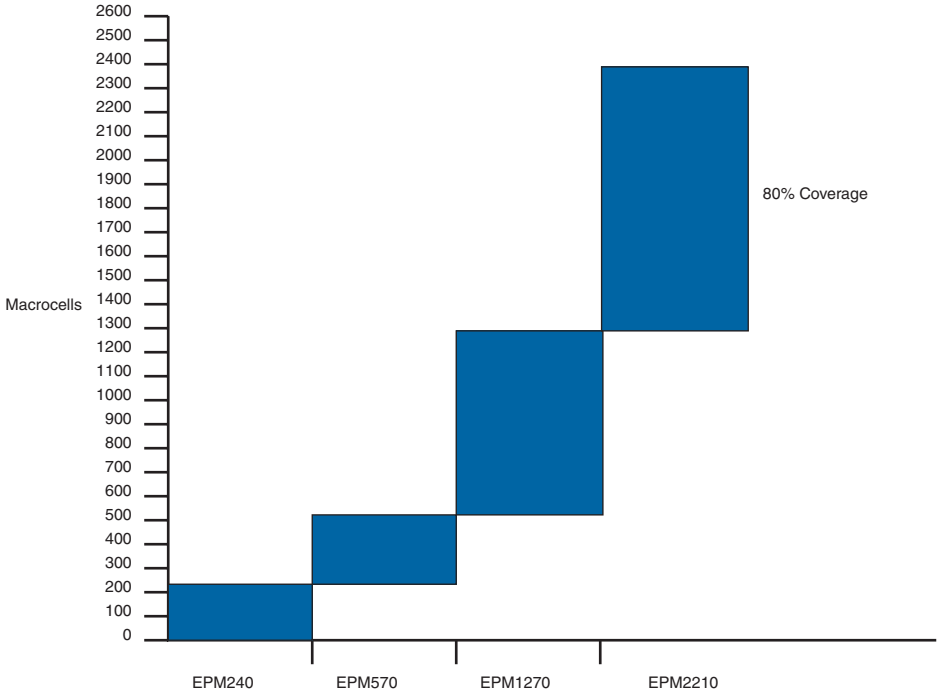
For each MAX II member, the designs were cross referenced against the logic utilization in macrocells. Table 1 shows the typical equivalent macrocell number for each density and the range of macrocell equivalents. The range provided is the macrocell range that was covered by 80% of designs. The outliers were remove and would not have been seen by the majority of designers.

Figure 4 is a graphical representation of Table 1, the corresponding equivalent macrocell densities that are common in the CPLD industry.

Table 1. MAX II LE/Macrocell Conversion Range

LEs	Macrocell Typical ~ 1.3 LEs	Macrocell Range
240	192	128 to 240
570	440	240 to 570
1,270	980	570 to 1,270
2,210	1,700	1,270 to 2,210

Figure 4. MAX II Device Coverage



Design Conversions

Determining where in the range a specific design will fall depends on the functions that are implemented. Many designs can be optimized for either architecture. An example is address decoding which can often be implemented via AND–OR or XOR functions. Decoding a single address is accomplished with a simple AND function, but an address range decode requires XOR functions. Using HDL and the Quartus® II software eliminates much of the bias toward either architecture.

Conclusion

Using the Quartus II software, designs running in product-term families can be compiled into MAX II devices with automatic device selection to determine the conversion factor for a specific design.

To develop the next generation of MAX II devices, Altera has taken advantage of LUT-based architectures to create an entirely new breed of CPLD products that radically transforms the price dynamics in this market. By extending an LUT-based architecture—combined with instant-on, non-volatile product attributes—into the low-density market, Altera introduces faster, lower-power products at less than half the price of prior generation CPLDs.

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