

MAX II I/O Characteristics During Hot Socketing

Introduction

Altera® MAX® II devices offer hot-socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot-socketing feature removes some of the difficulty faced by designers when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot-socketing feature provides:

- Support for board or device insertion and removal without system power-down
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This document describes I/O characteristics for different MAX II hot-socket cases.

☛ For more information on the MAX II hot-socketing specification, refer to *Chapter 4. Hot Socketing & Power-On Reset in MAX II Devices* of the *MAX II Device Handbook*.

Output Pin Voltage Level During Power Up and Power Down: Test Setup

The setups for the hot-socketing and power-sequencing tests are shown in Figures 1, 2, and 3. Figure 1 shows the test setup with both output pins weakly pulled up externally. Figure 2 shows the test setup with both output pins weakly pulled down externally. Figure 3 shows the test setup for both output pins without external resistors. All tests are at nominal conditions.

Channel 1 (yellow) shows the V_{CCINT} supply and channel 2 (blue) shows the V_{CCIO} supply to the device. Channel 3 (purple) shows an output pin driving high while channel 4 (green) shows an output pin driving low, for all the different conditions in the Figure 1, 2, and 3 test setups. For the different test setups, V_{CCINT} and V_{CCIO} are either ramped up or down separately, or together.

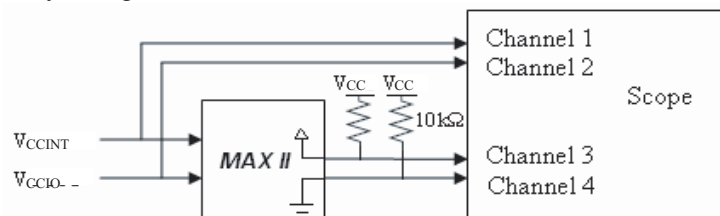


Figure 1. Output Pins With External Weak Pull-Up Resistors

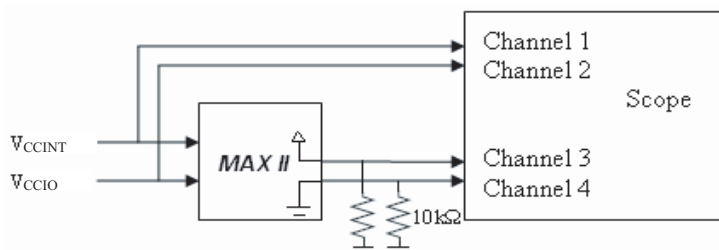


Figure 2. Output Pins With External Weak Pull-Down Resistors

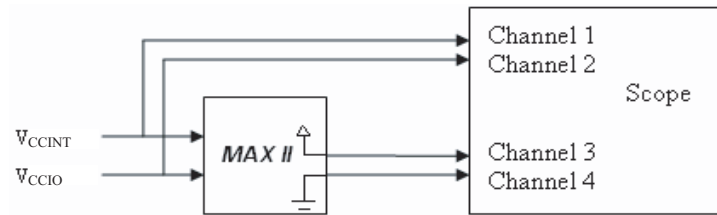


Figure 3. Output Pins Without External Resistors

Output Pin Voltage Level During Power Up and Power Down: Test Results

This section shows the output pin scope shots for different power-up sequences. Table 1 summarizes the different combinations of power-up and power-down sequences.

Table 1. Different Power-Up and Power-Down Sequence Combinations

V_{CCINT}	V_{CCIO}
0V → 3.3V	Steady 3.3 V
3.3V → 0V	Steady 3.3 V
Steady 3.3 V	0V → 3.3V
Steady 3.3 V	3.3V → 0V
0V → 3.3V	0V → 3.3V
3.3V → 0V	3.3V → 0V

If V_{CCINT} is powered up after V_{CCIO} is powered up, the internal I/O weak pull-up resistor will turn on at approximately 1.2 V V_{CCINT} . The weak pull-up resistor pulls the tri-stated I/O pin to V_{CCIO} . The device only releases the pin to user mode after the power-up timing delay (t_{CONFIG}). The power-up timing delays start from the point V_{CCINT} reaches the POR trip voltage point until the MAX II SRAM configuration completes.

If V_{CCINT} and V_{CCIO} are powered up simultaneously, the internal I/O weak pull-up resistor will turn on at approximately 0.4 V to 0.7 V V_{CCINT} , depending on the voltage of the I/O pins.

If V_{CCIO} is powered up after V_{CCINT} is powered up, the device releases the I/O pins at approximately 0.7 V to 1.2 V V_{CCIO} , depending on the voltage of the I/O pins, and the voltage level of any high-driving output pin will ramp up together with the V_{CCIO} supply after that.

Refer to *Chapter 4. Hot Socketing & Power-On Reset in MAX II Devices* of the *MAX II Device Handbook* for the POR trip point, and *Chapter 5. DC & Switching Characteristics* for the power-up timing for different devices as well as the range of the internal weak pull-up resistor.

V_{CCINT} Ramps Up, $V_{CCIO} = 3.3$ V

Figures 5 to 7 show the voltage levels of a high-driving output pin and a low-driving output pin with either an external pull-up resistor, an external pull-down resistor, or without external resistors, when V_{CCINT} ramps up from 0 V to 3.3 V, and V_{CCIO} set to 3.3 V.



Figure 4. V_{CCINT} Ramps Up, V_{CCIO} Is Steady at 3.3 V, Output Pins With External 10-k Ω Pull-Up Resistor



Figure 5. V_{CCINT} Ramps Up, V_{CCIO} Is Steady at 3.3 V, Output Pins With External 10-k Ω Pull-Down Resistor

As shown on channels 3 and 4 in Figure 5, the step before the output pins are released is the time when the internal weak pull-up resistor pulls the pins to V_{CCIO} while the external pull-down resistor pulls the pins to ground.

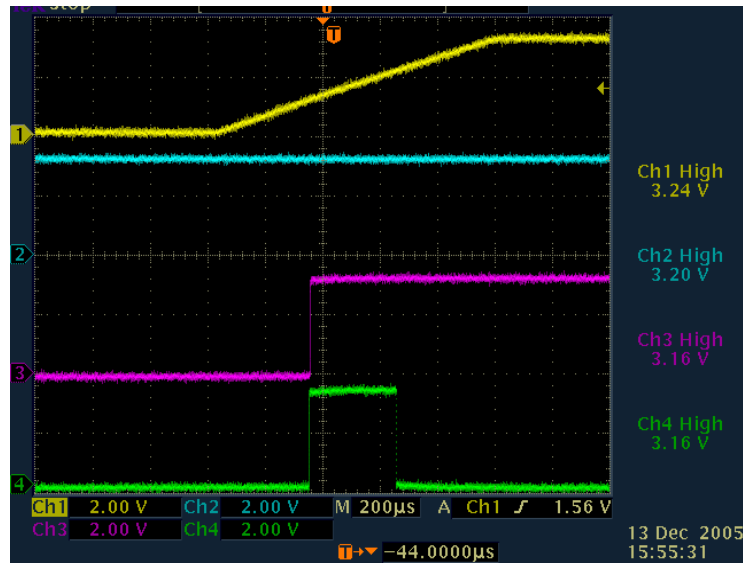


Figure 6. V_{CCINT} Ramps Up, V_{CCIO} Is Steady at 3.3 V, Output Pins Without External Resistors

As shown in channels 3 and 4 of Figure 6, the step before the output pins are released is the time when the internal weak pull-up resistor pulls the pins to V_{CCIO} .

V_{CCINT} Ramps Down, $V_{CCIO} = 3.3$ V

Figures 8 to 10 show the voltage levels of a high-driving output pin and a low-driving output pin with either an external pull-up resistor, an external pull-down resistor, or without external resistors, when V_{CCINT} ramps down from 3.3 V to 0 V, and V_{CCIO} is steady at 3.3 V.

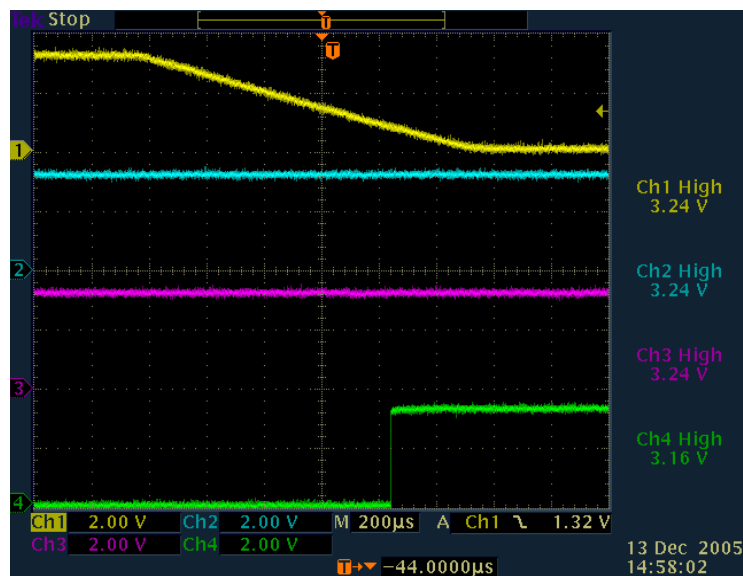


Figure 7. V_{CCINT} Ramps Down, V_{CCIO} Is Steady at 3.3 V, Output Pins With External 10-k Ω Pull-Up Resistor



Figure 8. V_{CCINT} Ramps Down, V_{CCIO} Is Steady at 3.3 V, Output Pins With External 10-k Ω Pull-Down Resistor

The step in the middle of channels 3 and 4 in Figure 8 is the time when the internal weak pull-up resistor pulls the pins to V_{CCIO} while the external pull-down resistor pulls the pins to ground.

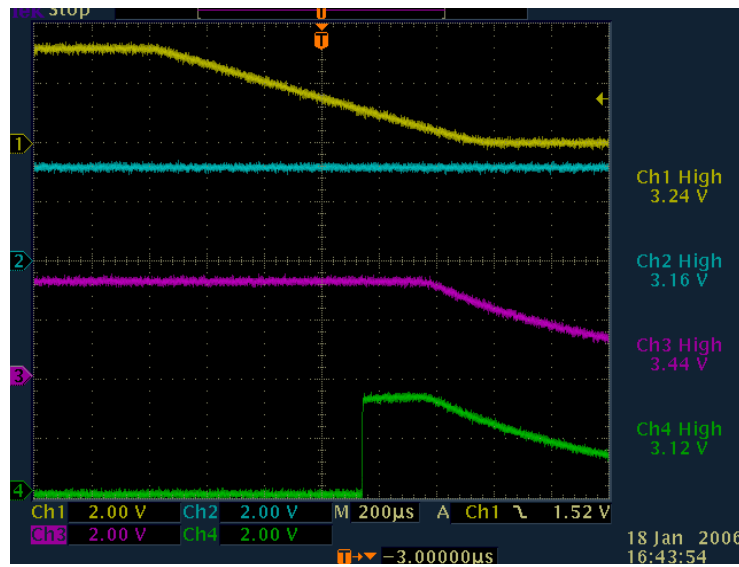


Figure 9. V_{CCINT} Ramps Down, V_{CCIO} Is Steady at 3.3 V, Output Pins Without External Resistors

$V_{CCINT} = 3.3\text{ V}$, V_{CCIO} Ramps Up

Figures 11 to 13 show the voltage levels of a high-driving output pin and a low-driving output pin with either an external pull-up resistor, an external pull-down resistor, or without external resistors, when V_{CCINT} is steady at 3.3 V, and V_{CCIO} ramps up from 0 V to 3.3 V.

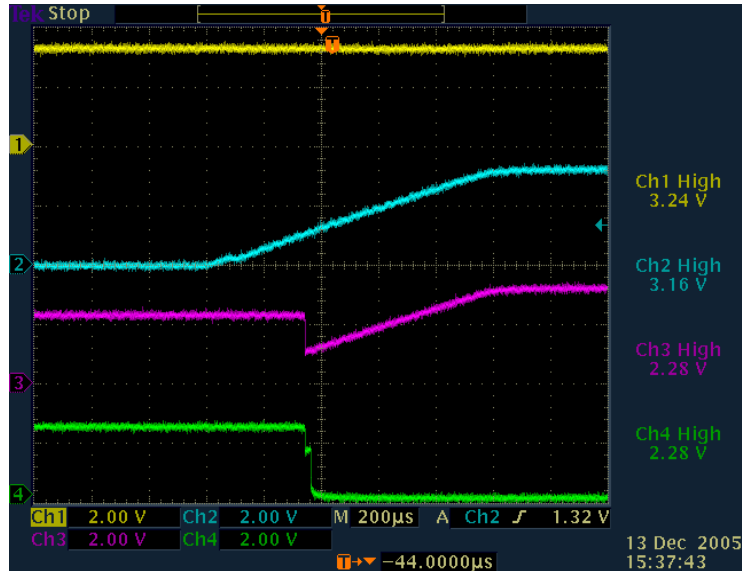


Figure 10. V_{CCINT} Is Steady at 3.3 V, V_{CCIO} Ramps Up, Output Pins With External 10-k Ω Pull-Up Resistor

The small step on channels 3 and 4 in Figure 10 is the time when the internal weak pull-up resistor pulls the pins to V_{CCIO} before the output pins are released.

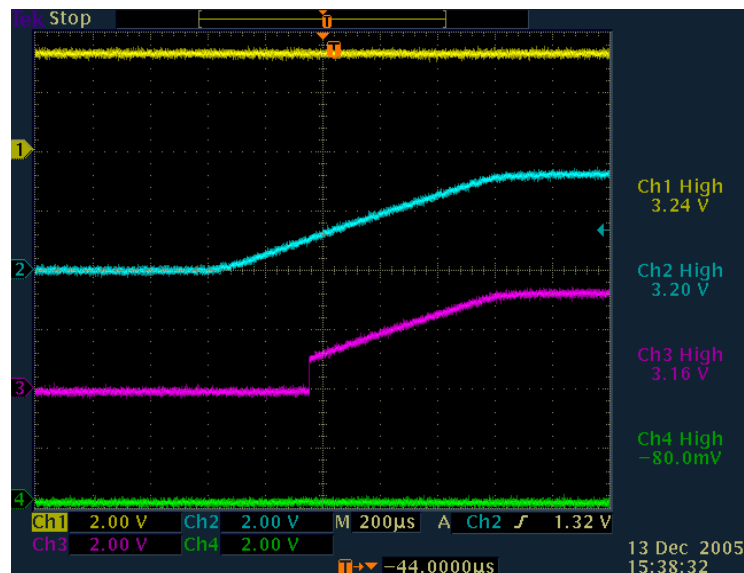


Figure 11. V_{CCINT} Is Steady at 3.3 V, V_{CCIO} Ramps Up, Output Pins With External 10-k Ω Pull-Down Resistors

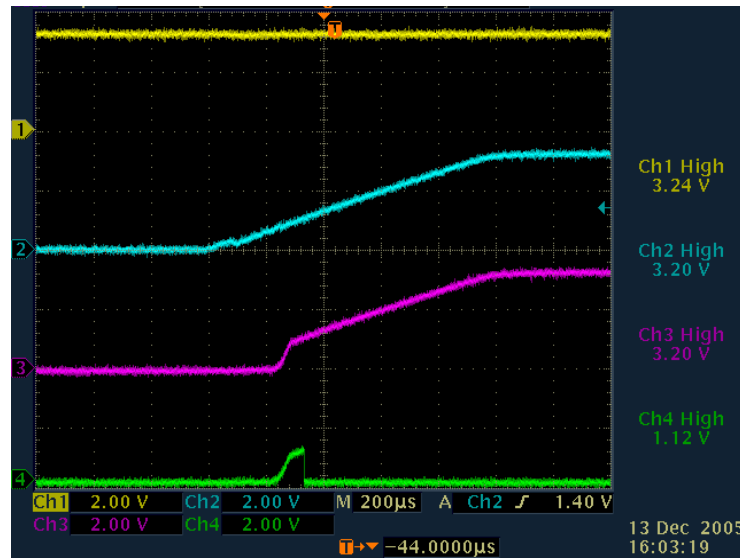


Figure 12. V_{CCINT} Is Steady at 3.3 V, V_{CCIO} Ramps Up, Output Pins Without External Resistors

The quick ramp on channels 3 and 4 in Figure 12 shows the internal weak pull-up resistor has just turned on and the pins are pulled quickly to V_{CCIO} , before slowly rising in voltage with the V_{CCIO} ramp.

$V_{CCINT} = 3.3$ V, V_{CCIO} Ramps Down

Figures 14 to 16 show the voltage levels of a high-driving output pin and a low-driving output pin with either an external pull-up resistor, an external pull-down resistor, or without external resistors, when V_{CCINT} is steady at 3.3 V, and V_{CCIO} ramps down from 3.3 V to 0 V.

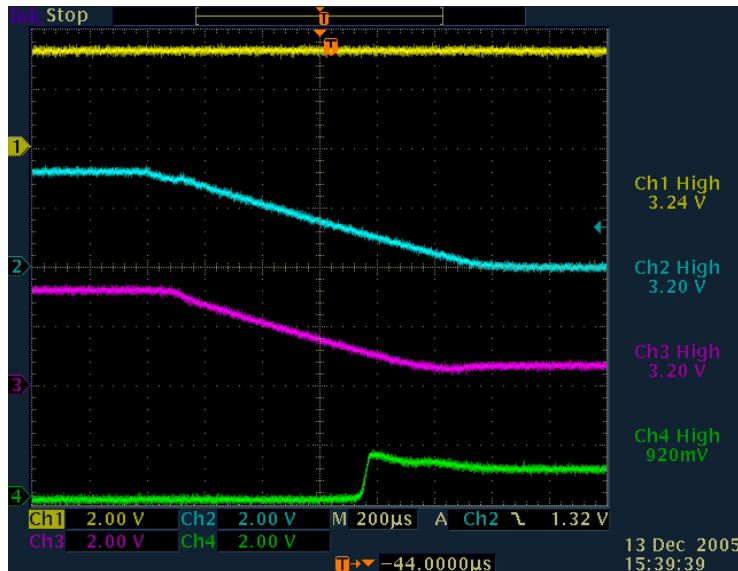


Figure 13. V_{CCINT} Is Steady at 3.3 V, V_{CCIO} Ramps Down, Output Pins With External 10-k Ω Pull-Up Resistor

The output pins on channels 3 and 4 in Figure 13 do not go to 3.3 V or 0 V after V_{CCIO} is powered down because the internal weak pull-up resistor is still active. The internal weak resistor pulls the pins to V_{CCIO} (0 V) while the external pull-up resistor pulls the pins to 3.3 V.

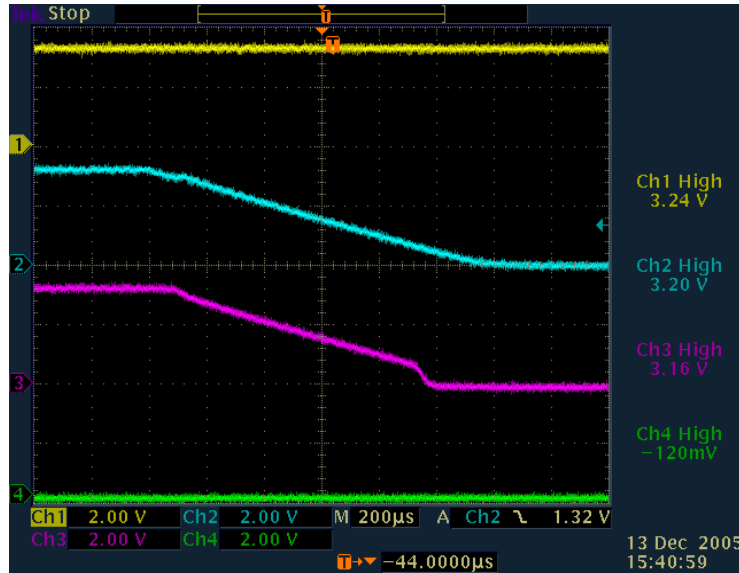


Figure 14. V_{CCINT} Is Steady at 3.3 V, V_{CCIO} Ramps Down, Output Pins With External 10-k Ω Pull-Down Resistor

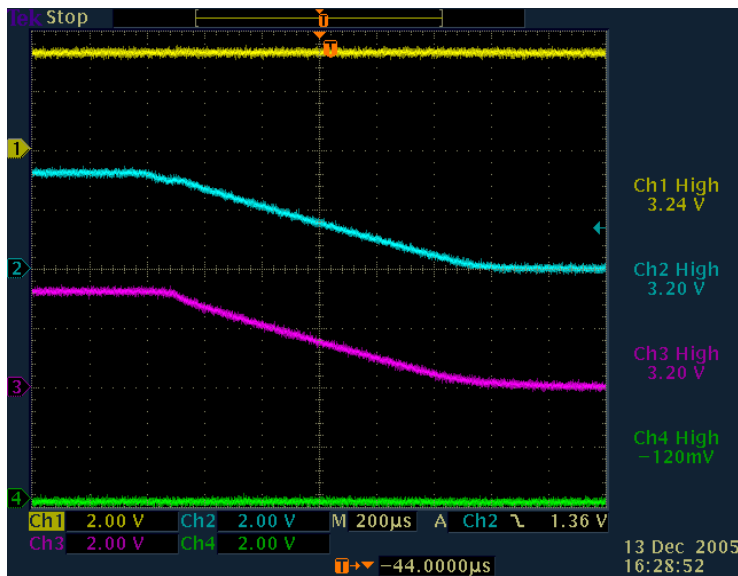


Figure 15. V_{CCINT} Is Steady at 3.3 V, V_{CCIO} Ramps Down, Output Pins Without External Resistors

V_{CCINT} and V_{CCIO} Ramp Up Simultaneously

Figures 16 to 18 show the voltage levels of a high-driving output pin and a low-driving output pin with either an external pull-up resistor, an external pull-down resistor, or without external resistors, when both V_{CCINT} and V_{CCIO} ramp up simultaneously from 0 V to 3.3 V.

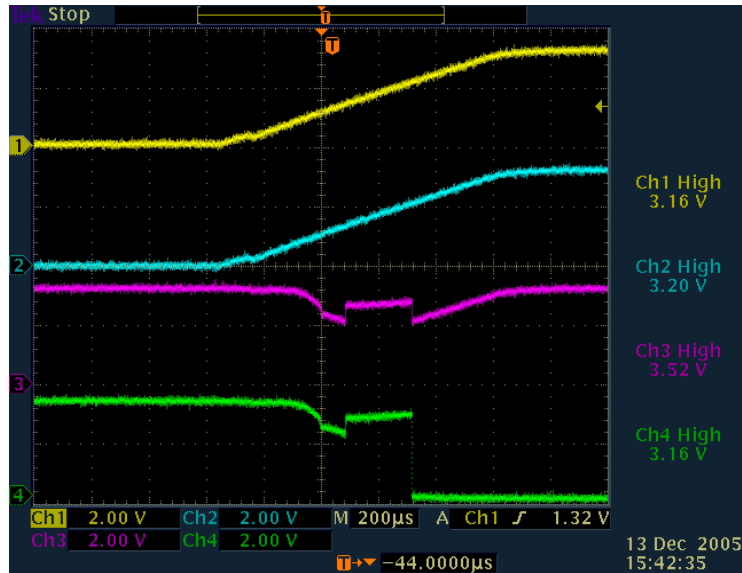


Figure 16. V_{CCINT} and V_{CCIO} Ramp Up Simultaneously, Output Pins With External 10-k Ω Pull-Up Resistor

The step shown in the middle of channels 3 and 4 for Figure 16 is the time when the internal weak pull-up resistor pulls the pins to V_{CCIO} while the external pull-up resistor pulls the pins to 3.3 V.

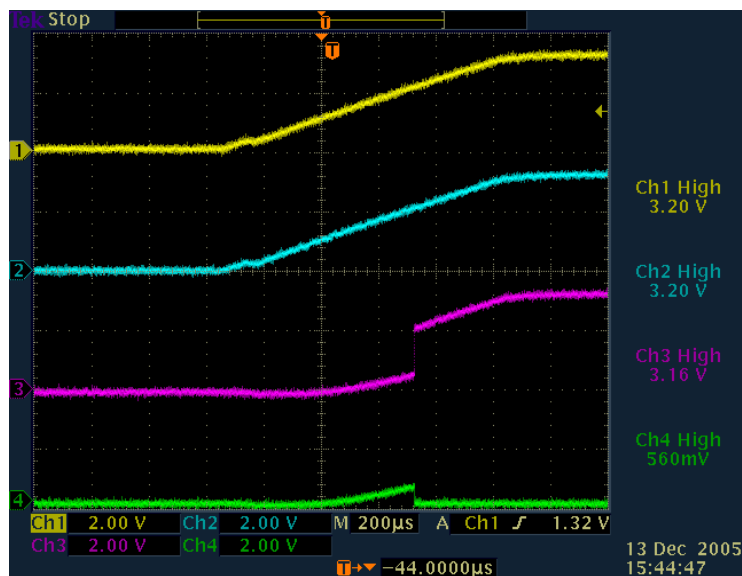


Figure 17. V_{CCINT} and V_{CCIO} Ramp Up Simultaneously, Output Pins With External 10-k Ω Pull-Down Resistor

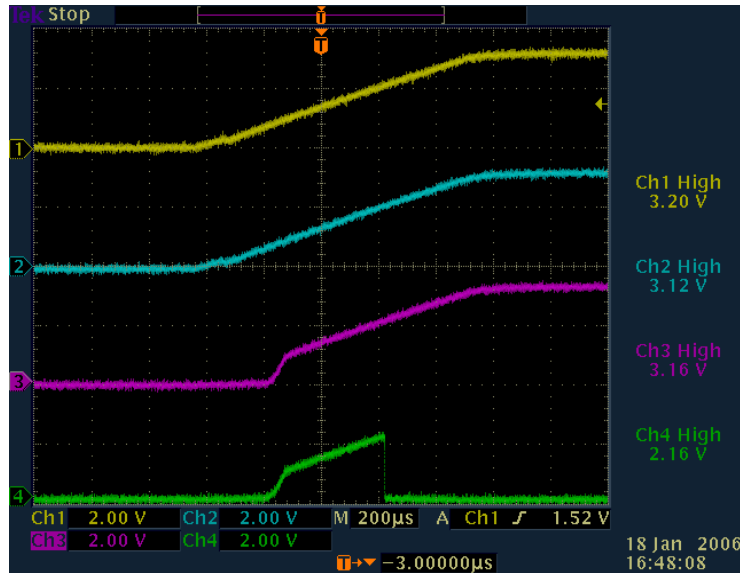


Figure 18. V_{CCINT} and V_{CCIO} Ramp Up Simultaneously, Output Pins Without External Resistors

The quick ramp on channels 3 and 4 in Figure 18 shows the internal weak pull-up resistor has just turned on and the pins are pulled quickly to V_{CCIO} , before slowly rising in voltage with the V_{CCIO} ramp.

V_{CCINT} and V_{CCIO} Ramp Down Simultaneously

Figures 19 to 21 show the voltage levels of a high-driving output pin and a low-driving output pin with either an external pull-up resistor, an external pull-down resistor, or without external resistors, when both V_{CCINT} and V_{CCIO} simultaneously ramp down from 3.3 V to 0 V.

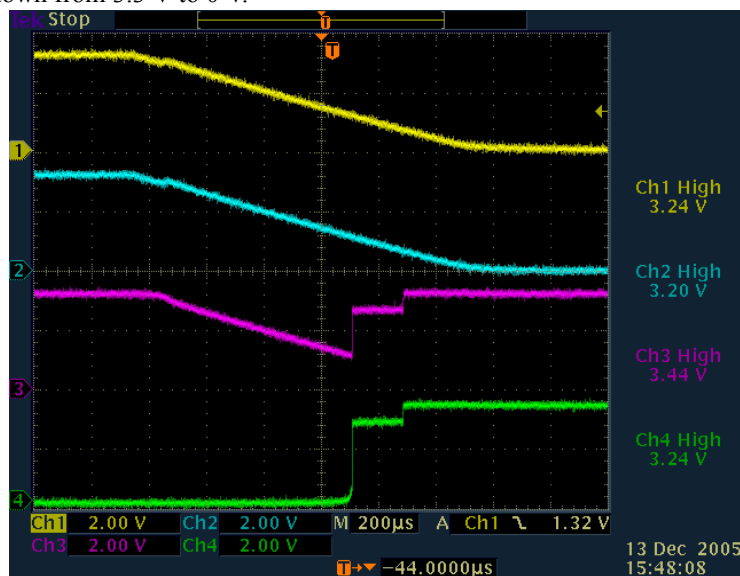


Figure 19. V_{CCINT} and V_{CCIO} Simultaneously Ramp Down, Output Pins With External 10-k Ω Pull-Up Resistor

The step in the middle of channels 3 and 4 in Figure 19 is the time when the internal weak pull-up resistor pulls the pins to V_{CCIO} while the external pull-up resistor pulls the pins to 3.3 V.

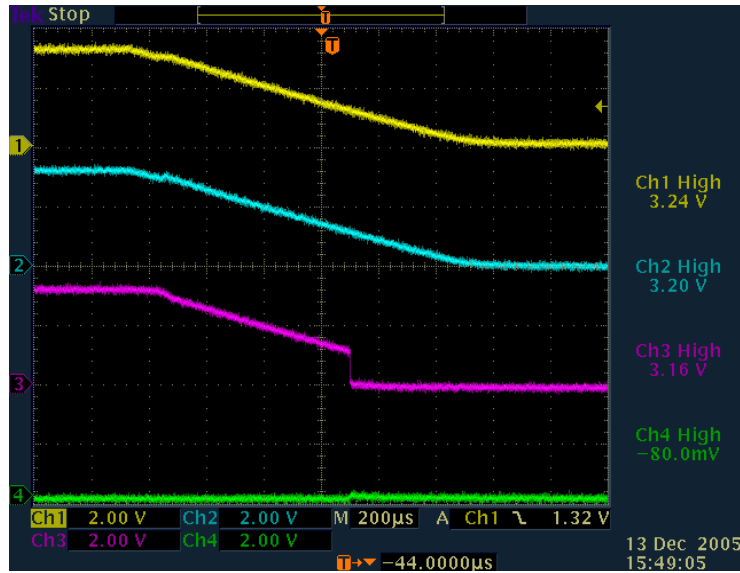


Figure 20. V_{CCINT} and V_{CCIO} Ramp Down Simultaneously, Output Pins With External 10-k Ω Pull-Down Resistor

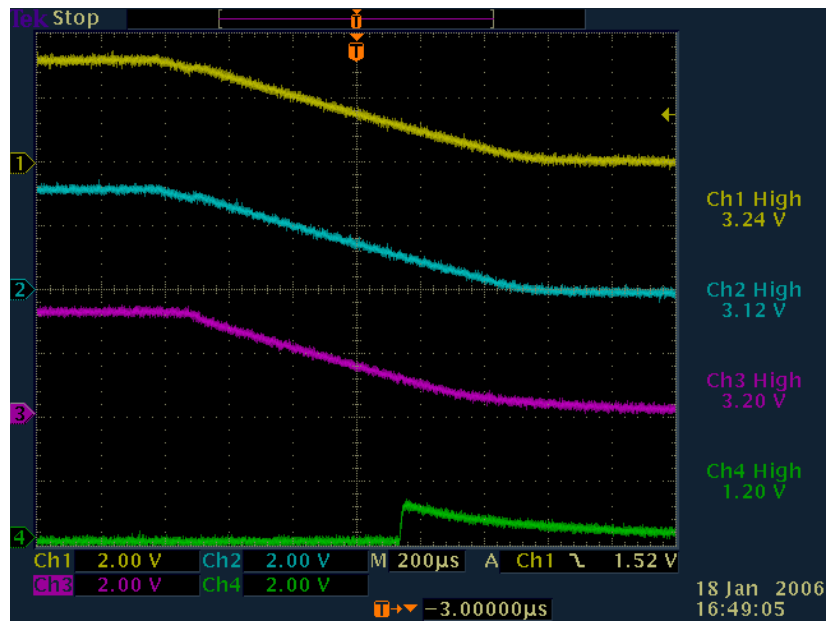


Figure 21. V_{CCINT} and V_{CCIO} Ramp Down Simultaneously, Output Pins Without External Resistors

Input Pin I/V Curve: Test Setup

This test shows the I/O leakage current of an input pin. Figure 4 shows the test setup for obtaining the I/V curve of the input pin using a curve tracer. The curve tracer varies the voltage to the input pin and measures the current sink by the pin. Different V_{CCINT} and V_{CCIO} combinations are used for this test.

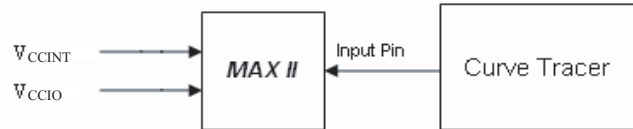



Figure 22. Obtaining the Input Pin I/V Curve

Input Pin I/V Curve: Test Results

Figures 23 to 26 show the I/O leakage current of an input pin with different V_{CCINT} and V_{CCIO} values. Figures 23, 24, and 26 show there is no detectable leakage current at the input pin while Figure 25 shows the input pin does not sink more than the maximum hot-socketing current of 300 μ A specified in the device handbook.

 Figures 23 to 25 represent the normal I/O pin I/V curve behavior, as well.

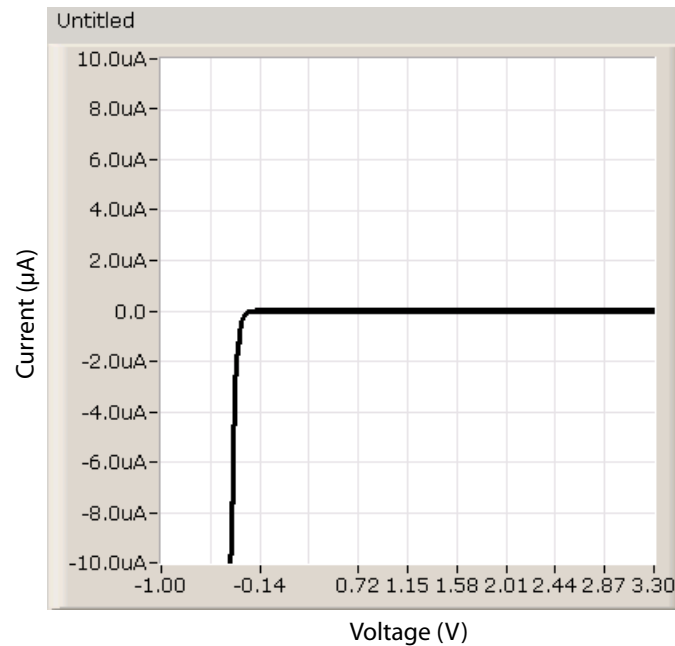


Figure 23. V_{CCINT} and V_{CCIO} 0 V

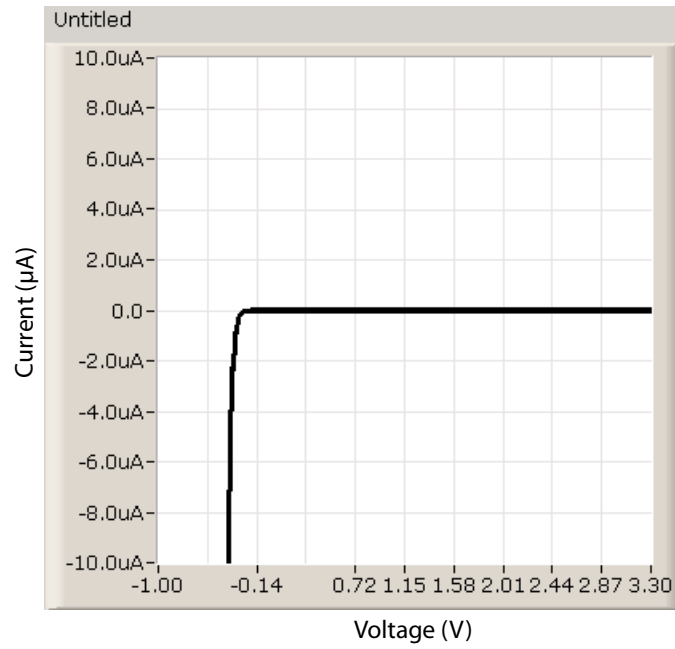


Figure 24. $V_{CCINT} 0V$, $V_{CCIO} 3.3V$

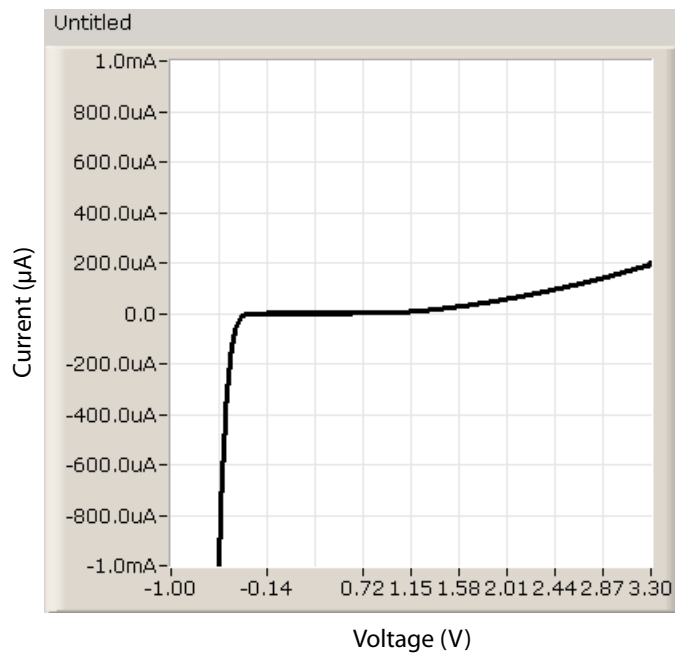


Figure 25. $V_{CCINT} 3.3V$, $V_{CCIO} 0V$

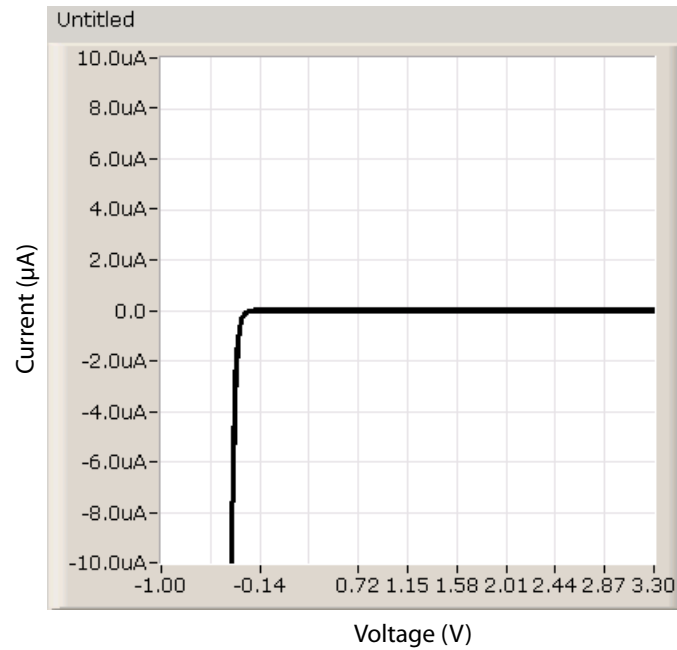


Figure 26. V_{CCINT} and V_{CCIO} 3.3 V

Conclusion

The MAX II device is designed and fully tested to support hot-socketing and different power-up sequences. With this feature, the MAX II device offers the flexibility to designers using the device in a multi-device system. The MAX II device does not effect the system during power up or power down, and additionally, is as able to tolerate different V_{CCINT} and V_{CCIO} power-up sequences.



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