White Paper

Voltage Regulator Selection for FPGAs

Introduction

As FPGAs increase in sophistication to provide additional features such as phase-locked loops (PLLs), memory interfaces, and transceiver functionality, the power requirements and designs for FPGAs are becoming more challenging. These include multiple power rails for specialty blocks and circuitry, multiple voltage levels, and increased current requirements. This paper discusses how to identify the various rails associated with Altera® devices, analyze the power requirements, and select the appropriate voltage regulator modules, then walks through a design example for a Stratix® IV FPGA.

FPGA Voltage Rails

As a first step in determining regulator selection, all of the voltage rails that the FPGA needs must be identified. These voltages are available via a pin list (commonly provided by the FPGA vendor), which identifies every power pin, provides definitions of each type, and specifies the required voltage levels. Figure 1 shows a sample pin list for a Stratix IV GX device.

Figure 1. Stratix IV GX Pin Table Excerpt

Pin Information for the Stratix® IV GX EP4SGX230 Device
Version 0.0
Notes (1), (2)

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Supply and Reference Pins
VCC	Power	VCC supplies power to the core and periphery. Connect to 0.9V.
VCCIO[1..8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V),3.0V PCI/PCI-X and LVTTL 3.3V I/O standards.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 2.5V, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 0.9V, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology. Connect to 1.5V.
VCCAUX	Power	Auxiliary supply for the programmable power technology. Connect to 2.5V.
VCCPGM	Power	Configuration pins power supply. Can be connected to1.8V, 2.5V or 3.0V depending on the particular design.

This example only identifies a few of the FPGA voltage rails. There are a number of different voltages an FPGA may need to operate, including:

- Core voltage, at which the internal logic array operates
- I/O voltages, which drive the I/O buffers. The I/O pins can support a range of voltages. The I/Os are grouped in banks, each of which can operate at a different voltage. I/O reference voltages are generated from the I/O voltage.
- PLL voltages, which power the analog and digital circuitry for the PLLs located in the core
- Transceiver voltages, which power the digital and analog circuitry of the transceiver, receiver, and transmitter paths, and transceiver I/O buffers

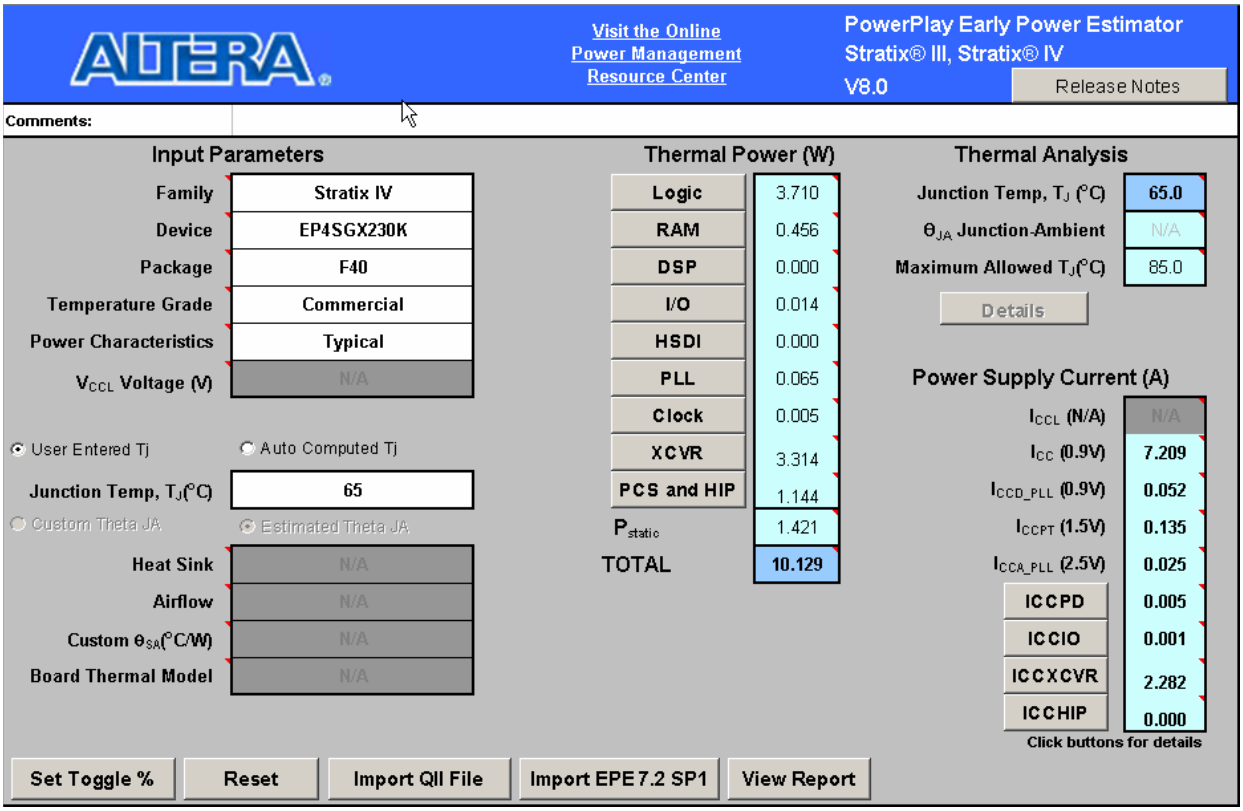
Voltage Rail Requirements

There are various parameters to take into consideration when selecting a voltage regulator. The current consumption requirement is the most important and should be considered first, followed by shared and isolated voltage rails, then regulator accuracy and ripple specifications.

Current Consumption

Before a regulator can be selected, the total current requirement must be known for that voltage rail. In an FPGA, a power calculator can be used to estimate the current draw of a specific voltage rail as well as for all voltage rails. Altera provides the customer with an Early Power Estimator (EPE), shown in Figure 2, for many of its devices. Each power rail of the FPGA can be calculated from this estimator. Add the current values of the shared rails to estimate the total current for that particular rail.

Figure 2. Stratix IV GX EPE—Main Page



For more information on the EPE, refer to the *PowerPlay Early Power Estimator User Guide for Stratix III and Stratix IV FPGAs*.

To get an even more accurate number, use Quartus® II software's PowerPlay Power Analyzer. This requires a reference design that represents the actual design to be implemented.

Shared/Isolated Voltage Rails

Special attention should be paid for the analog power rails for both the FPGA fabric and transceiver circuits. These power rails provide power to noise-sensitive circuits such as PLLs, and can affect the performance of the device in terms of jitter generation and PLL functionality.

For recommendations on which rails must be isolated and which regulator to use, refer to the Stratix IV GX Pin Out Files and Pin Connection Guidelines.

Table 1 identifies the voltage rails of a Stratix IV GX FPGA. A brief description is provided and the Share/Isolate column is representative of the recommendations given in the pin connection guidelines.

Table 1. Stratix IV GX Voltage Rails

Type	Voltage Value	Voltage Name	Description	Share/Isolate
FPGA voltages	0.9V	VCC	FPGA core power	Share
	0.9V	VCCD_PLL	PLL digital power	Share/isolate
	1.2V-3.0V	VCCIO	I/O supply voltage, banks 1-8	Share
	½ VCCIO	VREF	Input reference voltage banks 1-8	Share
	1.5V	VCCPT	Programmable power technology	Share/isolate
	1.8V/2.5V/3.0V	VCCPGM	Configuration pin power	Share
	2.5V	VCCCLKIN	Differential clock input power	Share
	2.5V	VCCA_PLL	PLL analog power	Share/isolate
	2.5V	VCCAUX	Auxiliary power	Share/isolate
	2.5V	VCCBAT	Battery back up, connect to battery	Isolate
	2.5V/3.0V	VCCPD	I/O pre-driver power	Share
Transceiver voltages	0.9V	VCCHIP	Transceiver hard IP digital power	Share
	1.1V	VCCR	Transceiver receiver analog power	Share/isolate
	1.1V	VCCT	Transceiver transmitter analog power	Share/isolate
	1.1V	VCCL_GXB	Transceiver clock power	Share/isolate
	1.4V/1.5V	VCCH_GXB	Transceiver transmit output buffer power	Share/isolate
	2.5V/3.0V	VCCA	Transceiver high voltage power	Share/isolate

Accuracy and Ripple

The voltage rails of an FPGA can only tolerate voltage swings in an allowable range as specified by the manufacturer. These parameters can be found in the *Stratix IV Device Handbook* Volume 4, Section 1, Chapter 1: *DC and Switching Characteristics* in the "Recommended Operating Conditions" section. The voltage regulator must be able to provide a constant DC-level voltage within a specified range. The load regulation specification gives the range (usually in mV) within which the voltage regulator output may deviate for changes in the load. The voltage regulator can only perform load regulation within the bandwidth (usually several 10s of KHz) of the regulation loop. Frequencies above 100 KHz require the load regulation to be managed by the decoupling capacitance. A typical specification for load regulation is ±5mV (switching regulator); this translates to 0.4 percent of a 1.2V supply. Some manufacturer's load regulation specs may be much higher.

Ripple is the alternating current component associated with switching regulators. The rise time of the switching circuitry is the main cause of the noise in switching regulators. Ripple performance depends heavily on the selection of decoupling capacitors and how well the power is filtered before reaching the decoupling capacitors. Voltage regulators specify their output ripple voltage level in mV(pk-pk). Most regulators have a ripple specification of 2 percent or better of the output voltage. When designing with an FPGA having voltage rails at 1.1V, and 0.9V, the 2 percent ripple level falls within specifications for the Stratix IV GX device.

Note that the combination of ripple voltage and load variation may add up to violate the specification of the FPGA voltage rail. These variances must be accounted for ahead of time in the selection of a voltage regulator.

Voltage Regulator Selection

When deciding on the type of regulator to use, there are two broad categories to choose from: linear regulators and switching regulators. Designers should be aware of the general advantages and disadvantages of each type of regulator in order to make the best selection for the required application. Some common advantages of the linear regulator are:

- Low output noise
- Fast response to output disturbances

- Low cost at lower power levels
- Less board area requirement
- Easy to use

Likewise, some advantages of switching regulators are:

- High power with higher efficiency
- Ability to provide a higher or lower output voltage (step-up/step-down)
- Lower cost at higher power levels

Because linear regulators have the advantage of providing very clean output power with faster response times at low power levels with lower cost, they are the ideal regulator choice for the FPGA analog and transceiver supply rails, where any noise can directly affect jitter performance. Additionally, linear regulators have the benefit of requiring less board real estate and are simpler to implement, as they require few external components.

Switching regulators typically are used for higher power applications where higher efficiencies are paramount to noise sensitivity. This makes the switching regulator ideally suited for digital core logic and I/O power, where current requirements can easily run from a few amps to tens of amps. Despite the efficiency advantage of switching regulators, they are usually more complicated to use and require more board space due to the external components required, such as power FETs and inductors. However, recent technology has been able to mitigate this concern by integrating most of the external circuitry requirements into the switching regulator module, thus significantly reducing board space. This integration has led to the availability of very small form factor, high efficiency, and high power regulators that are very cost effective.

FPGA Voltage Rail Design Example

The following sections demonstrate the process of determining the regulator type for a particular voltage rail of an FPGA board design. The design example targets the Stratix IV GX device (EP4SGX230KF40C), which consists of a high-density FPGA fabric with six high-speed transceiver blocks. The purpose of this board is to verify the performance of the high-speed transceivers. The voltage rail chosen for this example is the core voltage (VCC) at 0.9V.

Overview

The core activity consists of pattern generator circuits, and gray-code counters operating at multiple frequencies, all in an effort to generate core noise. One pattern generator module is linked to channels of the transceiver module, while one transceiver channel is routed out for measurement purposes. The voltage rail in this example is the core voltage of 0.9V. With the core utilization tested at 80 percent, the current consumption for this voltage rail can now be calculated.

Current Consumption

To calculate the current required for the VCC plane, the PowerPlay EPE is used. The areas of concern in the calculator pertaining to the core voltage are the logic, RAM, PLL, and clock sections. These sections incorporate enough usage to mimic a typical design. Listed below is the pertinent information required for the calculator on the main page.

Family	Stratix IV
Device	EP4SGX230K
Package	F40
Temperature Grade	Commercial
Power Characteristics	Typical
User Entered T_j	
Ambient Temp, T_A (°C)	65

Logic Usage

The logic usage section identifies the number of adaptive look-up tables (ALUTs) and flipflops. The *Stratix IV Device Handbook* provides the adaptive logic module (ALM) count; in this case, the total count is 91,200.

1 ALM = 2 ALUTs and 2 flipflops
(2) x (91200) = 182,400 ALUTs
= 182,400 flipflops
@ 80% core usage = 145,920 ALUTs
= 145,920 flipflops
@ 150-MHz clock frequency
@ 25% toggle percentage
@ 3 average fanout

With the above parameters entered into the calculator, the resulting estimated power for logic usage is 3.71W.

RAM Usage

The RAM usage section identifies the number of RAM blocks used in this design. Three memory types can be provided: the MLABs in this example are unused, the M9K block takes up 10 percent of the memory space, and the M144K block takes up 45 percent. Both ports A and B are used.

M9K Block:	**M144K Block:**
RAM blocks = 125	RAM blocks = 10
Data width = 16	Data width = 16
RAM depth = 512	RAM depth = 8000
RAM mode = dual port	RAM mode = dual port
Clock frequency = 600 MHz	Clock frequency = 600 MHz
Enable % = 25%	Enable % = 25%
Write % = 50%	Write % = 50%

With the above parameters entered into the calculator, the estimated power for RAM usage is 0.456W.

PLL Usage

The PLL usage section identifies the number of PLLs utilized. For this example, two PLL modules are instantiated.

PLL type = LVDS
PLL blocks = 2
DPA buses = 1
Output frequency = 150 MHz
VCO frequency = 700 MHz

With the above parameters entered into the calculator, the estimated power for PLL usage is 0.065W.

Clock Usage

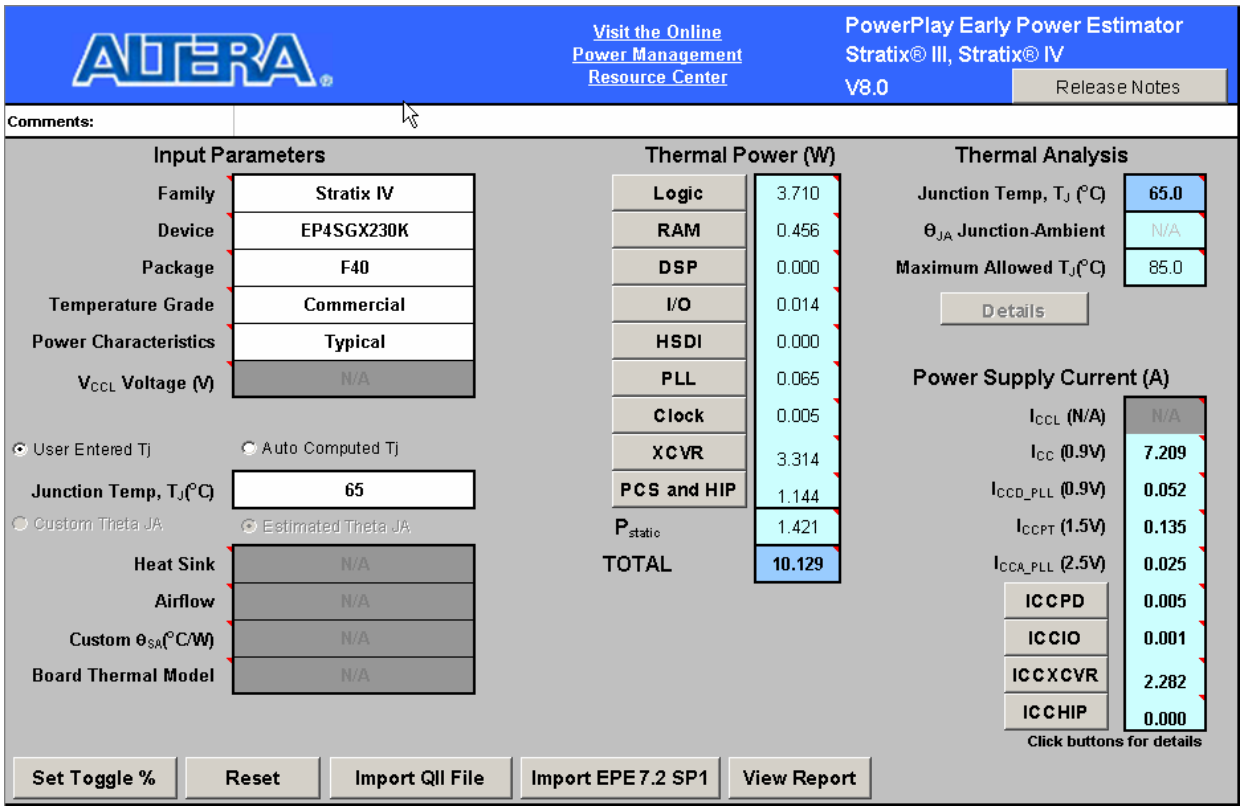
The clock usage section identifies the number of clocks required for this design. In this example, two clocks are called out, each of which has a fanout of five.

Clock frequency = 150 MHz
Fanout = 5
Global enable % = 100%
Local enable % = 50%

With the above parameters entered into the calculator, the estimated power for clocks usage is 0.005W.

The total current required for the VCC is estimated at 7.209A. Figure 3 shows the main page of the PowerPlay EPE. Note that the I_{CC} under "Power Supply Current (A)" is the core current, while the total current required for the PLL (VCCD) shows $I_{CCD-PLL}$ at 0.052A. The total current required for this voltage is 7.261A.

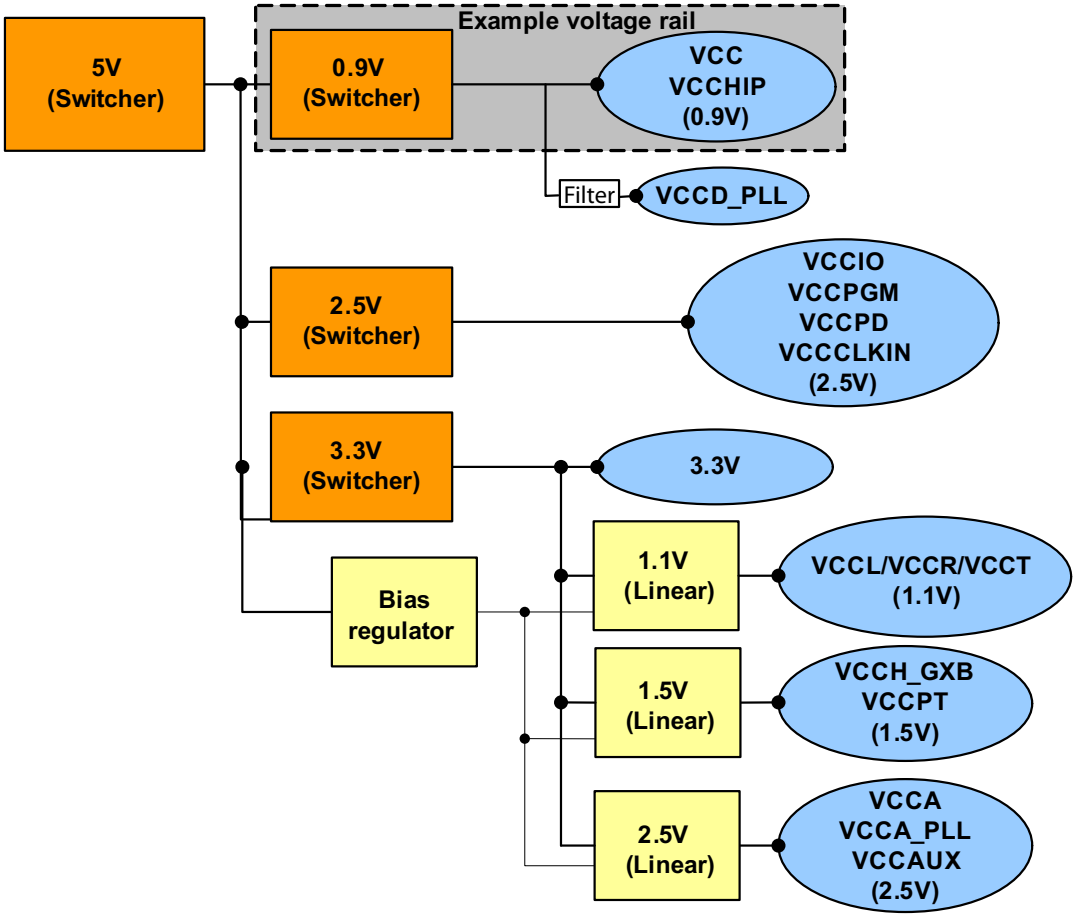
Figure 3. Stratix IV GX EPE—Main Page



Power Tree

The VCC voltage rail is one of the primary power rails for an FPGA. The power tree example shown in Figure 4 is the setup for a board design to target a PCI Express Gen1 card at 2.5 Gbps. This diagram shows how the VCC voltage rail—highlighted in gray—fits into the entire power network. Each blue oval represents a unique voltage plane. Each voltage rail must have its current calculated. When using a linear regulator, the dropout current must be calculated along with the current of that voltage plane. The linear regulator driving that voltage plane must have the current capability to handle the current draw of that plane. The regulator that drives the linear regulator must be able to handle the dropout of the linear regulator in addition to any other requirements on that regulator. In this case, the 3.3V switching regulator must be able to handle the dropout voltages of the six linear regulators it is driving, while also providing current to the 3.3V plane.

Figure 4. Stratix IV GX Power Tree



Voltage Regulator Selection

The example voltage plane, which powers the core logic (VCC), digital power for the PLLs (VCCD_PLL), and the hard intellectual property (IP) block (VCCHIP), uses a switching mode power supply due to its large current requirement. This voltage plane requires a current of 7.209A, and is assigned a 10A switching regulator, which provides a guard band of 40 percent on top of the estimated current draw.

Conclusion

Due to the number of voltage rails associated with an FPGA, the trade-offs between isolation versus quantity and noise versus performance must be weighed when selecting voltage regulators for a particular design. Many parameters are involved when selecting a voltage regulator; knowing which parameters are more important than others can be the difference between a successful, efficient design versus a costly, marginal design.

References

- *Stratix IV GX Handbook* and Literature:
  www.altera.com/literature/lit-stratix-iv.jsp
- Stratix IV GX Pin Out Files and Pin Connection Guidelines:
  www.altera.com/literature/lit-dpcg.jsp
- Stratix IV GX PowerPlay Early Power Estimators (EPEs) and PowerAnalyzer:
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- *PowerPlay Early Power Estimator User Guide for Stratix III and Stratix IV FPGAs:*
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- Quartus II software's PowerPlay Power Analyzer:
  www.altera.com/products/software/quartus-ii/subscription-edition/qts-se-index.html

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