Designing Home Appliances With FPGAs

Introduction

The efficient use of electricity enables home appliances to minimize cost and preserve the environment. Most home appliances, such as refrigerators, washers and dryers, dishwashers, and air conditioners, are driven by electric motor systems. These systems include a power supply, an electric motor, motor control circuitry, and a mechanical system. Various methods are used to improve the system efficiency:

- Maintain voltage level
- Minimize phase imbalance
- Maintain power factor
- Maintain good power quality
- Use adjustable speed drives or two-speed motors
- Control temperature
- Match motor operating speed

System costs and power consumption can be drastically reduced by using digital circuits, or FPGAs, to control an analog motor circuit. Besides energy conservation, FPGAs also incorporate features such as embedded digital signal processing (DSP) blocks, microcontrollers, and I/O interfaces to complete a home appliance design.

Pulse Width Modulation

One of the typical methods for digitally controlling analog motor circuitry is to use pulse width modulation (PWM). With PWM, the time period of the square wave is constant, and T_{ON}, the time of the signal remaining high, is varied or modulated. The duty cycle and average DC value of the signal can thus be varied. With help from the digital system, PWM is a powerful way to control analog circuits. Figure 1 shows an example of the "on" time of a digital pulse.

Figure 1. PWM Waveform Example
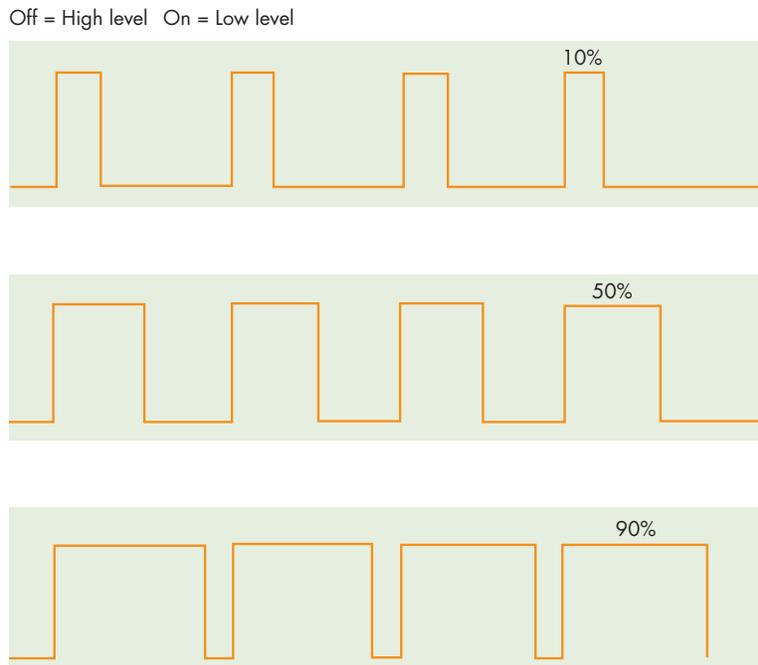
Application examples include voltage regulation, where the output voltage can be controlled to a desired level by varying the duty cycle. Another example is power delivery, where the average power delivered is a function of the modulated duty cycle. Depending on how it is to be used, PWM can be implemented using an Altera® MAX® II CPLD for simple voltage regulation or with a Cyclone® III FPGA for complex control algorithms using its internal DSP blocks.

Figure 2 shows the basic block diagram with PWM, and Figure 3 shows the output of the modulation driving an analog motor interface circuit. The UP and DOWN input signals are used to vary the duty cycle of the output signal, and can be generated by a microcontroller. The first module generates two clocks of different frequencies using the internal UFM oscillator available in all MAX II devices. The 4-bit output signal from this module, DUTY_CYCLE, is incremented or decremented, depending on whether UP or DOWN is asserted. The second 4-bit output signal, COUNT, is incremented continuously at the higher clock frequency generated in the first module. This signal is compared to DUTY_CYCLE at the same frequency in the second module. The result of the comparison is a single bit assigned to the final output signal PWM. The signal DUTY_CYCLE, being a 4-bit variable, allows 16 different variations in the duty cycle of the output signal. In this design implementation, input UP is given a higher priority over DOWN. Therefore, if both are high at the same time, the output signal sees an increase in its duty cycle.

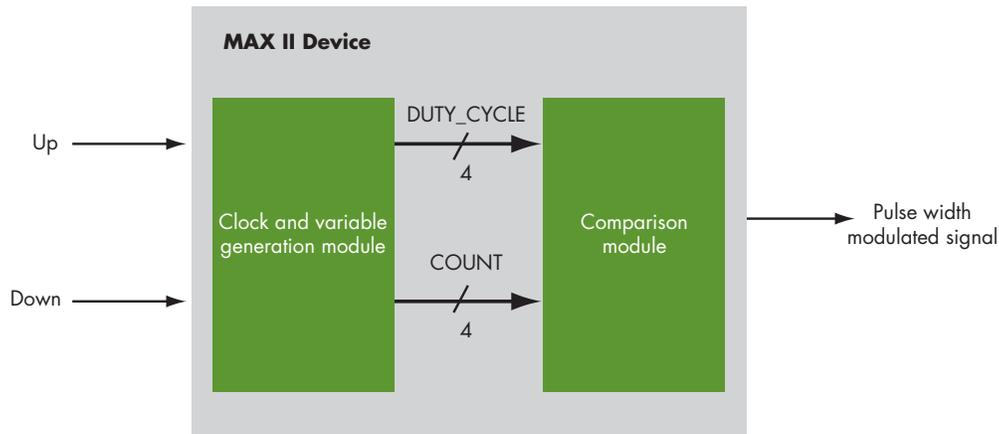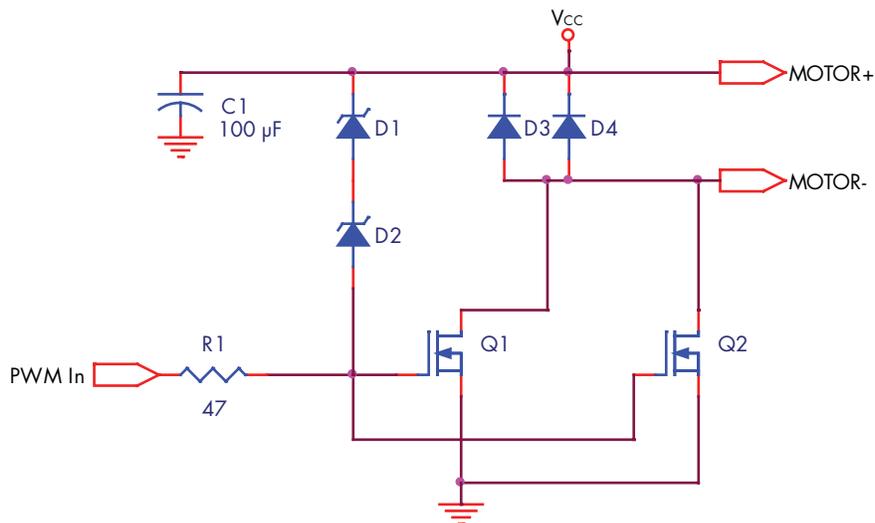*Figure 2. PWM Basic Block Diagram*

Figure 3. Motor Analog Drive Circuit

DSP Motor Control

Embedded DSP blocks (Figure 4) inside Cyclone III FPGAs provide the key elements to design a more complex and more energy-efficient motor control system. FPGA-based DSP ICs enable white goods manufacturers to reduce development time and cost, as well as future-proof their designs without needing to lay out new circuit boards. FPGAs provide a reconfigurable solution for implementing DSP applications as well as the necessarily higher DSP throughput. Since FPGAs can be reconfigured in hardware, FPGAs offer complete hardware customization while implementing complex motor control DSP functions. Therefore, DSP systems implemented in FPGAs can have customized architecture, customized bus structure, customized memory, customized hardware accelerator blocks, and a variable number of multiplier-accumulator (MAC) blocks.

Figure 4. Embedded DSP Block Inside a Cyclone III FPGA
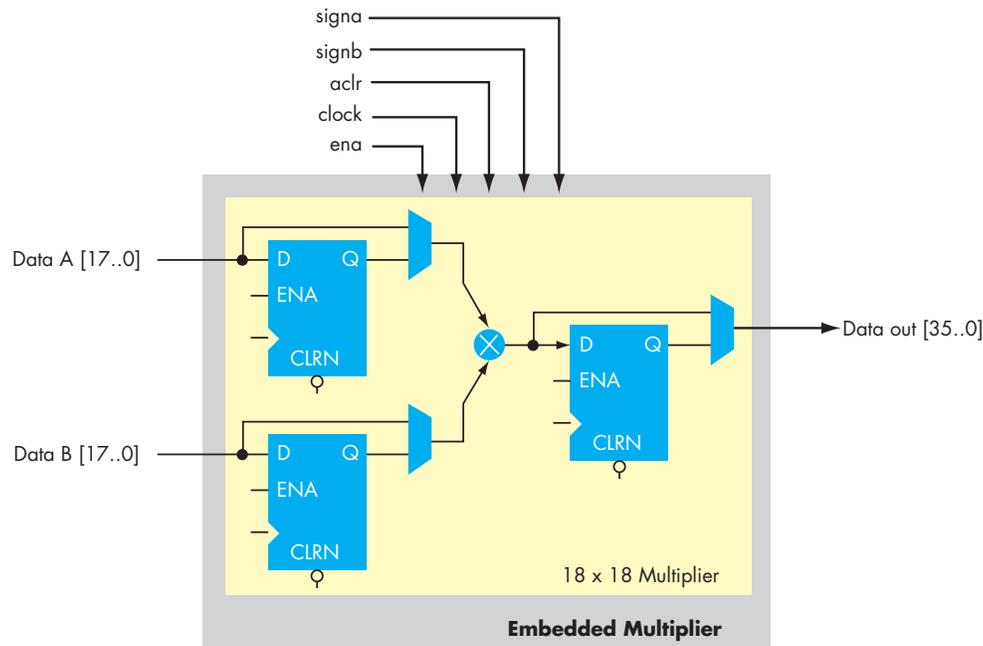
To run the AC motor efficiently, it is essential that the position of the internal permanent magnet synchronizes with the frequency of applied AC voltage. Sensors are used to detect the location of the magnetic rotor and adjust the frequency of the voltage accordingly. This is a method similar to a servo control phase-locked loop (PLL) system, but using DSP to accomplish the task.

The next generation of home appliances will require more complex circuitry to monitor the health of the motor and the overall appliance. The advanced control algorithm design using the Cyclone III FPGA's DSP features enables a more flexible system than ASSPs and ASICs do. Since the FPGA is programmable, new features may be added or modified as market requirements shift. By adding an Ethernet intellectual property (IP) core, the FPGA will also be able to communicate via an Internet protocol network, allowing the system to schedule maintenance and service before the system breaks down, as well as enabling wireless communication design to the user's home network.

Microcontroller

The next-generation home appliance will have a microcontroller for user interface and other functional controls. An FPGA with an embedded microcontroller offers an integrated solution without needing another external dedicated processor. A major challenge facing the embedded processor designer is selecting a processor that best fits the applications without overspending for performance or sacrificing features. Altera's Nios® II soft processor allows the designer to create the needed perfect fit of hardware (CPUs, peripherals, custom hardware accelerators), software (memory interfaces), and cost to meet the unique demands of every new home appliance design cycle.

In addition, Altera's Nios II C-to-Hardware Acceleration (C2H) Compiler allows engineers who are new to FPGA design to use ANSI C language instead of schematics or RLT entry to design the embedded processor system.

LCD Panel Interface

The built-in LVDS I/O interface of the FPGA allows direct coupling to drive either a simple text or video-quality display panel, so a video processor and timing controller for the display can be easily designed into the system. The Cyclone III FPGA can be designed and configured as an image enhancement engine that drives a typical liquid crystal display (LCD) interface. Pre-optimized IP MegaCore® functions, such as the Video Image Processing (VIP) Suite with its de-interlacers, scalers, filters, and color space converter, can process video input from any source and output to a LCD panel such as the video display on a network-enabled refrigerator.

Summary

Low-cost FPGAs and CPLDs can help home appliance designers implement energy-saving motor control by using a flexible and integrated single-chip solution with a DSP algorithm. In addition, the Cyclone III device's internal Nios II soft processor helps to facilitate an appliance's user interface. Altera devices also allow appliances to communicate wirelessly with the customer's home network, and other built-in features such as LVDS I/Os can be used to drive the LCD display panel.

Further Information

- Altera's Video and Image Processing Suite MegaCore Functions:
  www.altera.com/products/ip/dsp/image_video_processing/m-alt-vipsuite.html
- DSP Tools:
  www.altera.com/products/software/products/dsp/dsp-builder.html
- Cyclone III in Display Application:
  www.altera.com/products/devices/cyclone3/mkts-apps/cy3-mkts-display.html
- Embedded FPGA Processor:
  www.altera.com/products/ip/processors/nios2/ni2-index.html
- C2H Complier:
  www.altera.com/products/ip/processors/nios2/tools/c2h/ni2-c2h.html

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