PRODUCT BRIEF

Intel® Stratix® 10 DX FPGA Family
Product Brief

Enabling UPI and PCIe* Gen4 Accelerators

FPGAs Accelerate Selected Intel® Xeon® Scalable Processors, ASIC, or ASSPs via High-Bandwidth and Coherent Interfaces

Boost your server or embedded system performance with Intel® Stratix® 10 DX FPGAs when combined with selected Intel Xeon® Scalable Processors and Intel Optane™ DC persistent memory DIMMs, or other compatible CPUs, ASICs, or ASSP devices.

Technology Leadership Extends to Intel Coherent Interfaces

Innovation and technology leadership helps Intel maintain its position as one of the top semiconductor company worldwide1. By using the Intel Ultra Path Interconnect (UPI) chip-to-chip coherent protocol, server-based systems can exchange workloads or process/store critical information between Intel FPGAs and selected Intel Xeon Scalable Processors much faster.

- 37% lower latency vs. PCI Express* (PCIe*) protocol†
- 2.6X more bandwidth vs. PCIe only interfaces†

When using the UPI interface for memory expansion, the Intel CPUs can access additional memory attached to the Intel FPGA, increasing the total memory available for processing any workload.

- Expanded memory is addressable by the Intel CPU, host operating system, or any virtual machines running on the host
- Memory transactions are simple, without needing PCIe drivers or DMA transfers.
- Access to selected Intel FPGA available memories: on-die SRAM, in-package HBM2 DRAM stacks2, external DDR4 or selected Intel Optane DC Persistent Memory DIMMs or non-volatile SSDs, and so on

With a migration path from UPI to next generation industry standard Compute Express Link* (CXL) coherent accelerator, count on additional performance and more innovation helping your system accomplish bigger and better things in the future.

Industry Standard Performance

Intel Stratix 10 DX FPGAs deliver awesome PCI Express Gen4, x16 performance for interfacing to any PCI-SIG* compliant device for increased levels of data throughput. Take advantage of the FPGAs new virtualization features for easier integration with cloud managed services.

- SR-IOV with eight physical functions and 2,048 virtual functions
- VirtIO, shared virtual memory, scalable-IOV

Increase Server TCO with FPGA Accelerators

FPGAs are silicon devices that can be dynamically reprogrammed with a datapath that exactly matches your workloads, such as:

- Database analytics queries
- In-memory database delta merge and index recoding
- Image inference
- Storage encryption/decryption and/or compression/ decompression
- RCP or zero-copy acceleration
- FPGA-as-a-Service

This versatility enables the provisioning of a faster processing, more power efficient, and lower latency service – lowering total cost of ownership (TCO), and maximizing compute capacity within the power, space, and cooling constraints of data centers.

Embedded Systems Adopt PCI Express

High-performance embedded systems have long utilized FPGAs for their ability to bridge between different chipsets using industry standard interfaces based on general purpose I/O (or transceiver I/Os) combined with customized state machines. Ethernet is commonly used for peer-to-peer communication within embedded systems. As the need to handle increasingly large amounts of data (i.e. industrial image processing for smart factories) pushes up the performance requirements for embedded system, PCIe has migrated from use within computing systems (PCs and servers) into the embedded segment. Intel Stratix 10 DX FPGAs provide multiple, high-performance PCIe and Ethernet ports to satisfy the most demanding embedded system requirements.

Where to Get More Information

For more information, visit www.intel.com/stratix10

INTEL® STRATIX 10 DX DEVICE FAMILY FEATURES AT A GLANCE

FEATURES	BENEFITS
Intel® Ultra Path Interconnect hard and soft intellectual property (IP) blocks	Verified CPU + FPGA solution (selected Intel Xeon® Scalable Processors) to provide a platform with a low latency, cache coherent, or memory expanded capacity to accelerate critical functions.
PCI Express Gen4 hard IP blocks	Seamlessly connect to selected Intel Xeon Scalable Processors or other CPUs, ASICs, and ASSPs with fully compliant x16 lane PHY and controller IP implemented ASIC-style to minimize FPGA logic used.
SR-IOV, Scalable IOV, Shared Virtual Memory, VirtIO	Mix and match these virtualization IP features to enable easier FPGA control with cloud management software.
Intel Optane™ DC persistent memory DIMM	Get high-density, high-performance, and non-volatile memory capability all within existing DDR4 DIMM sockets when using Intel FPGA Optane DC Persistent Memory controller IP.
100G Ethernet	Ingest high-speed data using multiple 10/25/100 Gb Ethernet MAC ports
FPGA options[2]	HBM2 memory stacks and controller for superfast memory near the FPGA compute algorithms. Add more intelligence to your FPGA by using the quad-core A53 (1.3 GHz) subsystem with peripherals and fast internal buses to/from the FPGA fabric.
FPGA resources	1.3 – 2.8 million elements of FPGA logic resources M20K and MLAB memory blocks Multi-configuration DSP blocks General purpose I/Os and transceiver I/Os Clocks and phase-locked loops (PLLs) Memory controllers for various external memory types Secure Device Manager (bitstream encryption/authentication, PUF, boot code authentication, side channel attack protection) Multiple device programming options including partial FPGA reconfiguration

1 Gartner report Apr. 11, 2019: https://www.gartner.com/en/newsroom/press-releases/2019-04-10-gartner-says-worldwide-semiconductor-revenue-grew-12-

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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