Quartus II Software Release Notes

October 2005 **Quartus II version 5.1**

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **\altera\quartus<*version number*>** directory.

New Features & Enhancements

The Quartus II software version 5.1 includes the following new features and enhancements:

- Automated Power Optimization – The PowerPlay power analysis and optimization feature helps designers meet low-power targets.
- Bottom-Up Incremental Design Flow – This new design flow provides productivity advantages for team-based design by allowing engineers to independently develop and optimize design functions that are later integrated into the complete design.
- SOPC Builder enhancements – The SOPC Builder now comes standard with a set of embedded peripherals that were previously included only with the Nios® II development kits.
- External Logic Analyzer Interface – This new interface allows you to gain visibility of internal FPGA nodes when you are using an external logic analyzer for board-level debugging.

Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the listed devices.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Cyclone™ II	EP2C5Q208	EP2C5T144
	EP2C5F256	
	EP2C8Q208	EP2C8 T144
	EP2C8F256	
	EP2C20F256	EP2C20F484
	EP2C50F484	EP2C50F672
	EP2C35U484	EP2C50U484
	EP2C70F672	EP2C70F896
Stratix® II	EP2S130F780	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Stratix II	EP2S90F780	EP2S90H484
Stratix II GX	EP2SGX30CF780	EP2SGX30DF780
	EP2SGX60CF780	EP2SGX60DF780
	EP2SGX60EF1152	EP2SGX90EF1152
	EP2SGX90FF1508	EP2SGX130GF1508
HardCopy® II	HC210F484C	HC220F672C
	HC220F780C	HC240F1020C
	HC240F1508C	

Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
None	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device
HardCopy II	HC210
	HC220
	HC230
	HC240
Cyclone II	EP2C5*
	EP2C8*
	EP2C20*
	EP2C35*
	EP2C50*
	EP2C70*

* These devices had significant changes to their timing models in the version 4.2 release of the Quartus II software. You should run the Timing Analyzer on your design to see any effects of these changes.

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
FLEX 10K®	All	3.0
FLEX 10KA	All	3.0
MAX® 7000S	All	3.0
MAX II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2240	5.0 SP1
Stratix	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix II	EP2S15*	5.0 SP1
	EP2S30*	5.0
	EP2S60*	5.0
	EP2S90*	5.0 SP1
	EP2S130*	5.0 SP1
	EP2S180	5.1
Stratix GX	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1

* The final timing models have been updated in Version 5.1 for details, see the section entitled “Changes to Stratix II Timing Models” which follows.

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX® 20K, APEX 20KE, APEX 20KC, APEX II,

Excalibur™, FLEX® 6000, and FLEX 10KE device families. Timing models for these device families became final in versions earlier than version 3.0.

Changes to Stratix II Timing Models

The timing models for Stratix II devices are updated in the Quartus II version 5.1 software. The changes affect three areas: M4K memory blocks, I/O cells, and Logic cells as described in the following paragraphs. Altera recommends that you re-run timing analysis on affected Stratix II designs with the new software. For additional details on the Stratix II timing model changes, please contact Altera Technical Service at **http://mysupport.altera.com**.

M4K Memory Block Changes

Performance reduced for dual-port dual-clock mode and packed single-port mode

- f_{MAX} reduced by 14% in affected modes compared to v5.0 SP1 model
- Unregistered output delay (t_{CO}) increased per speed grade compared to v5.0 SP1 model
  - C3 speed grade slows down by 280ps
  - C4 speed grade slows down by 322ps
  - C5 speed grade slows down by 306ps

I/O Cell Changes

Output delay capacitive load de-rating factors are adjusted for some I/O standards

- For LVTTL and LVCMOS outputs, de-rating factor increased by up to 59 ps/pF
- For HSTL and SSTL outputs, de-rating factor decreased by up to 51 ps/pF
- For LVDS outputs, de-rating factor increased by 7ps/pF

SSTL output delays changed, when On-chip Termination (OCT) is used

- Output delays reduced by up to 300ps
- Output enable/disable delay increased by up to 40ps

Minimum output delays are adjusted for row I/Os

- For LVTTL and LVCMOS outputs, the delay increased by up to 300ps
- For HSTL and SSTL outputs, the delay decreased by up to 56ps

Logic Cell Changes

Logic cell delay slowed down by 2% for EP2S130 in C3 speed grade

Changes to Stratix and Stratix GX Timing Models

The timing models for Stratix and Stratix GX are updated in the Quartus II software version 5.1. The change affects the maximum DQS delay compensation.

Maximum DQS Delay Compensation Change

Maximum DQS delay compensation is limited to the following maximum delay for each speed grade:

- 1.675ns for C5
- 1.842ns for C6
- 2.093ns for C7
- 2.407ns for C8

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix II	Preliminary
Cyclone II	Preliminary
MAX II	Final – 5.0 SP1
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Cyclone	Final – 5.1
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1

EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink® support
Mentor Graphics® LeonardoSpectrum	2005a Update 1	✓
Synopsys Design Compiler	2004.12-SP4	
Synopsys Design Compiler FPGA	2005.09	
Synopsys FPGA Compiler II	3.8	✓
Mentor Graphics Precision RTL Synthesis	2005b	✓
Synplicity Synplify and Synplify Pro	8.2.2a or later	✓
Magma Design Automation PALACE™	2.4	✓
Verification Tools	**Version**	**NativeLink support**
Cadence NC-Verilog	5.4 s011	✓
Cadence NC-VHDL	5.4 s011	✓
Cadence Verilog-XL (Windows) Cadence Verilog-XL (UNIX)	3.3 5.4	
Mentor Graphics ModelSim®	6.0e	✓
Mentor Graphics ModelSim-Altera	6.0e	✓
Mentor Graphics Tau	ISD 2004 SPac3	
Mentor Graphics IO Designer	2004 SPac2	
Synopsys PrimeTime	2005.06	✓
Synopsys VCS / VCS MX	7.2	✓
Synopsys VSS	2002.06	
Synopsys Formality	2005.09	
Cadence Encounter Conformal	5.1	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Changes to Default Settings in This Release

This section lists the variable names for Quartus II settings that have different default values in the Quartus II software version 5.1 from the previous version. The default values and a list of the changed values are stored in the **\<*Quartus II Installation directory*>\bin\assignments_defaults.qdf** file.

Setting Keyword	Default in 5.0	Default in 5.1
ANALYZE_LATCHES_AS_SYNCHRONOUS_ELEMENTS	OFF	ON
STRATIXII_MRAM_COMPATIBILITY	ON	OFF

Changes to Software Behavior

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
The following primitives now use a new library instead of the **altera_mf** library: CARRY CARRY_SUM CASCADE CLKLOCK EXP GLOBAL LUT_INPUT LUT_OUTPUT ROW_GLOBAL TRI SOFT OPNDRN DFF DFFE DFFEA JKFF JKFFE DFFEAS LATCH SRFF SRFFE TFF TFFE ALT_INBUF ALT_IOBUF ALT_OUTBUF ALT_OUTBUF_TRI .	To perform functional simulations in Verilog HDL, you must use the **altera_primitives.v** library located in the **<*Quartus II installation directory*>\eda\sim_lib** directory. For VHDL, you must use the **altera_primitives.vhd** library located in the **<*Quartus II installation directory*>\eda\sim_lib** directory. The VHDL component declaration file is located in the **altera_primitives_components.vhd** library in the **<*Quartus II installation directory*>\eda\sim_lib** directory
The frequency limit on the PLL reference clock on Stratix GX devices changed to 640 MHz.	To take advantage of the new setting, change your design and recompile after installing the Service Pack.
Designs compiled with the Quartus II software version 5.0 and earlier could fail their boundary-scan test (BST) if the test expected all input buffers to be active after device configuration. Under some circumstances, unused input buffers are disabled by the Quartus II software to minimize power usage in Stratix II, Cyclone II, and MAX II device families.	Beginning in version 5.0 Service Pack 1, the Quartus II software supports the **always_enable_input_buffers** option to prevent unused input buffers from being disabled during configuration.

Description	Workaround
The Quartus II software version 5.0 and earlier did not correctly enforce the Fitter rule that there must be one row of separation between dynamic phase alignment (DPA) channels to prevent interference.	Beginning in version 5.0 Service Pack 1, the Quartus II software gives a critical warning of this condition if the maximum data rate is between 701 MHz and 1 GHz and an error if the data rate is 1GHz and above. If you receive such warning, reassign your DPA channels to have one row of separation between them.
The Quartus II software version 5.0 and earlier incorrectly permitted the VCCIO voltage of an I/O bank that contains On-Chip Termination `RUP` and `RDN` pins to be different from the VCCIO of the associated I/O standard on Stratix II devices.	Beginning in version 5.0 Service Pack 1, the Quartus II software requires that the voltage assignments be the same. This restriction may cause designs that fit using the Quartus II software version 5.0 to not fit when compiling after installing Service Pack 1.
The **data_out[]** bus signals from the `altremote_update` megafunction are incorrectly inverted in the Quartus II software version 5.0. This condition is corrected in version 5.0 SP1.	Recompile your design after installing the Quartus II software version 5.0 Service Pack 1.
The settings for Stratix II PLLs are updated in the Quartus II software version 5.0. The changes reflect the allowable settings for the PLL resulting from device characterization.	
The Quartus II software version 5.0 SP1 no longer supports use of the **HyperTransport** I/O standard on clock inputs and outputs on Top Edge and Bottom Edge pins.	
The Quartus II software version 5.0 and later supports Comma-Separated Value files (**.csv**) for using the PowerPlay Early Power Estimation spreadsheet with Stratix II and Cyclone II devices.	
You cannot use the Quartus II stand-alone Programmer to erase devices when you are using JAM files (**.jam**) or Jam Byte Code files (**.jbc**).	

Description	Workaround
Some designs that compiled without error in the Quartus II software version 4.2 and earlier may cause an error similar to the following example to be displayed, when compiled in the Quartus II software 5.0 and later: `Error: Fast PLL DPA-mode channels span rows 2 to 28, but location assignment of LVDS DPA-mode SERDES driven by PLL altlvds_rx:altlvds_rx_component|lvds_rx_9p31:auto_generated|pll is not within 25 from driving fast PLL`	Remove your pin assignments and recompile the design with the Quartus II software version 5.0 or later.
The Quartus II software version 5.0 corrects a previous problem in which the Cyclone and Cyclone II CRC configuration oscillator was shown to run at 100 MHz rather than the 80 MHz rate correctly shown in the device family handbooks.	
In the Quartus II software version 5.0 and later, you can assign the **Allow XOR Gate Usage** logic option to individual nodes and entities. In previous versions, you could apply this logic option only to the entire design (that is, it was a global logic option).	
In the Quartus II software version 5.0 and later, if your Quartus II Settings File (**.qsf**) contains an error, you cannot compile the project until the error has been corrected. In previous versions, a warning message was displayed and compilation continued.	
In the Quartus II software version 5.0 and later, the **\altera\qdesigns<*version number*>\ll_makefile** directory has been replaced by the the **\altera\qdesigns<*version number*>\logiclock_makefile** directory.	
The `altgxb` megafunction has been updated in the Quartus II software version 5.0. Any Stratix GX project that used the `altgxb` megafunction and was archived with the **Include functions from system libraries** option turned on will not compile correctly.	You must delete the **altgxb.tdf** file that is included in the project archive, and recompile your design.

Description	Workaround
The Quartus II software version 5.0 and later does not support Advanced NativeLink integration with the Synopsys VCS MX software.	
For all Stratix GX devices, a change has been made to the PLL settings in the gigabit transceiver blocks, which results in a reduction of total jitter for a specific data rate range. If your design has a data rate in the range of 1.01 Gbps to 1.25 Gbps, recompiling your design in the Quartus II software version 5.0 and later will result in a reduction in Total Transmit Jitter by ~35%.	
In the Quartus II software version 4.2 SP1 and later for UNIX and Linux workstations, the **Copy** command is disabled when the RTL Viewer, Technology Map Viewer, and certain Report window panes are open.	

Description	Workaround
SOPC Builder systems using an Avalon™ Tri-State Bridge may fail to compile after upgrading to the Quartus II software version 4.2 and later due to an address width mismatch.	In the Quartus II software versions 4.1 and earlier, SOPC Builder created an extra most-significant-address bit for registered slave peripherals (also called native peripherals) connected to an Avalon Tri-State Bridge. If this bridge has only native slave devices connected to it, then some designers may have connected this extra address bit in their design to a peripheral. This extra address bit no longer exists if the embedded system is regenerated using the Quartus II software version 4.2 and later. If a design uses the extra address bit and the Quartus II software is upgraded to version 4.2and later, a compilation error will occur due to the most significant address bit not being connected. This issue can be corrected without the need to modify software or hardware interconnects. If the peripheral affected by this issue is connected to an interface to user logic, then increasing the address width by one (in the interface to user logic) will correct the issue. If the peripheral affected by this issue is a custom component, edit the **class.ptf** file for that component by increasing the value called `Address_Width` by one.
For MAX 7000S family devices, the Quartus II software version 4.2 and later reports unused I/O pins as **RESERVED** by default, or as **RESERVED_INPUT** if the setting **Reserve all unused pins as inputs, tri-stated** is selected. Previous versions report unused I/O pins as **GND***, which is incorrect for MAX 7000S family devices.	To generate a correct Pin-Out file (**.pin**), recompile any MAX 7000S designs that were created in earlier versions of the Quartus II software.

Description	Workaround
The Quartus II software version 4.2 and later prohibits the placement of the IOE registers within the same LAB row as a SERDES RX or TX channel. IOE registers must be placed at least one LAB row away from an RX or TX channel. The Quartus II software version 4.1 SP2 and earlier does not prohibit the use of IOE registers in the same LAB row as a receiver (RX) or transmitter (TX) channel that utilizes the SERDES block.	Recompile any Stratix II design that was created in an earlier version of the Quartus II software with the current version. The setup time of the register (t_{SU}) will increase if the IOE register is moved to the PLD core. It is up to the designer to ensure that all setup times are met. Contact Altera Applications for more details.
The Tcl Console Window is disabled while a compilation or simulation flow is in progress. This behavior is necessary to prevent inadvertent changes to settings files during compilation.	Wait until compilation or simulation is complete before trying to run a Tcl command in the Tcl Console.
The `pll` megafunction has been removed from the Quartus II software version 4.2 and later. This megafunction implemented a digital PLL in logic cells, and was maintained for backward compatibility only.	If you wish to still use the `pll` megafunction rather than the `altpll` or `altclklock` megafunctions, you must copy the **pll.inc** and **pll.tdf** files from the **/<*Path to Quartus II installation*>/mega** directory of a previous version and place them in the same directory of the current version.
The PLLs in Stratix, Stratix II, and Stratix GX device families no longer support delay shift (time delay elements).	Altera recommends using the phase shift feature of the `altpll` megafunction to implement time shifts.
The Quartus II software version 4.2 and later no longer supports the `-entity` option for the `LL_IMPORT_FILE` assignment.	You must make the `LL_IMPORT_FILE` assignment for each instance of the entity to which you want to make the assignment.

Description	Workaround
In the Quartus II software version 4.2 and later, the RAM atom simulation models have changed in the following ways: 1. In the Quartus II software version 4.1 and earlier, all ports on the RAM atom had fixed widths (data port width=144, address port width=16, and so on). Starting in version 4.2, the widths of all ports are parameterized. 2. The default port width in the simulation model is 1 (that is, if an input is not used, it is assumed that the width of that input is 1). 3. Instead of using parameters such as `MEM1`,…, `MEM9` to hold initialization data for RAM, two parameters called "`MEM_INIT0 and MEM_INIT1`" are used. The `MEM_INIT0` parameter holds lower bytes of initialization data in increasing order of address up to a maximum of 2048 bits. The `MEM_INIT1` parameter holds the remaining upper bytes.	You must recompile your project in the Quartus II software version 4.2 or later to generate new Verilog Output files (**.vo**) or VHDL Output files (**.vho**) for the simulation tool. If your design runs at a clock speed of greater than 500 MHz, you must set the simulation resolution to picoseconds (ps).
The Quartus II software no longer uses the registry to store non–user interface–related settings. Non–user interface–related settings are stored automatically in the **quartus2.ini** file when you open the Quartus II software user interface for the first time.	You must open the Quartus II software user interface at least once before using the command-line version of the software.
The following Tcl simulator commands are no longer supported by the Quartus II software version 4.0 and later: • `dbg` • `get_time` • `get_value` • `force_value` • `release_value` • `read_memory` • `write_memory` • `run` • `print` • `get_memory_width` • `get_memory_depth` • `testbench_mode`	There are new versions of most of these commands in the **::quartus::simulator** package, which is available in the **quartus_sim.exe** module. Refer to the Quartus II Command-Line and Tcl API Help for more details. To view Tcl online Help type the following command at a command prompt: `quartus_sh --qhelp` <Enter>

Description	Workaround
When you instantiate a new RAM or ROM function with the **MegaWizard® Plug-In Manager**, the outputs of the memory function will be registered using the same clock as the inputs, by default. This is a change of behavior in that the Quartus II software versions earlier than version 4.0, the outputs are not registered by default.	This is a change of behavior that affects only new instantiations of RAM or ROM function. Existing memory functions are not affected.
In the Quartus II software version 3.0 and earlier, LogicLock™ assignments are stored in lowercase. In version 4.0 and later, designs written in case-sensitive languages may require that LogicLock assignments be in mixed case. Due to the difference in case-sensitivity between versions, LogicLock assignments made in the Quartus II software version 3.0 and earlier may not be usable in the Quartus II software version 4.0 and later.	Do not use upper case or mixed case in your HDL design files.
When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.	Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.
In the Quartus II software version 4.0 SP1 and later, the labeling of unused `GXB_TX` and `GXB_RX` pins has changed.	Pins previously labeled `GXB_VCC+` are now labeled `GXB_VCC*`. Pins previously labeled `GXB_GND+` are now labeled `GXB_GND*`.
The behavior of the Quartus II Fitter has been modified to minimize compilation time when there are no timing constraints applied to the design. This change in behavior results in an average of 40% faster compilation times and an average of 15% slower f_{MAX} performance. This change to the Fitter behavior applies only when you select the **Auto Fit** option for **Fitter Effort** on the **Fitter Settings** page of the **Settings** dialog box, and affects only Stratix, Stratix GX, Stratix II, Cyclone, and Cyclone II device families.	To return to the same behavior as earlier versions of the Quartus II software, select **Standard Fit** under **Fitter Effort** on the **Fitter Settings** page of the **Settings** dialog box, or apply appropriate timing constraints.

Description	Workaround

The following megafunctions have clear box simulation models that contain assignments that are not stored in the Quartus Settings File (**.qsf**) and are not written out to a Verilog Quartus Mapping File (**.vqm**):
`altdqs`
`altdq`
`altddio_bidir`
`altddio_out`
`altddio_input`
`altlvds_rx`
`altlvds_tx`
`altufm_i2c`
`dcfifo`
	Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.

The following megafunctions now use clear box models instead of the generic model libraries:
`altmemmult`
`altufm`
`altdq`
`altdqs`
`altremoteupdate`
`altpll_reconfig`
`altclkctrl`
	When you are simulating a design that uses one of these megafunctions, you must use the family-specific atom model library (such as **stratix_atoms.v**) instead of the generic **altera_mf.v** (or **.vhd**) library.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Changing global levels on input ports with the Resource Property Editor may cause the Quartus II software to crash in the following scenarios: • Assigning global levels to ports that do not supported global levels other than Off or Don't Care (for example, CIN). • Assigning a global level that is not supported by the current device to an input port. • Assigning a global level that is inaccessible due to location constraints on the CLKBUF and the destination input port.	Do not assign a global level to signals meeting any of these criteria.
Creating a LogicLock or custom region in the Timing Closure Floorplan by clicking and dragging outside the boundaries of the device floorplan may cause the Quartus II software to crash with an internal error.	Click within the device floorplan boundary to begin creating a region.
Opening the **Paths** dialog box by selecting a critical path in the Timing Closure Floorplan and then right-clicking and selecting **Properties** causes the destination node in the **Paths** dialog box to be populated with the source node name.	Double-click a critical path in the Timing Closure Floorplan instead of using the shortcut menu.
Restoring an I/O cell that was deleted with the Chip Editor may not restore all the settings associated with that I/O cell.	
The Quartus II software may crash with an internal error if you turn on **Full Incremental Compilation** and you turn on **Allow In-System Memory Content Editor to capture and update content independently of the system clock** in a RAM- or ROM-related megafunction. Or if you instantiated the RAM- or ROM-related megafunction directly and added "`ENABLE_RUNTIME_MOD=YES`" as part of the `LPM_HINT` parameter value.	Disable the feature or change the parameter value to "`ENABLE_RUNTIME_MOD=NO`". If you need to use the feature, turn off Incremental Compilation.

Issue	Workaround
When you are using the Chip Editor to delete the connections in carry chains, the destination node must be in a legal location for the carry chain. If this is not the case you will not be able to undo the operation or any prior operations.	Perform the following steps: 1. Delete the **Remove-Chain** command in the Change Manager. 2. Move the node back to its legal position. 3. Recreate the chain in the Resource Property editor. 4. Move the node to the desired position.
The Quartus II Fitter may fail with an error if the path to the Quartus II installation directory is longer than 96 characters.	Install in a directory with a path with fewer than 96 characters in its length.
If your design for Stratix, Stratix GX, Stratix II, Stratix II GX, Cyclone, Cyclone II, or MAX II device families uses virtual pins, the number of registers shown in the Synthesis and Fitter reports is under reported by exactly the number of virtual pins used in the design.	Manually add the number of virtual pins to the reported number of registers.
The Quartus II archive feature does not correctly archive files that have duplicate filenames, even when they are in different directories. This failure can cause compilation failures when you are using the distributed processing feature of Design Space Explorer (DSE).	Make all design file names unique.
If you remove an input term or an output term from a pin with the Chip Editor, and then use the **Undo** command, it is possible that that the pin's delay chain settings may revert to their default settings.	Use the Resource Property Editor to reset the delay chain settings for the affected pin.
If you have specified the Mozilla Firefox browser as your default browser, or specified it on the **Internet Connectivity** page of the **Options** dialog box, you may not be able to open the HDL Tutorial PDF files from the Help menu.	Use the Adobe Acrobat reader to browse to and open the PDF files.
If your design contains illegal pin assignments, and you open the Resources window in the Pin Planner, the Quartus II software may crash.	Remove any illegal pin location assignments before opening the Resources window.

Issue	Workaround
When you are listing paths from a Timing Analyzer table in the Report Window and the row number is >= 65536, the results displayed in the Messages window will be for the wrong nodes.	Use the `list_path` Tcl command shown in the following example to obtain the correct results. `list_path -npaths 1 -from <From> -to <To> <other options>` Where the <*From*> and <*To*> correspond to the values in the "From" and "To" columns in the Report Window table. The <*other options*> depend on the type of table. For example, use `-clock_setup` for Clock Setup tables, and so on. See the help on the `list_path` command for more information.
If you make a single-point `CUT=ON` assignment to a node, and then override it with a point-to-point `CUT=OFF` assignment on a specific path, the `OFF` assignment will not be honored.	
Under certain circumstances the Design Assistant reports Critical Warnings (that locate to the `altlvds_rx` or `dcfifo` megafunction) for your project, which uses the `altvds_rx` or `dcfifo` megafunction or an IP core that uses the `altvds_rx` or `dcfifo` megafunction.	These warnings can be safely ignored; no action is necessary.
You may receive a "`License not found...`" error if the path to the license file contains non-ASCII characters.	Change or remove any non-ASCII characters from the license file path.
During a SignalProbe™ compilation, you might receive warning message(s) similar to the following example: "`Routing constraints for signal <signal_name> seem to be causing unresolvable routing congestion. The constraints for the signal were removed.`"	The Compiler issues these warnings when it is unable to retain the routing constraints from a previous compilation because those routing resources were needed by the SignalProbe signal routing.
If you modify a resource (node or connection) used by a SignalProbe pin using the Resource Property Editor and then perform another SignalProbe compilation, the compilation will fail and the Quartus II software may crash with an internal error.	Do not use the Chip Editor features (Resource Property Editor, Chip Editor, or Engineering Change Manager) to modify properties of SignalProbe pins.

Issue	Workaround
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the `RETURNS` keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, click **Search** on the Help menu, and type the name of the item.
The Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the **Group** command on the Edit menu to create groups of arbitrary nodes.
If you are using the `altcam`, `altclklock`, `altlvds_rx`, or `altlvds_tx` megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name **file.eda.edif**.	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation `(debug[7..0])`, the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "`Unsupported data type in the top-level module.`"	Reserve the pins using single-name notation (for example, `debug[7]`, `debug[6]`, and so on).

Issue	Workaround
Do not change the file permissions (such as changing "read-only" to "read and write") of Quartus II Settings File (**.qsf**) and Quartus II Project File (**.qpf**) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2^31-1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (**.pof**) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (**.qsf**) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the **Assignment Editor** on the Assignments menu or by manually editing the Quartus II Settings File.	If you experience a "no fit" or an Internal Error while using routing back-annotation, delete the Routing Constraints File (**.rcf)** and back-annotate the design again after a successful compilation.
If you receive an error message saying "`System resources low...`" or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.	You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and click **Clear Messages from Window** on the shortcut menu. Additional memory can be recovered by closing the Timing Closure Floorplan.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus II Workspace File (**.qws**) <***project name***>**.qws** from the project directory. If the problem persists, delete the \<***project directory***>**db** directory.

Issue	Workaround
When you are setting phase shift and duty cycle values for clock signals using the `altpll` megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may "hang" and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.
Running individual Quartus II software executables (**quartus_map**, **quartus_fit**, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	You should run individual executables either from within the Quartus II scripting shell (**quartus_sh**) or directly at a command prompt.
If you have chosen migration devices in the **Compatible Migration Devices** dialog box, which is available from the **Device** page in the **Settings** dialog box on the Assignments menu, the Timing Closure floorplan displays only the pins and PLLs that are common to all the selected devices. However, the Chip Editor displays all the pins and PLLs available for the device specified for compilation.	
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor's "auto-completion" feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	

Issue	Workaround
Under certain circumstances, a design that uses **Virtual Pin** assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using **Virtual Pin Clock** assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the `dcfifo` or `scfifo` megafunctions in an AHDL design, you may receive an error message similar to "`The parameter LPM_WIDTHU has been set to an invalid value...`"	Either remove the `LPM_WIDTHU` parameter arguments from your AHDL `dcfifo` or `scfifo` megafunction instantiation, or explicitly set the `LPM_WIDTHU` parameter to `ceil(log2(LPM_NUMWORDS)`.
Do not open, change permissions, or delete the **/<*project directory*>/db** directory or any file therein while any Quartus II executable is running.	
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash (\) to the end of the library file name. The Quartus II user interface ignores this trailing backslash.	
Support for non-decimal radix numbers (such as hexadecimal) used as constants in the `lpm_constant`, `lpm_compare`, and `lpm_add_sub` megafunctions is limited to values that can be represented by 31 bits or fewer.	For values that require more than 31 bits, use decimal radix only.

Issue	Workaround
Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations. For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it). The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal <*name*> to atom <*name*>" are displayed to inform the user; the appearance of such messages is not a cause for alarm.	This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network.	To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (**support.microsoft.com/?kbid=896054**) for more information about possible workarounds.
The keyboard accelerators (underlines) for Alt+ key combinations do not appear in the Quartus II user interface until the Alt key is pressed the first time.	This behavior is a Windows 2000 user-specified preference. To change to the previous behavior, follow these steps: 1. On the Start menu, click **Control Panel** 2. Click **Display properties** 3. Click the **Appearance** tab 4. Click **Effects** 5. Turn off "Hide underlined letters for keyboard navigation until I press the Alt key"
If you use Windows 2000 as a software server to serve the Quartus II software to a client computer running Windows XP, running the Quartus II software on the Windows 2000 server at the same time clients are running the Quartus II software, will cause the Quartus II software on the server to crash.	Do not run the Quartus II software on the Windows 2000 server.
You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content.	Refer to the Altera Knowledge Database on the Altera web site for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.
Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.	Change the font in the **Active Title Bar** section of the **Windows Appearance** Control Panel.
If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly.	Altera recommends that you have Administrator privileges when installing the Quartus II software.

Issue	Workaround
Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.	Reinstall the **stdole32.tlb** file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.) **Windows 2000:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter> **Windows XP:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter>
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.
Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.
If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the **\quartus\bin** directory.	You must share the **\quartus** directory, not the **\quartus\bin** directory.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the **Services Control Panel** on the Start menu before running the Quartus II software.
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.	The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the **Reset All** button on the **Toolbars** page of the **Customize** dialog box, or, if the user interface does not appear, type the following command at a command prompt: `quartus -reset_desktop` <Enter>

Issue	Workaround
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "`JTAG Server -- internal error code 82 occurred`" when you click the **Add Hardware** button in the **Hardware Setup** dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the **jtagserver.exe** program and at a command prompt for that directory, type `jtagserver --install` <Enter>
If you choose to uninstall a previous version of the Quartus II software during installation, and there is a "locked" file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.	Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.
The Quartus II software version 4.2 and later does not allow a Parallel Port Software Guard (T-guard or dongle) to be used on the same parallel port as a ByteBlaster™ II download cable.	Use another download cable, such as a USB-Blaster™ or MasterBlaster™ to configure your device, or use separate parallel ports for the Software Guard and the download cable. The Quartus II Programmer is not a licensed feature, so you can remove the Software Guard to program your device, but you must replace it to use any other Quartus II software features. You can also use the USB Software Guard.
During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, a Windows Explorer window may appear.	Close the Windows Explorer window before proceeding with the installation.

Solaris, HP-UX & Linux

Issue	Workaround
On certain Solaris 8 and Linux systems, the text in the Assignment Editor and in other dialog boxes may not be readable because of the text size.	Delete or move the **~/.mw** directory and restart the Quartus II software.
If the operating system crashes, and the file system in $TMP is rebuilt automatically, the data in the **$TMP/Mw_<*user ID*>** file is corrupted, the Quartus II software may fail to start correctly.	Delete the **$TMP/Mw_<*user ID*>** file and restart the Quartus II software.

Issue	Workaround
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed on the Window menu that you cannot see.	To display the hidden windows, click **Cascade** on the Window menu.
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the **Internet Connectivity** page of the **Options** dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type `hh quartus.chm` <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at **www.hummingbird.com** for a patch for the Exceed software.
If you are running the Quartus II software version 4.0 and later on a Linux or Solaris workstation, even though **Reopen current project and files at startup** is turned on, the last project is not reopened when you restart the software.	Use the **Recent Projects** command on the File menu to reopen your last project.
The stand-alone Quartus II Programmer and SignalTap® II programs are not available on Solaris, Linux, and HP-UX workstations.	

Solaris Only

Issue	Workaround
The **Excalibur™ MegaWizard Plug-In**, which is available from the **MegaWizard Plug-In Manager**, requires the Java Runtime Environment (JRE), which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for the JRE to function properly.	Check the web site **http://sunsolve.sun.com/pub-cgi/show.pl?target=patches/J2SE** for information about any patches that might be needed.

HP-UX Only

Issue	Workaround
If you have installed patch PHCO_22076, the Quartus II software may crash when you open Help with the **hh** command.	Open Help from the user interface.
If you have installed patches PHCO_25707 or PHCO_28543, the Quartus II software will crash when you open Help from the UI.	Open Help with the **hh** command.
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: **/etc/passwd** and **/etc/group**.
Programming EPC16 configuration devices is disabled on HP-UX workstations.	

Linux Only

Issue	Workaround
If you run a remote Linux desktop session in a Windows client such as Exceed, depending on your configuration, the SignalTap II Logic Analyzer may be unstable and could crash with a segmentation fault.	Use an Xterm window to access the Quartus II software instead of a remote desktop session.
Clicking the “X” close button is visible on the Chip Editor loading progress dialog box may cause the Quartus II software to crash.	Do not click the “X” button while the Chip Editor is loading.

Issue	Workaround
If the MasterBlaster™ download cable is not listed in the **Available hardware items** list in the **Hardware Settings** tab of the **Hardware Setup** dialog box, but it is connected properly, you may not have read/write permission for the serial (`dev/ttyS`*x*) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the "`uucp`" group, or by giving read/write permission for the serial port to everyone, using the following command: `chmod o+rw /dev/ttyS`*x* where *x* is the serial port affected.
If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the `QUARTUS_MWWM` environment variable to `allwm` and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: `setenv QUARTUS_MWWM allwm` <Return> `quartus -no_splash` <Return>
Under certain circumstances, the Quartus II software may not start properly.	On a system with a static IP address, ensure that the **/etc/hosts** file has an entry for the host name of the machine on which you are running. For example, if the workstation is named "orange," there should be an entry in **/etc/hosts** with the IP address of the "orange" workstation as shown below: <*IP address of orange*> `orange` In addition, the network configuration (hostname, DHCP host name, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.
If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.	Make sure your VNC server software is version 3.3.4 or later.
If you are running the Quartus II software under Red Hat Linux 8.0, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.	Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following document for more information: **www.netapp.com/tech_library/ftp/3183.pdf**

Device Family Issues

Excalibur

Issue	Workaround
You may receive the message "`System Build Descriptor File missing parameter programming clock frequency`" for System Build Descriptor Files (**.sbd**) generated in the Quartus II software version 2.0 and earlier, after selecting the **Boot from Serial** option in the **ARM-based Excalibur MegaWizard Plug-In**.	Rerun the **ARM-based Excalibur MegaWizard Plug-In** in the current version of the Quartus II software to regenerate the SBD File and correct the error.
If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software: **Remove Redundant Logic Cells** **Perform WYSIWYG Primitive Resynthesis** Please refer to the *EPXA10 Device Errata Sheet* for details on the device errata.	To avoid bridge lockup, ensure that the **Remove Redundant Logic Cells** option is turned off for the project. If the **Perform WYSIWYG Primitive Resynthesis** option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the **MegaWizard Plug-In Manager** in the Quartus II software version 2.2 or later. This procedure will create an additional settings file (**alt_exc_stripe.esf**) to ensure that the required logic elements are implemented.

Cyclone, Stratix & Stratix GX

Issue	Workaround
If you turn off the **Optimize timing** option, and turn on the **Optimize fast-corner timing** option, the Quartus II software will crash with an internal error when you compile the design. Also applies to Cyclone II, Stratix II, and HardCopy II device families.	Be sure to turn on the **Optimize timing** option if you turn on the **Optimize fast-corner timing** option.

Issue	Workaround
The Quartus II software generates a design resource summary file for the Early Power Estimator spreadsheet for your specified device family. The file lists resources only in clock domains that have an f_{MAX} constraint. The file does not list any resources that are not associated with a clock domain, nor does it list any resources associated with an unconstrained clock domain. The Quartus II software issues a warning if unconstrained clocks are detected while generating a design summary file for the Early Power Estimator.	Apply f_{MAX} constraints to all clocks in the design, and run the Timing Analyzer before generating an Early Power Estimator file. For logic not associated with any clock domains, enter those resource counts manually into the Early Power Estimator spreadsheet.
When you use a Routing Constraints File (**.rcf**) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.	
If you use the SignalProbe feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.	The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.
In the **SignalProbe Source to Output Delays** table of the Timing Analyzer Report, the following shortcut menu commands are not available although they are available in other similar Timing Analyzer Report tables: • **List Paths** • **Locate in Chip Editor** • **Locate in Timing Closure Floorplan**	You can use other Timing Analyzer Report tables to list and locate the affected paths.

Stratix and Stratix GX

Issue	Workaround
If you use the `altddio_bidir` or `alt_dqs` megafunction and connect any data port directly to `VCC` or `GND`, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.	

Issue	Workaround
The behavior of the 0-degree phase shift setting of the `DLL_PHASE_SHIFT` parameter of the `altdqs` megafunction or the **DQS Phase Shift** logic option with the `altddio_bidir` megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.	If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2 or later, you should contact the Altera Applications department for further information.

Stratix

Issue	Workaround
Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.	
Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.	Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.

Stratix II

Issue	Workaround
An intermittent read failure has been detected on Stratix II M4K RAMs due to a software configuration error for designs compiled with Quartus II software version 5.0 SP1 and earlier.	This issue has been resolved in the Quartus II software 5.0 Service Pack 2 and Quartus II software version 5.1. To learn more about this issue, please refer to the Stratix II Errata on the Altera web site.
Due to changes in the `altlvds_tx` and `altlvds_rx` megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.	Check your assignments to make sure that the Quartus II software implemented them correctly.

Issue	Workaround
The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the `STRATIXII_MRAM_COMPATIBILITY` option is turned off.	For more information about programming file support for Stratix II devices, please refer to the *Stratix II FPGA Family Errata Sheet*, which is available on the Altera web site.
The Quartus II software version 4.2 and later supports programming file generation for EP2S60 ES devices, but only for designs where the M-RAM memory is not used.	For more information about programming file support for Stratix II devices, please refer to the *Stratix II FPGA Family Errata Sheet*, which is available on the Altera web site.
Back-annotating some designs targeted to a Stratix II device with the **Demote cell assignments to** option set to **LABs** may prevent the design from fitting.	Back-annotate the design with **Demote cell assignments to** turned off.

Stratix GX

Issue	Workaround
The `RREFB` pin names for EP1SGX10C, EP1SGX25C, EP1SGX25D, and the EP1SGX40F devices changed in the Quartus II software version 5.0. This may affect your PCB layout.	Each `RREFB` pin must be tied to ground through a resistor. Altera recommends that you not connect multiple `RREFB` pins through a single resistor to ground.

Stratix II GX

Issue	Workaround
The Quartus II software will crash with an internal error if you make a SignalProbe connection within an HSSI block.	Do not make SignalProbe connections within an HSSI block.
In Basic protocol, when the 8B10B encoder is used, the `alt2gxb` MegaWizard provides the `tx_forcedisp` and `tx_dispval` ports. These ports do not have any effect on the transmitted serial data when used in the Quartus II software version 5.1. This behavior is reflected in simulation.	None necessary.

Cyclone

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).	Recompile your design after installing the current version of the Quartus II software.
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

Cyclone II

Issue	Workaround
A write error has been detected on Cyclone II M4K RAMs when using dual ports and dual clocks for designs compiled with Quartus II software version 5.0 SP1 and earlier.	A software workaround is available to address this issue in the Quartus II software version 5.0 SP2 and Quartus II software version 5.1. To learn more, please refer to the Cyclone II Errata on the Altera web site
If your design uses dual-port, dual-clock memory with a Memory Initialization File (**.mif**) and you have set the CYCLONE_SAFE_WRITE parameter in the altsyncram megafunction to RESTRUCTURE, any changes to the MIF file contents will be ignored if you have Smart Compilation turned on.	
Back-annotating some designs targeted to a Cyclone II device with the **Demote cell assignments to** option set to **LABs** may prevent the design from fitting.	Back-annotate the design with **Demote cell assignments to** turned off.

MAX II

Issue	Workaround
If your design uses an `altparallel_flash_loader` instantiation created in the Quartus II software version 5.0 SP1 or earlier, you may receive errors during compilation because the port names have changed in the `altparallel_flash_loader` megafunction included in the Quartus II software version 5.1.	Use the Megawizard Plug-in Manager to re-generate your `altparallel_flash_loader` instantiation. Modify your design files to connect to the new `altparallel_flash_loader` port names.

HardCopy II

Issue	Workaround
The HardCopy II Companion Revision Comparison tool can be too strict and produce false positives. That is, it flags certain netlist block differences as functionality differences when they do not actually produce different behavior in silicon. The following examples illustrate this behavior: • When a DSP multiplier uses distinct asynchronous clears on its input registers, they might be ordered differently on the two revisions, but still have the same functionality. • Additional clock buffers may be inserted by the Fitter during routing that are different between the two revisions, but function identically. • The Companion Revision Comparison tool considers a global assignment of <NONE> to be different from "" (null), and reports a difference.	In each of these cases, the functionality of the two revisions is the same in silicon, but you must manually verify that the functionality is the same. You can use the block names listed in the Companion Revision Report to locate to the Resource Property Editor to verify the functionality
If you have multiple Stratix II devices in a migration chain for a HardCopy II device, you will receive a critical warning that the feature is not supported in the software.	Ignore the critical warning, it is in error, the feature is supported.

Issue	Workaround
PCI core designs compiled with versions of the PCI Compiler earlier than 4.0.0 will cause numerous spurious differences to be reported in the Companion Revision Compare section of the Compilation Report, even though the source files are correct.	Recompile the PCI core with the PCI Compiler version 4.0.0 or later.
If a PLL placed at a corner PLL location (PLL_7, PLL_8, PLL_9, or PLL_10) uses global clocks for its clock outputs, then the Companion Revision Compare report may incorrectly report that the PLL changed between the Stratix II and the HardCopy II compilation.	Make GLOBAL_SIGNAL assignments to the PLL clock outputs, recompile the design, and run the Companion Revision Compare command again.
If a PLL is being driven by a side clock, the Companion Revision Compare report may incorrectly report a difference in the PLL structures because the name of the CLKCTRL atom driving the PLL may be different in the Stratix II revision versus the HardCopy II revision.	Use global clocks to drive the PLL.
You may receive Revision Comparison warnings about differing EDA tool settings if your project directory contains a Quartus II Defaults File (**.qdf**).	Delete the Quartus II Defaults File from your project directory.

Design Flow Issues

Verification

Issue	Workaround
When an application that uses the JTAG interface to communicate with an Altera device (that is, SignalTap II, Nios II, and so on) is running, a Tcl script that calls the commands in the `jtag` Tcl package may fail with a timeout error if the `-timeout` argument is not specified with the `device_lock` Tcl command. The default timeout value of 0 sets the timeout to immediate.	Specify a non-zero timeout value when calling the `device_lock` command

Issue	Workaround
If you are using IP Toolbench to generate simulation models for Altera IP Megacore® functions, you will get an error if support for the Stratix device family is not installed.	Install support for the Stratix device family.
If you are using IP Toolbench to generate simulation models for Altera IP Megacore® functions, and you do not turn on **Generate Simulation Model** in the **Set Up Simulation Model** dialog box during setup, you will get an error when you launch the simulation using Modelsim.	Turn on **Generate Simulation Model** in the **Set Up Simulation Model** dialog box and regenerate the Megacore® .
Incremental routing may fail for nodes assigned to the SignalTap II Logic Analyzer if you have turned on any of the Physical Synthesis Fitter optimizations, such as **Perform physical synthesis for combinational logic** or **Perform register duplication** or **Perform register retiming**.	

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
When a VHDL or Verilog design specifies a RAM, there are a few cases in which the read-during-write behavior of the RAM will differ between the original design and the hardware implementation and no warning will be given. The following examples illustrate this behavior: The first case occurs when a RAM in a lower-level module directly drives a set of registers in an upper-level module. To work around this problem, move the registers to the lower-level module. The second case occurs when there is combinational logic between a RAM and a set of registers, and the design specifies the write operation of the RAM will occur before the read operation. To work around this problem, remove the logic between the RAM and the registers. The third case is the same as the second case, with the exception that the design specifies the read operation of the RAM will occur before the write operation, and the read address of the RAM is registered. To get around this problem, either remove the logic between the RAM and the registers, or set the Automatic RAM Replacement option to "Off."	The workaround for each case is shown immediately following the example.

Issue	Workaround
The Quartus II software version 4.0 and later may give the message "`Error: Duplicate entity <name> found in file <filename1> colliding with the one found in file <filename2>`," for a project that compiled successfully with Quartus II 2.2 or earlier.	The Quartus II software gives an error message when it finds two or more entities with the same name. To avoid this error in the future, remove the duplicate entity or entities. If you cannot remove the duplicate entity, you can direct the Quartus II software to ignore the duplication by adding `set_global_assignment -name IGNORE_DUPLICATE_DESIGN_ENTITY ON` to your Quartus II Settings File (**.qsf**). Altera recommends that you avoid using this workaround if possible.

Verilog HDL Integrated Synthesis

Issue	Workaround
A Verilog HDL design that compiles successfully in earlier versions fails in the Quartus II software version 5.1 with the message "`Formal port <port_name> must be connected to a structural net expression`."	The Verilog language requires that a module instance output port be connected to a net, and not to a reg variable or to a constant. Previous versions of the Quartus II software did not enforce this restriction. Change the variable connected to the module instance output port to a wire datatype.
A Verilog design that compiles successfully in earlier versions fails in the Quartus II software version 5.0 with the message "`Error: Verilog HDL or VHDL error at <filename(line)>: object "<pin_name>" declared in a List of Port Declarations cannot be redeclared within the Module Body`"	Remove the declaration in the module body. Ports must be completely specified in the Verilog 2001 list of ports declaration, including where necessary the direction, width, net or variable type, and whether the port is signed or unsigned.

SignalTap II

Issue	Workaround
Under some circumstances, an incremental SignalTap II compilation that follows a full compilation for a Cyclone II device, will fail with an error message reporting that an input port cannot be inverted.	Perform a full compilation and reapply the SignalTap II settings.

In SignalTap II, nodes dropped in from the Node Finder are always sorted and inserted in descending order, for example, `foo[3]`, `foo[2]`, `foo[1]`, `foo[0]`. If this is the incorrect order, you can select the **LSB on Top, MSB on Bottom** option. In version 5.1, negative ranges are now allowed in Verilog HDL, however negative numbers are inserted in the reverse order, for example, `foo[3]`, `foo[2]`, `foo[1]`, `foo[0]`, `foo[-3]`. foo`[-2]`, `foo[-1]`.	

SOPC Builder Issues

Issue	Workaround
Avalon burst read transfers fail if the master and slave port are in different clock domains. In this case, the Avalon switch fabric allows the master port to initiate a read burst, but never asserts the master port's readdatavalid signal later. This unexpected condition could lock the master port, preventing it from performing further transfers, or cause other trouble within the master component.	In SOPC Builder do not connect master and slave ports in different clock domains if the master port can initiate read bursts.
Avalon burst transfers can be interrupted if pipelining for high performance is turned on. In this case, during a burst transfer between a master-slave pair, the Avalon switch fabric might grant slave access to a different master port before completion of the previous burst.	In SOPC Builder do not turn on pipelining for high performance on clock domains that contain Avalon ports capable of performing burst transfers.
SOPC Builder system generation might fail for VHDL systems that use pipelining for high performance, if a slave port does not use the address signal.	Add an address signal to the slave port. You do not have to use the address signal in the VHDL code.
Back-to-back burst transfers from a master to a slave that has a different burst count or bandwidth may fail.	Wait until the slave has finished the read burst before starting a write burst.
Under some circumstances, the automatic addressing feature does not function correctly.	Assign the base address for the component manually.
The setting of the **Dual-Port Access** option , in the Legacy On-Chip Memory wizard is always shown as “Off” regardless of setting.	Always set the **Dual-Port Access** option to your desired setting before clicking **Finish** in the wizard.

Issue	Workaround
Under some circumstances, the SOPC Builder does not display correctly on systems in which the graphics card uses hardware acceleration.	Turn off, or reduce the level of hardware acceleration.
In SOPC Builder, Avalon Masters that address more than 32 bits of slave address space do not issue warning.	Redesign your system to avoid giving masters greater than 32 bits of address space.
On the SOPC Builder PLL component, you cannot access the `pfdena` signal through the Avalon `control` register. If you enable the `pfdena` signal on the `altpll` block, the PLL component configuration GUI allows you to select that you want to access the `pfdena` signal via the PFDENA bit in the `control` register. However, the hardware does not support this mode of operation. Software attempting to access the PFDENA bit will not function correctly.	You can export the `pfdena` signal to the top level of the system module, or you can disable the `pfdena` signal on the `altpll`. The hardware will support this feature in version 6.0 of the Quartus II software.
If you open more than one SOPC Builder project simultaneously, you will receive an error message similar to the following example: "`bad or corrupt 'class.ptf' file`."	Open the SOPC Builder only when no other SOPC Builder project is already open.
SOPC Builder fails to open on UNIX when invoked from the **MegaWizard Plug-In Manager**.	Open SOPC Builder by clicking **SOPC Builder** on the Quartus II Tools menu.
You may see random display errors, such as streaks and blotches, in the SOPC Builder GUI.	Lower the **Hardware Acceleration** setting on the **Troubleshooting** tab of the **Advanced Display Settings** dialog box in your **Display Settings** control panel. There is a known incompatibility between the current Java Runtime Environment (JRE) and certain laptop graphics drivers.
When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.	Using the SOPC Builder Component Editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.

Issue	Workaround
If the Quartus II software is installed in a directory that has space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.
When adding an Excalibur Stripe component in conjunction with Avalon peripherals, you may encounter SOPC Builder errors indicating that too many masters are present.	If the master-connection patch-panel is not visible, click **Show Master Connections** on the View menu. Then click the master/slave intersection indicated by the error message. This will remove the connection. Click again to restore the connection and the error will not reappear.
Designs targeting Excalibur devices that use Boot From Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.	The Excalibur boot loader in the Quartus II software version 3.0 and later does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the **makeprogfile** utility during the software build process does not work with this version of the boot loader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the **makeprogfile** utility at the command line with the `–nc` (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the \<***XA dev kit install directory***>**\bin** folder. Modify line 1034 of this script to remove the `-nc` option. For example, line 1034 should be changed as shown in this example. `$command = "makeprogfile –nc -b ${fileBase}_bootdata.o $SBD $SBI ${fileBase}.hex";` You must recompile your software project for this change to take effect.
The SOPC Builder and Nios Software Development Kit shell may “hang” and become unresponsive if you run either program while the Frisk antivirus software is running.	Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios SDK shell.

EDA Integration Issues

Issue	Workaround
Timing simulation with the Synopsys VCS MX software is not supported in the Quartus II software version 5.1.	
You cannot perform RTL simulation of the SerialLite and RLDRAM IP MegaCores in 3rd party simulators using the NativeLink integration feature.	Perform simulation manually as described in the User Guide for the MegaCore you are using.
FIFO Partitioner instances can only be simulated in 3rd party simulators using the original VHDL source files from the **quartus/libraries/megafunctions/** directory, and NativeLink integration is not supported.	Perform simulation manually as described in the FIFO Partitioner User Guide available from the Literature page of the Altera web site.
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
Support has been added for generation of IBIS Output Files (**.ibs**) for EPCS1 and EPCS4 Serial Configuration Devices.	The IBIS Output File will be generated in the **\<*project name*>\board\ibis** directory after compilation when the design is targeted to a Cyclone device and Active Serial configuration scheme using EPCS1 or EPCS4 devices is chosen.
NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.	

Simulation Model Changes

altera_mf Models

I/O Models

Model	Change
altlvds_rx	Added parameter "PORT_RX_DATA_ALIGN" to control connectivity of data_align port for Stratix, Stratix GX, Stratix II, Stratix II GX, HardCopy, and HardCopy II families.
altlvds_tx	Fixed byte ordering problem in LE-based LVDS transmitter
altddio_in	Added parameter "INVERT_INPUT_CLOCKS" for APEX II, Stratix, Stratix GX, Stratix II, Stratix II GX, Cyclone, Cyclone II, HardCopy, and HardCopy II families.

220model Models

Model	Change
lpm_counter	Added parameter "LPM_PORT_UPDOWN" to control connectivity of the updown port.

Notes:

- Major changes to Altera primitives simulation models:
    - Added new primitives CLKLOCK, TRI, LUT_INPUT, LUT_OUTPUT, DFF, DFFE, SRFF, SRFFE, JKFF,JKFFE, TFF, TFFE, LATCH, ALT_INBUF, ALT_IOBUF, ALT_OUTBUF & ALT_OUTBUF_TRI.
    - All new and existing primitives have been reallocated to new **altera_primitives** library.

      altera_primitives.v(hd) and **altera_primitives_components.vhd** are located in the **quartus\eda\sim_lib** directory.
    - Only LCELL primitive still remains in **altera_mf** library.
- Simulation PLI function convert_hex2ver.dll has been replaced by Verilog task convert_hex2ver , located in the **altera_mf** and **220model** libraries.

- The ModelSim software gives the following warning when **altera_mf** or **220models** megafunction models are compiled with the `-87` option:

```
#** Warning (vcom-1148) Condition in IF GENERATE must
be static
```

You can safely ignore this warning because under the 1987 rules, the constant is not considered to be static because of the initialization from the function call.

- RAM Megafunction models support only the HEX format for all other EDA simulators. Manually convert MIF format to HEX first in the Quartus II software.

Software Issues Resolved

This section list the numbers of the Customer Service Requests that were fixed or otherwise resolved in this version of the Quartus II software.

Customer Service Request Numbers Resolved in this Release				
10163295	10248419	10250875	10270391	10300409
10338260	10338582	10340296	10346256	10346256
10365528	10376774	10381692	10382648	10401684
10407570	10408238	10409876	10409876	10415752
10419478	10420852	10422062	10422062	10433346
10440258	10442554	10443920	10445096	10445596
10445726	10448158	10448626	10449222	10451568
10451758	10451808	10451960	10453146	10454672
10455230	10455928	10457732	10457946	10459150
10462818	10464114	10464212	10465514	10465884
10466610	10466738	10467124	10467502	10468194
10468284	10470220	10472820	10473962	10474310
10474374	10475352	10475500	10476632	10478762
10480544	10481602	10481803	10482443	10482443
10482443	10483519	10484309	10485011	10485785
10486084	10486346	10486346	10486408	10486768
10487160	10487197	10487658	10487669	10487776
10488089	10488126	10488443	10488463	10488561
10488561	10488562	10488757	10488865	10488865
10489130	10489142	10489227	10489353	10489461
10489675	10489883	10489911	10490035	10490636
10490667	10490799	10491128	10491215	10491299
10491382	10491614	10491660	10491709	10491777
10491964	10492530	10492571	10492892	10493008
10493265	10493374	10493374	10493453	10493453
10493500	10493658	10493781	10493811	10493888
10494188	10494333	10494369	10494372	10494399
10494745	10494762	10494816	10494839	10495018
10495018	10495022	10495229	10495311	10495434
10495585	10495687	10495861	10495880	10496064
10496098	10496445	10496503	10496592	10496721
10497357	10497359	10497464	10497538	10497677
10497778	10497778	10497810	10497835	10497953
10498060	10498148	10498167	10498180	10498180
10498237	10498519	10498636	10498678	10498695
10498791	10498823	10498857	10498864	10498891
10498949	10498949	10498962	10499014	10499014
10499014	10499014	10499014	10499014	10499014
10499077	10499108	10499160	10499160	10499275
10499356	10499407	10499447	10499491	10499505
10499531	10499566	10499577	10499660	10499767
10499770	10499815	10500096	10500098	10500152
10500281	10500325	10500346	10500520	10500536
10500543	10500544	10500587	10500596	10500631

Customer Service Request Numbers Resolved in this Release				
10500631	10500639	10500639	10500756	10500776
10500791	10500843	10500950	10501002	10501004
10501011	10501149	10501322	10501335	10501335
10501420	10501482	10501800	10501815	10502043
10502108	10502333	10502378	10502398	10502437
10502569	10502574	10502577	10502690	10502704
10502751	10502751	10502899	10502962	10502989
10503059	10503098	10503100	10503142	10503142
10503350	10503452	10503476	10503530	10503546
10503550	10503652	10503675	10503678	10503699
10503728	10503790	10503805	10503882	10503942
10503961	10503961	10504014	10504014	10504110
10504152	10504232	10504235	10504260	10504352
10504442	10504498	10504517	10504613	10504630
10504643	10504647	10504647	10504660	10504660
10504846	10504878	10504915	10504966	10504978
10504998	10505103	10505104	10505148	10505162
10505247	10505299	10505447	10505492	10505494
10505603	10505627	10505663	10505667	10505790
10505838	10506004	10506143	10506180	10506180
10506218	10506218	10506269	10506336	10506358
10506363	10506442	10506477	10506477	10506479
10506595	10506609	10506689	10506795	10506869
10506869	10506869	10506942	10507004	10507053
10507083	10507136	10507144	10507171	10507268
10507342	10507369	10507484	10507488	10507509
10507509	10507734	10507764	10507873	10507930
10507966	10507986	10508092	10508138	10508176
10508257	10508279	10508308	10508315	10508318
10508379	10508512	10508579	10508580	10508580
10508588	10508644	10508680	10508744	10508803
10508830	10508830	10508863	10508976	10509086
10509125	10509163	10509289	10509684	10509808
10510005	10510112	10510187	10510242	10510255
10510372	10510379	10511075	10511089	10511302
10511334	10511589	10511768	10511981	10512041
10512252	10512366	10512430	10512431	10512436
10512441	10512564	10512823	10512823	10512858
10512879	10512944	10513082	10513141	10513201
10513256	10513322	10513351	10513470	10513472
10513487	10513488	10513585	10513703	10513963
10514038	10514071	10514071	10514071	10514118
10514212	10514493	10514557	10514597	10514601
10514681	10514743	10514774	10514898	10515046
10515113	10515274	10515307	10515369	10515369
10515533	10515630	10516099	10516297	10516329
10516730	10516800	10516911	10517023	10517268
10517623	10517844	10517884	10518123	10518133
10518172	10518939	10519580		

Latest Known Quartus II Software Issues

For known software issues after publication of this version of the *Quartus II Software Release Notes*, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Find Answers Database at the following URL:

http://answers.altera.com/altera/index.jsp?/Topics/Support Solutions/Known Issues/Software/Quartus II

Revision History

Revision	Description
1.0	Initial Release
1.1	Added SR Numbers
1.2	Added information about Timing Model changes