Quartus II Software Release Notes

July 2004 **Quartus II version 4.1**

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **\altera<*version number*>\quartus** directory.

New Features & Enhancements

The Quartus II software version 4.1 includes the following new features and enhancements:

- In-System Updating of RAM/ROM and Constants – allows you to update the contents of your FPGA memory without recompiling the design
- Technology Map Viewer – allows you to view a post-synthesis representation of your design mapped into Altera device primitives.
- SignalTap® II Logic Analyzer enhancements – the SignalTap II Logic Analyzer now includes a new MegaWizard® Plug In to allow you to easily embed the analyzer in your HDL code, as well as new advanced trigger conditions.
- Resource and Timing Optimization Advisors – these new tools provide specific advice to improve resource utilization and timing performance through suggestions for changing your settings and assignments.
- Enhanced support for revisions and versions – allows you to more easily experiment with different versions of settings and source files.
- CSV-format file import and export – aids in transferring assignments and pin-out data between the Quartus II software and other tools such as PCB design software that support this Microsoft Excel file format.

Project & Settings Files In This Release

The method that the Quartus II software version 4.0 and later uses to store assignments has changed substantially from the method used by the Quartus II software version 3.0 and earlier.

If you wish to work on a project you created using the Quartus II software version 3.0 or earlier, you should open and save the project in the GUI once, even if you are using the command-line executables to compile your project. Opening and saving your project in the GUI ensures that your setting and assignment files are converted properly.

When you open a project created in the Quartus II software version 3.0 or earlier, the following changes are made to your assignment and setting files:

- Your **<*project*>.quartus** file is converted to the new Quartus Project File (**.qpf**) format, and the original file is moved to the \<***project***>\<***project***>**.bak** directory.
- The contents of your Compiler Settings File (**.csf**), Entity Settings File(s) (**.esf**), Simulation Settings File (**.ssf**), Project Settings File (**.psf**), and Software Build Settings File (**.fsf**) are merged into the new Quartus Settings File (**<*project*>.qsf**), and the original files are moved to the \<***project***>\<***project***>**.bak** directory.

- Once the Quartus II software has converted your files and moved the originals to the backup directory, the original files will not be used by the Quartus II software, so subsequent changes made to those files will be ignored.

Device Support & Pin-Out Status

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices
Serial Configuration Device	EPCS16

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Cyclone™ II	EP2C5	EP2C8
	EP2C20	EP2C35
	EP2C50	EP2C70

Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
None	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device
Stratix® II	EP2S15
	EP2S30
	EP2S60
	EP2S90
	EP2S130
	EP2S180
Cyclone® II	EP2C5
	EP2C8
	EP2C20
	EP2C 35
	EP2C 50
	EP2C 70
MAX® II	EPM240
	EPM570
	EPM1270
	EPM2210

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
APEX™ II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
Cyclone	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
FLEX® 10K	All	3.0
FLEX 10KA	All	3.0
Mercury™ *(1)*	EP1M120	2.1 SP1
MAX 3000 *(1)*	EPM3512A	2.1 SP1
MAX 7000 *(1)*	EPM7512B	2.1 SP1
MAX 7000S	All	3.0
Stratix *(2)*	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix GX *(2)*	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1

(1) Timing models for devices in this device family not listed here became final in versions 2.1 and earlier.
(2) The timing models for devices in this family have been updated in this version of the Quartus II software.

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX 20K, APEX 20KE, APEX 20KC, Excalibur, FLEX 6000, and FLEX 10KE device families. Timing models for these device families became final in versions earlier than version 2.1.

EDA Interface Information

The Quartus II software version 4.1 supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink® support
Mentor Graphics® LeonardoSpectrum	2004a-Update1	✓
Synopsys Design Compiler	2003.06	
Synopsys Design Compiler FPGA	2004.06	
Synopsys FPGA Compiler II	3.8	✓
Mentor Graphics Precision RTL Synthesis	2004a-Update1	✓
Synplicity Synplify and Synplify Pro	7.6.1	✓
Magma Design Automation PALACE™	2.4	✓
Verification Tools	**Version**	**NativeLink support**
Cadence NC-Verilog (Windows) Cadence NC-Verilog (UNIX)	5.1-s010 5.1-s012	✓
Cadence NC-VHDL (Windows) Cadence NC-VHDL (UNIX)	5.1-s010 5.1-s012	✓
Cadence Verilog-XL (Windows)	3.3	
Cadence Verilog-XL (UNIX)	5.1-s012	
Model Technology™ ModelSim®	5.8c	✓
Model Technology ModelSim-Altera	5.8c	✓
Mentor Graphics BLAST	1.2.2	
Synopsys PrimeTime	2003.03 SP1	✓
Synopsys Scirocco	2002.06	✓
Synopsys VSS	2000.05	
Synopsys VCS	7.1.1	
Mentor Graphics Tau	EN2002	
Cadence Incisive Conformal	4.3.0.a	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Changes to Default Settings in This Release

This section lists the variable names for Quartus II settings that have different default values in the Quartus II software version 4.1 from the previous version. The default values and a list of the changed values are stored in the **/<*Quartus II Installation directory*>/bin/assignments_default.qdf** file.

Setting Keyword	Default in 4.0	Default in 4.1
FITTER_EFFORT	"Standard Fit"	"Auto Fit"

Changes to Software Behavior

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
The order of ports for the **ARM®-based Excalibur MegaWizard® Plug-In**-generated symbol for the stripe changed in version 2.0 of the Quartus II software. If you re-run the **MegaWizard Plug-In Manager** (Tools menu) for a design created in a version of the Quartus II software earlier than version 2.0, you will receive port connection errors when you compile the design.	To avoid receiving these errors, adjust the port connections in the Block Design File (**.bdf**) after updating the symbol.

Description	Workaround
Versions of the Quartus II software earlier than version 2.2 did not correctly implement the following functions in DSP blocks in Stratix devices: • Mixed-sign multiplications of 19 bits and greater • Dynamic-sign multiplications of 19 bits and greater • Signed multiplications greater than 36 bits	Designs that implement DSP functions must be recompiled in the Quartus II software version 2.2 or later. The current version of Quartus II software implements the design correctly, but uses more resources and has reduced performance from earlier versions.
Versions of the Quartus II software earlier than version 3.0 cannot open BDF created with the Quartus II software version 3.0 and later.	You can alter the BDF so that it can be opened in earlier versions, but location assignments will be lost. 1. Open the BDF in any text editor (vi, emacs, notepad). 2. Change the version from `1.3` to `1.2` in the header section. 3. Remove all the lines with string "`location`," for example, `(annotation_block (location)(rect -336 -40 -248 -8)).` 4. Save the file.
The Quartus II software no longer uses the registry to store non-user interface-related settings. Non-user interface-related settings are stored automatically in the **quartus2.ini** file when you open the Quartus II software user interface for the first time.	You must open the Quartus II software user interface at least once before using the command-line version of the software.
If you open a project that was created using an earlier version of the Quartus II software, you may receive a message that indicates that the database is incompatible and that results of the last compilation will be lost.	To maintain existing placement information and optionally routing information, back-annotate all of the project assignments in the earlier version. You may also need to generate a Quartus II Verilog Mapping file (**.vqm**) netlist to preserve the result of Physical Synthesis.
The Quartus II software versions 2.1 and later no longer support the Quartus Settings File (**.qsf**) variable `MIGRATION_DEVICES`.	To specify migration device names in the QSF, use the `DEVICE_MIGRATION_LIST` variable. For example: `DEVICE_MIGRATION_LIST = "DEVICE_A,DEVICE_B,DEVICE_C";`

Description	Workaround
You may receive an "`invalid command name`" error when you run an existing Tcl script that uses the Tk toolkit for its user interface. Beginning with the Quartus II software version 2.2, the Quartus II software no longer initializes the Tk toolkit automatically when starting any process.	Add the Tcl command "`init_tk`" to the beginning of any Tcl script that uses the Tk toolkit.
The **lpm_fifo MegaWizard Plug-In** has been removed from the Quartus II software version 2.2 and later. The `lpm_fifo` megafunction is still included for backward compatibility with older designs.	Altera recommends that you use the **"memory compiler/FIFO" MegaWizard Plug-In** for all new designs requiring FIFO functions.
The following Tcl simulator commands are no longer supported by the Quartus II software version 4.0 and later: • `dbg` • `get_time` • `get_value` • `force_value` • `release_value` • `read_memory` • `write_memory` • `run` • `print` • `get_memory_width` • `get_memory_depth` • `testbench_mode`	There are new versions of most of these commands in the ::quartus::simulator package which is available in the **quartus_sim.exe** module. Refer to the Tcl online help for more details. To view Tcl online help type the following command at a command prompt: `quartus_sh --qhelp` <Enter>
When you instantiate a new RAM or ROM function with the **MegaWizard Plug-In Manager**, the outputs of the memory function will be registered using the same clock as the inputs, by default. This is a change of behavior in that prior to the Quartus II software version 4.0, the outputs were not registered by default.	This is a change of behavior that affects only new instantiations of RAM or ROM function. Existing memory functions are not affected.

Description	Workaround
In the Quartus II software version 3.0 and earlier, LogicLock™ assignments are stored in lower case. In version 4.0 and later, designs written in case-sensitive languages may require that LogicLock assignments be in mixed case. Due to the difference in case-sensitivity between versions, LogicLock assignments made in the Quartus II software version 3.0 and earlier may not be usable in the Quartus II software version 4.0 and later.	Do not use upper case or mixed case in your HDL design files.
When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0, under certain circumstances when you open the design in the Quartus II software version 4.0, the LogicLock regions will not be handled properly.	Redefine the LogicLock regions in the Quartus II software version 4.0 to eliminate the errors.
Changes made to settings and/or assignments in the Assignment Editor, Floorplan Editor, or with Tcl commands in the Tcl Console window are saved to disk only when you choose **Save Project** (File menu). Choosing **Save** in the Assignment Editor, Floorplan Editor, or **Settings** dialog box saves the changes to memory only. They are not committed to disk until you choose **Save Project** (File menu), close the project, or exit from the Quartus II software. If you have turned off **Save changes to all files before starting a compilation, simulation, or software build** on the **Processing** page of the **Options** dialog box (Tools menu), changes you made may not be reflected in the latest compilation.	Turn on **Save changes to all files before starting a compilation, simulation, or software build** on the **Processing** page of the **Options** dialog box (Tools menu). *or* Choose **Save Project** (File menu) after making any changes to Settings or Assignments.
In the Quartus II software version 4.0 SP1, the labeling of unused `GXB_TX` and `GXB_RX` pins has changed.	Pins previously labeled `GXB_VCC+` are now labeled `GXB_VCC*`, pins previously labeled `GXB_GND+` are now labeled `GXB_GND*`.

Description	Workaround
The behavior of the Quartus II Fitter has been modified to minimize compilation time when there are no timing constraints applied to the design. This change in behavior results in an average of 40% faster compilation times and an average of 15% worse f_{MAX} performance. This change to the Fitter behavior applies only when the **Auto Fit** option is chosen for **Fitter Effort** on the **Fitter Settings** page of the **Settings** dialog box (Assignments menu), and affects only Stratix, Stratix GX, Stratix II, Cyclone, and Cyclone II device families.	To return to the same behavior as earlier versions of the Quartus II software, choose **Standard Fit** under **Fitter Effort** on the **Fitter Settings** page of the **Settings** dialog box (Assignments menu), or apply appropriate timing constraints.

The following megafunctions have clear box simulation models which contain assignments that are not stored in the Quartus Settings File (**.qsf**) and are not written out to a Verilog Quartus Mapping File (**.vqm**).
`altdqs`
`altdq`
`altddio_bidir`
`altddio_out`
`altddio_input`
	Do not use VQM to save an atom netlist file if you are using these megafunctions.

The following megafunctions now use clear box models instead of the generic model libraries:
`altmemmult`
`altufm`
`altdq`
`altdqs`
`altremoteupdate`
`altpll_reconfig`
`altclkctrl`
	When you are simulating a design that uses one of these megafunctions, you must use the family-specific atom model library (such as **stratix_atoms.v**) instead of the generic **altera_mf.v** (or**.vhd**) library.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Not all speed grades of a given device share the same features.	Refer to the Altera device Handbook or Data Sheet for further information.
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the `RETURNS` keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, choose **Index** (Help menu) and type the name of the item.
For APEX 20KE devices, the Quartus II software provides limited support for the following I/O standards that are not available with the **I/O Standard** logic option: • **LVPECL** is a differential I/O standard that is similar to the **LVDS** I/O standard. APEX 20KE devices can support LVPECL I/O pins by using the I/O pins in LVDS mode with an external resistor network. • **PCI-X** is an enhanced version of the **PCI** I/O standard that can support a higher average bandwidth. This standard has more stringent requirements than PCI.	To use the **LVPECL** I/O standard in APEX 20KE devices in the Quartus II software, set the **I/O Standard** logic option for the pins to **LVDS** and connect the pins to an appropriate external resistor network. The APEX 20KE I/O drivers meet the requirements for **PCI-X**. Turn on the **PCI I/O** logic option to support PCI-X requirements, including the overshoot clamp.
The Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.

Issue	Workaround
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the **Group** command (Edit menu) to create groups of arbitrary nodes.
If you are using the `altcam`, `altclklock`, `altlvds_rx`, or `altlvds_tx` megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Last Compilation floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name **file.eda.edif**.	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (`debug[7..0]`), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "`Unsupported data type in the top-level module.`"	Reserve the pins using single name notation (for example, `debug7`, `debug6`, and so on).
If you are using the **HSTL Class II** I/O standard with an APEX II device, additional information is required.	Contact the Altera Customer Applications department at **apexii@altera.com** for information about Service Packs and device pin-outs.
Do not change the file permissions (such as changing "read-only" to "read and write") of Quartus II settings and configurations files (**.qpf**, and **.qsf**,) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2^31-1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (**.pof**) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.

Issue	Workaround
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the QSF or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the **Assignment Editor** (Assignments menu) or by manually editing the QSF.	If you experience a "no fit" or an Internal Error while using routing back-annotation, delete the Routing Constraints File (**.rcf)** and back-annotate the design again after a successful compilation.
After register duplication has occurred, the duplicated register has a unique name in the form <*original name*>~<*suffix*>. The new register name may not properly inherit timing assignments made with wild cards.	Make sure that duplicated register names are included in your wild card match when making timing assignments.
If you receive an error message saying "`System resources low...`" or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.	You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and choose **Clear Messages from Window** (right button pop-up menu). Additional memory can be recovered by closing the Floorplan Editor.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus Workspace File (**.qws**) **<*project name*>.qws** from the project directory. If the problem persists, delete the **<project directory>***\db** directory.
When you are setting phase shift and duty cycle values for clock signals using the `altpll` megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may "hang" and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes its execution.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.
Running individual Quartus II software executables (**quartus_map**, **quartus_fit**, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	You should run individual executables either from within the Quartus II scripting shell (**quartus_sh**) or directly at a command prompt.

Issue	Workaround
If you have chosen migration devices in the **Compatible Migration Devices** dialog box, which is available from the **Device** page in the **Settings** dialog box (Assignments menu), the Timing Closure Floorplan and the Last Compilation Floorplan will display only the pins and PLLs that are common to all the selected devices. However, the Chip Editor will display all the pins and PLLs available for the device specified for compilation.	
Turning **Physical Synthesis** on in the **Physical Synthesis Optimizations** page under **Fitter Settings** in the **Settings** dialog box on average will cause compilation time to double and peak memory usage to increase by approximately 20%. For large designs, the Progress Bar for the Fitter may appear to be stuck in the 50-70% range while the elapsed time continues to increase. Provided that compilation time has not increased over 10X, this is normal and the compilation should be allowed to finish. In rare cases, the compilation time may increase by more than 10X. In these cases, it is appropriate to apply the workaround if you cannot tolerate such a long compilation time.	If compilation time is excessive with **Physical Synthesis** turned on, you can either remove or convert LogicLock regions to soft before recompiling, or you can turn off **Physical Synthesis**.
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
Occasionally you may receive an error message saying "`Can't contact license server <`*port@server*`>`..." even though you know the license server is connected and running.	Add an explicit port number to the `SERVER` line of the license file on the server in question. For example `1700@athena`. Altera recommends that you do not use port 27000 because it is the default port that is used when no explicit port number is specified.
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor's "auto-completion" feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.

Issue	Workaround
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	
Under certain circumstances, a design that uses **Virtual Pin** assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using **Virtual Pin Clock** assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
Setting the left and right page margins to any values totaling more than 7.78 inches in the **Page Setup** dialog box (File menu) may cause the Quartus II software to "hang."	Set the page margins to values totaling less than 7.78 inches.
If you export settings and assignments and do not assign a file extension, the Quartus II software will not recognize the file format and will give an error message.	Always use the appropriate file extension when exporting files from the Quartus II software.
If you use the `dcfifo` or `scfifo` megafunctions in an AHDL design, you may receive an error message similar to "`The parameter LPM_WIDTHU has been set to an invalid value…`"	Either remove the `LPM_WIDTHU` parameter arguments from your AHDL `dcfifo` or `scfifo` megafunction instantiation, or explicitly set the `LPM_WIDTHU` parameter to `ceil(log2(LPM_NUMWORDS)`.
If you use the MegaWizard Plug-In Manager to create files for your design, the Quartus II software might not "remember" your settings for device, etc.	The Quartus II software does not write your settings to the Quartus Settings File (**.qsf**) until you close the MegaWizard Plug-In manager. You must save your settings with the **Save** or **Save As** command (File menu).
If you change the number of pipelining registers in your SignalProbe signal path from zero to one, the Quartus II software will report the connection as successfully routed, even though it is not.	Either make the original SignalProbe assignment with one pipeline register, or perform the SignalProbe compilation twice. The second SignalProbe compilation will make the connection correctly.
If your design uses an on-demand synchronous load behavior for registers that drive output pins or output enables and you have put tight t_{CO} constraints on those registers, you may experience unexpected results after back-annotating your design.	Save the post-fitting netlist as a Verilog Quartus Mapping file (**.vqm**), and use the VQM as the top-level entity in a new project for subsequent compilations/fitting attempts.

Issue	Workaround
Do not open, change permissions, or delete the **quartus/db** directory or any file therein while any Quartus II executable is running.	
If you open the **Import Assignments** dialog box from the Assignments menu, the regions you selected in the LogicLock Regions window will be ignored and you may receive a warning message saying "`Warning: No LogicLock Regions to Import`"	Use the **Import Assignments** command on the right button pop-up menu after selecting the LogicLock region in the LogicLock Regions window.
If you open the **Back-Annotation** dialog from the **LogicLock Region Properties** dialog box when the device selected for the last compilation is different from the currently assigned device, the Quartus II software may crash during back-annotation.	Close the **LogicLock Region Properties** dialog box and open the **Back-Annotation** dialog box from the Assignments menu.
If you select a LogicLock region in the Timing Closure Floorplan or the Last Compilation Floorplan and open the LogicLock Regions window, and then change any property of the selected LogicLock region, any changes you made will be lost. In the case where you have a second LogicLock region selected in the LogicLock Regions window, the changed region will acquire the properties of the second region, rather than the changes you made.	Open the LogicLock Regions window and make the desired changes there instead of in the **LogicLock Region Properties** dialog box.
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash (\) to the end of the library filename. The Quartus II user interface ignores this trailing backslash.	
If you back-annotate the routing of a LogicLock region for which the **Reserve unused logic** option has been turned on, the Quartus II may not be able to fit your design in the selected device because too much logic may have been reserved for the LogicLock region(s).	Turn on the **Reserve unused logic** option for all your LogicLock regions.

Issue	Workaround
The MegaWizard Plug-In Manager erroneously permits the In System Memory Editor to be used with M512 memory blocks in Stratix devices for single-port memory megafunctions such as `lpm_ram_dq` or `altsyncram`.	Do not use the In System Memory Editor to edit M512 memory blocks.
Support for non-decimal radix numbers (such as hexadecimal) used as constants in the `lpm_constant`, `lpm_compare`, and `lpm_add_sub` megafunctions is limited to values that can be represented by 31 bits or fewer.	For values that require more than 31 bits, use decimal radix only.
In situations where the Quartus II software merges multiple ROMs into a single RAM block when using LogicLock regions in an APEX II design, a new Memory Initialization File (.**mif**) will be created and should be used for subsequent compilations. If you need to change the ROM data, you must change it in the new MIF.	
If you delete the location of the license file and then click **Cancel** in the **License Setup** page of the **Options** dialog box (Tools menu), the Quartus II software may "hang."	
The `lpm_counter` megafunction no longer recognizes the value "DEFAULT" for the `LPM_DIRECTION` parameter.	Either manually change the "DEFAULT" value to "UNUSED" or rerun the MegaWizard Plug-In Manager to modify your variation of the megafunction.

Platform-Specific Issues

PC Only

Issue	Workaround
Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.	Reinstall the **stdole32.tlb** file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.) **Windows NT:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter> **Windows 2000:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter> **Windows XP:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter>
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.
Path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters.
If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the **\quartus\bin** directory.	You must share the **quartus** directory, not the **\quartus\bin** directory.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the **Services Control Panel** (Start menu) before running the Quartus II software.

Issue	Workaround
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.	The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the **Reset All** button on the **Toolbars** page of the **Customize** dialog box (Tools menu), or, if the user interface does not appear, type the following command at a command prompt: `quartus -reset_desktop` <Enter>
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "`JTAG Server -- internal error code 82 occurred`" when you click the **Add Hardware** button in the **Hardware Setup** dialog box (Edit menu). This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the **jtagserver.exe** program and at a command prompt for that directory, type `jtagserver --install` <Enter>
If you choose to uninstall a previous version of the Quartus II software during installation, and there is a "locked" file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.	Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.
The Quartus II software version 4.1 does not allow a parallel port T-Guard (dongle) to be used on the same parallel port as a ByteBlaster II download cable.	Use another download cable, such as a USB-Blaster or MasterBlaster to configure your device, or use separate parallel ports for the T-Guard and the download cable. The Quartus II programmer is not a licensed feature, so you can remove the T-Guard to program your device, but you must replace it to use any other Quartus II software features.
Clicking on the internet links in the Quartus II interface, or choosing any subcommand from the **Altera on the Web** command (Help menu) may cause the Quartus II software to close without warning.	Use an external browser to view the Altera web site.
If you are running the Quartus II software on Windows with a country setting that uses the comma (,) as the decimal point, instead of the period (.), you may encounter unexpected results when performing arithmetic functions in the Tcl Console window.	

Issue	Workaround
During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, an Explorer window may appear.	Close the Explorer window before proceeding with the installation.

Solaris, HP-UX & Linux

Issue	Workaround
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.	To display the hidden windows, choose **Cascade** (Window menu).
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the **Internet Connectivity** page of the **Options** dialog box (Tools menu). If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
If you cannot access the Quartus II online Help in the user interface, you can access it by typing `hh quartus.chm` <Return> at a command prompt.	
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at **www.hummingbird.com** for a patch for the Exceed software.
If you are running the Quartus II software version 4.0 on a Linux or Solaris workstation, even though **Reopen current project and files at startup** is turned on, the last project is not reopened when you restart the software.	Use the **File/Project 1, 2, 3, ...** command (File menu) to reopen your last project.

Issue	Workaround
The stand-alone Quartus II Programmer and SignalTap programs are not available on Solaris, Linux, and HP-UX workstations.	
If you double-click or click and hold on drop-down list boxes in the Resource Property Editor, the Quartus II software may crash.	
When you are changing values in the Resource Property Editor, you must press the Return key to apply the changed values.	

Solaris Only

Issue	Workaround
The **ARM-based Excalibur MegaWizard Plug-In**, which is available from the **MegaWizard Plug-In Manager** requires the Java Runtime Environment (JRE), which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for the JRE to function properly.	Check the web site **http://sunsolve.sun.com/pub-cgi/show.pl?target=patches/J2SE** for information about any patches that might be needed.
The **Copy** command (Edit menu) is not functional in Report Window chart pages and RTL Viewer and Technology Map Viewer schematic pages.	
On certain Solaris 8 systems, the position and size of the Help window are not maintained when the Quartus II software is closed and then started again.	Install Solaris OS patch 109147-12 or higher to regain the normal Help functionality.

HP-UX Only

Issue	Workaround
The instructions in the *Installation & Licensing manual for UNIX & Linux Workstations* to mount and install the ModelSim-Altera software from the CD-ROM are incorrect.	Type the following commands at a command prompt: `mkdir /mnt` <Return> `pfs_mountd&` <Return> `pfsd&` <Return> `pfs_mount /dev/dsk/`<*device name of cdrom*> `/mnt`<Return> For example: `pfs_mount /dev/dsk/c0t0d0 /mnt` <Return> After installation is complete unmount the CD-ROM with the following command: `pfs_umount /mnt` <Return>
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: **/etc/passwd** and **/etc/group**.
Programming EPC16 configuration devices is disabled on HP-UX workstations.	

Linux Only

Issue	Workaround
If the MasterBlaster™ download cable is not listed in the **Available hardware items** list in the **Hardware Settings** tab of the **Hardware Setup** dialog box, but it is connected properly, you may not have read/write permission for the serial (`dev/ttyS`*x*) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the "`uucp`" group, or by giving read/write permission for the serial port to everyone, using the following command: `chmod o+rw /dev/ttyS`*x* where *x* is the serial port affected.
If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the `QUARTUS_MWWM` environment variable to `allwm` and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: `setenv QUARTUS_MWWM allwm` <Return> `quartus -no_splash` <Return>

Issue	Workaround
If you double-click or click and hold on drop-down list boxes in the Resource Property Editor, the Quartus II software may crash.	
Under certain circumstances, the Quartus II software may not start properly.	On a system with a static IP address, ensure that the **/etc/hosts** file has an entry for the hostname of the machine on which you are running. For example, if the workstation is named "orange," there should be an entry in **/etc/hosts** with the IP address of the "orange" workstation as shown below: <*IP address of orange*> `orange` In addition, the network configuration (hostname, DHCP hostname, DNS search path, and domain names) must be correct or the Quartus II software will abort on start up.
If you are running the Quartus II software version 4.0 using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.	Make sure your VNC server software is version 3.3.4 or later.
If you are running the Quartus II software under Red Hat Linux 7.3, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.	Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following URL for more information: **http://www.netapp.com/tech_library/3183.html**
If you select a node in the Timing Closure Floorplan, and select **Locate** in the Resource Property Editor (right button pop-up menu), and then select **Goto Source Node** (right button pop-up menu), the Quartus II will not display the entire, hierarchical node name.	

Device Family Issues

Excalibur

Issue	Workaround
You may receive the message "`System Build Descriptor File missing parameter programming clock frequency`" for System Build Descriptor Files (**.sbd**) generated in the Quartus II software version 2.0 and earlier, after selecting the **Boot from Serial** option in the **ARM-based Excalibur MegaWizard Plug-In**.	Rerun the **ARM-based Excalibur MegaWizard Plug-In** in the current version of the Quartus II software to regenerate the SBD File and correct the error.
If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software: **Remove Redundant Logic Cells** **Perform WYSIWYG Primitive Resynthesis** Please refer to the EPXA10 Device Errata Sheet for details on the device errata.	To avoid bridge lock-up, ensure that the **Remove Redundant Logic Cells** option is turned off for the project. If the **Perform WYSIWYG Primitive Resynthesis** option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the **MegaWizard Plug-In Manager** in the Quartus II software version 2.2 or later. This procedure will create an additional settings file (**alt_exc_stripe.esf**) to ensure that the required logic elements are implemented.

Issue	Workaround
Designs targeting Excalibur devices that use Boot-from-Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.	The Excalibur boot loader in the Quartus II software version 3.0 does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the **makeprogfile** utility during the software build process does not work with this version of the bootloader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the **makeprogfile** utility at the command line with the `–nc` (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the \<***XA dev kit instalationl directory***>**\bin** folder. Modify line 1034 of this script to remove the `-nc` option. For example, line 1034 should be changed as shown in this example. `$command = "makeprogfile –nc -b ${fileBase}_bootdata.o $SBD $SBI ${fileBase}.hex";` You must recompile your software project for this change to take effect.
If you are developing new designs with the XA MegaWizard, you should manually import the file settings from the **<*block_name*>.esf** file into the Quartus Settings File (**.qsf**) using the **Import Assignments** command (Assignments menu). This ensures that the Quartus II software does not remove certain cells and uses the inverting input on the stripe interface, which does not work.	

Cyclone, Stratix & Stratix GX

Issue	Workaround
When you use a Routing Constraints File (**.rcf**) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.	
If you use the SignalProbe™ feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.	The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.
In the **SignalProbe Source to Output Delays** table of the Timing Analyzer Report, the following right-button menu commands are not available although they are available in other similar Timing Analyzer Report tables: • **List Paths** • **Locate in Chip Editor** • **Locate in Timing Closure Floorplan** • **Locate in Last Compilation Floorplan**	You can use other Timing Analyzer Report tables to list and locate the affected paths.
If your design targets a Cyclone, Stratix, Stratix GX or MAX II device, and has the Auto Packed Registers option set to Auto, you may receive the following error message if you back-annotate to Logic Cells, and compile the design again: `Error: Can't split carry or cascade chain crossing` <*number*> `logic cells …`	Perform either of the following steps: • Save the post-fitting netlist as a Verilog Quartus Mapping file (**.vqm**) and use the VQM for subsequent compilations. *or* • Select the logic cells listed in the error message and remove all location assignments from those logic cells.

Stratix and Stratix GX

Issue	Workaround
If you use the `altddio_bidir` or `alt_dqs` megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.	

Issue	Workaround
The behavior of the 0-degree phase shift setting of the `DLL_PHASE_SHIFT` parameter of the `altdqs` megafunction or the **DQS Phase Shift** logic option with the `altddio_bidir` megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.	If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2, you should contact the Altera Applications department for further information.
Updated the previously final timing model for Stratix and Stratix GX devices to address inaccuracies in the output buffer timing (t_{CO}, tpd). The changes made to the I/O timing model to correct the output buffer timing will have a small impact on the input buffer timing (t_{SU}, t_H) as well. The core timing model is accurate and was not modified.	For more information, please contact your Altera Support Representative

Stratix

Issue	Workaround
Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.	
Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.	Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.

Changes to Stratix PLL Timing:

Enhanced PLL Maximum VCO Frequency (MHz)			
Speed Grade	**-5**	**-6**	**-7**
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	800	800	800
Quartus II Ver. 2.2 SP1	800	800	600

Fast PLL Maximum VCO Frequency (MHz)			
Speed Grade	**-5**	**-6**	**-7**
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	840	840	840
Quartus II Ver. 2.2 SP1	1000	1000	700

For Enhanced PLLs (EPLLs):

The Quartus II software version 2.2 SP1 and later will enforce the 300–800 MHz maximum VCO frequency range as specified in the Stratix device family data sheet for -5 and -6 speed grades. The PLL VCO frequency range for the -7 speed grade is 300–600 MHz.

For Fast PLLs (FPLLs):

The Quartus II software version 2.2 SP1 and later will continue to support the 300–1000 MHz PLL VCO frequency range when the FPLL is used as a general purpose PLL. The higher PLL VCO frequency range enables more flexibility in choosing multiplication and division factors in the Quartus II software. When the FPLL is used in Source Synchronous mode, the PLL VCO frequency range is unchanged from the data sheet specification of 300–840 MHz.

Stratix GX

Issue	Workaround
When using the `altlvds_tx` or `altlvds_rx` megafunction to set up a PLL with a Stratix II device, the default setting for all clocks, including core clocks and SERDES clocks, will be -180 degrees (with respect to the data rate frequency) compared to the input clock, which is required for legal SERDES operations. The `altlvds_tx` or `altlvds_rx` megafunction will automatically add this phase offset.	

Stratix II

Issue	Workaround
Back-annotating some designs targeted to a Stratix II device with the **Demote cell assignments to** option set to **LABs** may prevent the design from fitting.	Back-annotate the design with **Demote cell assignments to** turned off.

Issue	Workaround
If you are compiling a design for a Stratix II device that was originally targeted to a Stratix device, you may receive the following error message from the **quartus_map** executable if the design uses PLLs that have external clock outputs: `"Info: Messages issued during the elaboration of <`*design entity*`> Error: PLL pll uses extclk[2] output clock port, which cannot be remapped to clk port because target device does not have enough available clk ports."`	Enhanced PLLs on Stratix II devices have fewer output taps than Enhanced PLLs on Stratix devices. Therefore, you must reduce the number of taps on that PLL. If two taps have exactly the same configuration including their enables, you can merge them into a single tap. You must reinstantiate the PLL in your source code with the **MegaWizard Plug-In Manager**, and recompile the design.

Cyclone

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The Cyclone EP1C3T100 device does not support the **LVDS** I/O standard on any pins.	Use the Cyclone EP1C3T144 device instead. It supports the **LVDS** I/O standard.
The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).	Recompile your design after installing the current version of the Quartus software.
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

Cyclone II

Issue	Workaround
Back-annotating some designs targeted to a Cyclone II device with the **Demote cell assignments to** option set to **LABs** may prevent the design from fitting.	Back-annotate the design with **Demote cell assignments to** turned off.

HardCopy Stratix

Issue	Workaround
The pin table shown in the Quartus II online Help for the HC1S40F780 HardCopy Stratix device incorrectly shows pins U12 and U18 as user I/O.	These pins are factory test pins and should be connected to `GND`. Select the EP1S40_HardCopy_Prototype when compiling for this device.
When targeting HardCopy Stratix devices, the Quartus II software discards floating LogicLock regions of size [1,1] (including Auto-size regions with default dimensions) and may generate an internal error when processing LogicLock Regions containing RAM.	Ensure that floating regions are of size greater than [1,1] and use location assignments for RAMs instead.

Design Flow Issues

Verification

Issue	Workaround
If you select **SignalTap II: pre-synthesis** or **SignalTap II: post-fitting** in the **Filter** list of the Node Finder and select a bus to add to the STP File, the Quartus II software may expand the bus into individual nodes that may be removed during synthesis, resulting in an error.	Delete the nodes and recompile the project. You can select individual nodes in the Node Finder and group them in the SignalTap II window using the **Group** command (Edit menu).
Incremental routing may fail for nodes assigned to the SignalTap Logic Analyzer if you have turned on any of the Physical Synthesis Fitter optimizations, such as **Perform physical synthesis for combinational logic** or **Perform register duplication** or **Perform register retiming**.	

Issue	Workaround
Advanced Trigger Conditions for the SignalTap Logic Analyzer are not available on UNIX platforms. If you edit on a UNIX workstation an instance of the SignalTap Logic Analyzer that was created on a PC, the advanced trigger condition will not be changed.	
If you instantiate multiple VHDL instances of the SignalTap Logic Analyzer with the MegaWizard Plug-In Manager, you may receive error messages at compilation similar to this example: "`Error: VHDL error at sld_signaltap.vhd(<number>): formal parameter <name> must have actual or default value.`"	Choose another language, such as Verilog HDL.

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
The Quartus II software version 4.0 and later may give the message "`Error: Duplicate entity <name> found in file <filename1> colliding with the one found in file <filename2>`," for a project that compiled successfully with Quartus II 2.2 or earlier.	The Quartus II software gives an error message when it finds two or more entities with the same name. To avoid this error in the future, remove the duplicate entity or entities. If you cannot remove the duplicate entity, you can direct the Quartus II software to ignore the duplication by adding `set_global_assignment -name IGNORE_DUPLICATE_ASSIGNMENT ON` to your QSF file. Altera recommends that you avoid using this workaround if possible.

Verilog HDL Integrated Synthesis

Issue	Workaround
Verilog-2001 mode is enabled by default. This mode can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as `config`.	Do not use Verilog-2001 reserved words as identifiers or select **Verilog-1995** on the **Verilog HDL** input page under **HDL Input Settings** of the **Settings** dialog box (Assignments menu).

Issue	Workaround
Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single-bit component port named `\my_vector_port[3:0]`, the Quartus II software versions 2.1 and later will treat it as an array port.	You should avoid using escaped port names in the Quartus II software version 2.1 and later.
Some designs that compiled successfully in the Quartus II software version 3.0 may fail with the error message "`Value cannot be assigned to input <`*name*`>`."	The Quartus II software version 4.0 and later does not allow an assignment to an input. Change the port to be an output.
Some designs that compiled successfully in the Quartus II software version 3.0 may fail with the error message "`Index Z cannot be outside range (x to y) of array <`*name*`>`."	The Quartus II software version 4.0 and later does not allow out-of-bounds array accesses. The Quartus II software version 3.0 would return "`don't care`." You must rewrite your design to keep array accesses within the valid range of the array.

SOPC Builder Issues

Issue	Workaround
If the Quartus II software is installed in a directory having space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.
When adding an Excalibur Stripe component in conjunction with Avalon peripherals, you may encounter SOPC Builder errors indicating too many masters are present.	If the master-connection patch-panel is not visible, choose **Show Master Connections** (View menu). Then click on the master/slave intersection indicated by the error message. This will remove the connection. Click again to restore the connection and the error will not reappear.

Issue	Workaround
Designs targeting Excalibur devices that use Boot From Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.	The Excalibur boot loader in the Quartus II software version 3.0 and later does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the **makeprogfile** utility during the software build process does not work with this version of the bootloader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the **makeprogfile** utility at the command line with the `–nc` (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the \<***XA dev kit install directory***>**\bin** folder. Modify line 1034 of this script to remove the `-nc` option. For example, line 1034 should be changed as shown in this example. `$command = "makeprogfile –nc -b ${fileBase}_bootdata.o $SBD $SBI ${fileBase}.hex";` You must recompile your software project for this change to take effect.
The SOPC Builder and Nios Software Development Kit shell may "hang" and become unresponsive when run while the Frisk antivirus software is running.	Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios SDK shell.

SOPC Builder Compatibility

Nios version 3.1 and later

You can use your existing Nios components and they will be recognized automatically by the SOPC Builder integrated into the Quartus II version 4.0 software.

Nios version 2.2 / SOPC Builder 2.7

Your Nios components are not compatible with the SOPC Builder integrated with the Quartus II version 3.0 software. You will receive upgraded Nios components as part of a new Nios Development Kit. You can run your earlier version of SOPC Builder by following these steps:

1. If Altera SOPC Builder 2.7 is not shown in the **MegaWizard Plug-In Manager**, reinstall the SOPC Builder version 2.7 software, or copy the **sopc_builder_2_7_wizard.lst** file into your **\quartus\libraries\megafunctions** directory.

2. When you open a system that uses the Nios version 2.2 embedded processor, you will be given the choice of using the Altera SOPC Builder or the Altera SOPC Builder 2.7. Choose the 2.7 version. If you choose the version without a number (version 3.0) your components will be disabled.

EDA Integration Issues

Issue	Workaround
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
The directory containing the ARM-based Excalibur stripe models changed in the Quartus II software version 2.0. This change may cause compilation scripts that were created for earlier versions of the Quartus II software to fail.	Edit your compilation scripts so that the models and simulation wrapper files are located in the following directory: **\ <*Quartus II installation*>\eda\sim_lib\ excalibur\stripe_model_<*operating system*> \ModelGen\models\epxa<*1 | 4 | 10*> \r0\<*simulator_language*>**
Support has been added for generation of IBIS Output Files (**.ibs**) for EPCS1 and EPCS4 Serial Configuration Devices.	The IBIS file will be generated in the **\<*project name*>\board\ibis** directory after compilation when the design is targeted to a Cyclone device and Active Serial configuration scheme using EPCS1 or EPCS4 devices is chosen.
A Synplicity VQM project that compiles successfully in the Quartus II software version 3.0 or earlier may fail when compiled with the Quartus II software version 4.0 and later with errors "`Port A_IN does not exist in primitive` <*PRIM*> `of instance` <*inst_name*>" and "`Port A_OUT does not exist in primitive` <*PRIM*> `of instance` <*inst_name*>"	This error can occur if your Quartus II project specifies that the Synplicity-generated VQM is a Verilog HDL file. Change the file type of the VQM to Verilog Quartus Mapping File in the **Properties** dialog box of the **Files** page of the **Settings** dialog box (Assignment menu)

Issue	Workaround
NativeLink support does not work with versions of Precision RTL Synthesis Software earlier than version 2003b due to a change in Precision's project interface.	
The ModelSim – Altera software is not compatible with the new USB Software Guard.	Use the Parallel Port software guard or a FLEXlm shared license.

Simulation Model Changes

altera_mf Models

RAM Models

Model	Change
altsyncram	• Added support for Cyclone II
dcfifo	• Added support for showahead speed mode and showahead area mode

DSP Models

Model	Change
altmult_add	• Added support for Cyclone II. • Added support for 18 bit inputs when saturation and rounding feature are used.
altmult_accum	• Added support for Cyclone II. • Added support for 18 bit inputs when saturation and rounding feature are used

I/O Models

altpll	• Added support for Cyclone II. • Added support to handle the large clk*multiply_by and clk*divide_by numbers that are generated by the wizard when you select the clk*_output_frequency method of defining output clock frequency, instead of defining the ratios.
altlvds_tx	• Added support for -180 degrees phase shift on PLL serial clock. • Fixed simulation halt issue under x1 mode and x2 mode when inclock period is set to 0.
altlvds_rx	• Added support for -180 degrees phase shift on PLL serial clock • Fixed simulation halt issue under x1 mode and x2 mode when inclock period is set to 0.

Notes:

The ModelSim software version 5.8 gives the following warning when **altera_mf** or **220models** megafunction models are compiled with the -87 option:

```
#** Warning (vcom-1148) Condition in IF GENERATE must
be static
```

You can safely ignore this warning because under the 1987 rules, the constant is not considered to be static because of the initialization from the function call.

RAM Megafunction models only support HEX format for all 3rd-party simulators. Manually convert MIF format to HEX first in the Quartus II software.

Latest Known Quartus II Software Issues

For known software issues after publication of this version of the Quartus II Software Release Notes, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Knowledge Database at the following URL:
http://answers.altera.com/altera/index.jsp?/Topics/Support Solutions/Known Issues/Software/Quartus II