Quartus II Software Release Notes

July 2003 **Quartus II version 3.0**

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **quartus** directory.

New Features & Enhancements

The Quartus II software version 3.0 includes the following new features and enhancements:

- New I/O assignment analysis allows you to validate your I/O assignments before compiling the design
- New Chip Editor feature to make incremental design changes easily
- Incremental fitting feature for small design changes reduces compilation time while maintaining timing closure
- Updated Assignment Editor now supports all device families and provides increased functionality and usability
- New design space explorer script provides an automated method to increase design performance by performing compilations using varying optimization settings
- Enhanced LogicLock™ methodology to lock down routing as well as placement
- Support for HardCopy Stratix™ mask-programmed devices
- Support for MAX® 7000S, MAX 3000A, FLEX® 10K, and FLEX 10KA device families
- Enhanced command-line operation with simplified Tcl scripting and makefile support
- Support for Red Hat Linux 8.0
- Timing-driven Compilation includes enhancements in the following areas:
  - Automatically optimizes I/O hold times by adding delays to paths in order to satisfy hold time requirements for those paths
  - Optimizes user-specified timing constraints (for example; clock period, t_{SU}, t_{CO}, and t_{PD}). Clocks and paths without any user-specified constraints will not be optimized.
  - In the absence of any user-specified timing constraints, timing-driven compilation only focuses on maximizing the slowest clock in the design and does not optimize I/O timing paths.
  - The Quartus II software displays information messages to communicate what the timing-driven compilation is focusing on.
- New Physical Synthesis Tools, including register duplication and register retiming, extend the existing Fitter Netlist Optimizations.

Device Support & Pin-Out Status

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
MAX 7000S	EPM7032S	EPM7064S
	EPM7128S	EPM7160S
	EPM7192S	EPM7256S
MAX 3000A	EPM3128A FC256	EPM3256A FC256
FLEX 10K	EPF10K10	EPF10K20
	EPF10K30	EPF10K40
	EPF10K50	EPF10K70
FLEX 10KA	EPF10K10A	EPF10K30A
	EPF10K50V	EPF10K100A
Stratix™	EP1S10	EP1S20 F484
	EP1S40	EP1S60
	EP1S80 F1020	
Stratix™ GX	EP1SGX25ES	EP1SGX40ES
Cyclone™	EP1C3	EP1C6
	EP1C12	EP1C20
HardCopy Stratix	HC1S25	HC1S30
	HC1S40	HC1S60
	HC1S80	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Cyclone	EP1C4F324	EP1C4F400

Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
None	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	Notes
Stratix GX	EP1SGX10	
	EP1SGX25	
	EP1SGX40	
Cyclone	EP1C3	
	EP1C4	
	EP1C12	

No changes have been made to preliminary timing models for this version of the Quartus II software.

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
APEX™ II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
APEX™ 20KC(1)	EP20K200C	2.0 SP1
	EP20K1000C	2.0 SP1
Cyclone	EP1C6	3.0
	EP1C20	3.0
Excalibur™	EPXA1	2.0 SP2
	EPXA4	2.0 SP2
	EPXA10	2.0 SP1
FLEX 10K	All	3.0
FLEX 10KA	All	3.0
Mercury™(1)	EP1M120	2.1 SP1
MAX 3000(1)	EPM3512A	2.1 SP1
MAX 7000(1)	EPM7512B	2.1 SP1
MAX 7000S	All	3.0
Stratix	EP1S10	2.2 SP2
	EP1S20	2.2 SP2
	EP1S25	2.2 SP2
	EP1S30	2.2 SP2
	EP1S40	2.2 SP2
	EP1S60	3.0
	EP1S80	3.0

(1) Timing models for devices in this device family not listed here became final in versions 2.0 and earlier.

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX 20KE, FLEX 6000, and the FLEX 10KE device families. Final timing models for these device families became final in versions earlier than version 2.0.

EDA Interface Information

The Quartus II software version 3.0 supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink® support
Mentor Graphics® LeonardoSpectrum™-Altera	2002f	✓
Mentor Graphics® LeonardoSpectrum™	2003b	✓
Synopsys Design Compiler	2002.02	
Synopsys FPGA Compiler II	3.7	✓
Mentor Graphics Precision RTL Synthesis	2003a	✓
Synplicity Synplify and Synplify Pro	7.3	✓
Aplus Design Technologies (ADT) PALACE™	2.3	✓
Verification Tools	**Version**	**NativeLink support**
Cadence NC-Verilog	5.0	✓
Cadence NC-VHDL	5.0	✓
Cadence Verilog-XL	3.3	
Model Technology™ ModelSim®	5.7c	✓
Model Technology ModelSim-Altera	5.7c	✓
Mentor Graphics BLAST	1.2.2	
Synopsys PrimeTime	2003.03 SP1	✓
Synopsys Scirocco	2002.06	✓
Synopsys VSS	2000.05	
Synopsys VCS	7.0	
Mentor Graphics Tau	2.2	
Verplex Conformal LEC	3.4.0.a	

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
The Quartus II software no longer uses the registry to store non-user interface-related settings. Non-user interface-related settings are stored automatically in the **quartus2.ini** file when you open the Quartus II software user interface for the first time.	You must open the Quartus II software user interface at least once before using the command-line version of the software.
Versions of the Quartus II software earlier than version 3.0 cannot open Block Design Files (**.bdf**) created with the Quartus II software version 3.0 and later.	You can alter the BDF so that it can be opened in earlier versions, but location information will be lost. 1. Open the BDF in any text editor (vi, emacs, notepad). 2. Change the version from `1.3` to `1.2` in the header section. 3. Remove all the lines with string "`location`," for example: `(annotation_block (location)(rect -336 -40 -248 -8))`. 4. Save the file.
Changes made in the Assignment Editor are saved only when you choose **Save** (File menu). If you have turned off the **Save changes to all files before starting a compilation, simulation, or software build** option on the **Processing** page of the **Options** dialog box (Tools menu), changes you made in the Assignment Editor may not be reflected in the latest compilation.	Turn on the **Save changes to all files before starting a compilation, simulation, or software build** option on the **Processing** page of the **Options** dialog box (Tools menu). *or* Chose **Save** (File menu) after making any changes in the Assignment Editor
Not all speed grades of a given device share the same features.	Refer to the Altera data sheet for the device family for further information.
The default setting for the **Power-Up Don't Care** logic option has been changed to **On** in the Quartus II software version 2.1 Service Pack 1 and later.	

Issue	Workaround
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
To use the EP20K400GC655 device in your design, please contact the Altera Customer Applications Department.	
If you have a version of the Quartus® software earlier than the Quartus II software version 1.0 installed on your computer in addition to the Quartus II software, you can start the previous version of the program only by running the **runq.exe** program from the **\quartus\bin** directory that contains the earlier version you wish to use.	
You should not create multiple Compiler settings that have the same design entity as the "compilation focus."	
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, choose **Index** from the Help menu and type the name of the item.

Issue	Workaround
For APEX 20KE devices, the Quartus II software provides limited support for the following I/O standards that are not available with the **I/O Standard** logic option: • **LVPECL** is a differential I/O standard that is similar to the **LVDS** I/O standard. APEX 20KE devices can support LVPECL I/O pins by using the I/O pins in LVDS mode with an external resistor network. • **PCI-X** is an enhanced version of the **PCI** I/O standard that can support a higher average bandwidth. This standard has more stringent requirements than PCI.	To use the **LVPECL** I/O standard in APEX 20KE devices in the Quartus II software, set the **I/O Standard** logic option for the pins to **LVDS** and connect the pins to an appropriate external resistor network. The APEX 20KE I/O drivers meet the requirements for **PCI-X**. Turn on the **PCI I/O** logic option to support PCI-X requirements, including the overshoot clamp.
You cannot locate the source of an error in a design file if compilation was unsuccessful due to a syntax error.	
If you open a project that was created using an earlier version of the Quartus II software, you may receive a message that indicates that the database is incompatible and that results of the last compilation will be lost.	To maintain existing placement information and optionally routing information, back-annotate all of the project assignments in the earlier version. You may also need to generate a Quartus II Verilog Mapping file (**.vqm**) netlist to preserve the result of Physical Synthesis.
The Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the **Group** command (Edit menu) to create groups of arbitrary nodes.
If you are using the `altcam`, `altclklock`, `altlvds_rx`, or `altlvds_tx` megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Last Compilation floorplan.
The Quartus II software does not support file names with more than one extension. For example, you cannot use the file name **file.eda.edif**.	Use file names with only one extension.

Issue	Workaround
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (`debug[7..0]`), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "`Unsupported data type in the top-level module.`"	Reserve the pins using single name notation (for example, `debug7`, `debug6`, and so on).
The Quartus II software versions 2.1 and later supports only version 5.2 and later of the Altera PowerKit™ software. Previous versions of the PowerKit software are not supported with these versions of the Quartus II software.	
If you are using the **HSTL Class II** I/O standard with an APEX II device, additional information is required.	Contact the Altera Customer Applications department at **apexii@altera.com** for information about Service Packs and device pin-outs.
Do not change the file permissions (such as changing "read-only" to "read and write") of Quartus II settings and configurations files (**.csf**, **.esf**, and so on) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
The order of ports for the **ARM®-based Excalibur MegaWizard® Plug In**-generated symbol for the stripe changed in version 2.0 of the Quartus II software. If you re-run the **MegaWizard Plug-In Manager** (Tools menu) for a design created in a version of the Quartus II software earlier than version 2.0, you will receive port connection errors when you compile the design.	To avoid receiving these errors, adjust the port connections in the BDF after updating the symbol.
Node names containing numbers greater than 2^31-1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.

Issue	Workaround
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (**.pof**) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
The Quartus II software versions 2.1 and later no longer support the Compiler Settings File (**.csf**) `MIGRATION_DEVICES` variable.	In order to specify migration device names in the CSF, use the `DEVICE_MIGRATION_LIST` variable. For example: `DEVICE_MIGRATION_LIST = "DEVICE_A,DEVICE_B,DEVICE_C";`
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the CSF or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the **Assignment Editor** (Assignments menu) or by manually editing the CSF.	If you experience a "no fit" or an Internal Error while using routing back-annotation, delete the Routing Constraints File (**.rcf)** and back-annotate the design again after a successful compilation.
After register duplication has occurred, the duplicated register has a unique name in the form <*original name*>~<*suffix*>. The new register name may not properly inherit timing assignments made with wild cards.	Make sure that duplicated register names are included in your wild card match when making timing assignments.
You may receive an "`invalid command name`" error when you run an existing Tcl script that uses the Tk toolkit for its user interface. Beginning with the Quartus II software version 2.2, the Quartus II software no longer initializes the Tk toolkit automatically when starting any process.	Add the Tcl command "`init_tk`" to the beginning of any Tcl script that uses Tk
The **lpm_fifo MegaWizard Plug-In** has been removed from the Quartus II software version 2.2. The `lpm_fifo` megafunction is still included for backward compatibility with older designs.	Altera recommends that you use the **lpm_fifo+ MegaWizard Plug-In** for all new designs requiring single-clock FIFO functions.

Issue	Workaround
If you receive an error message saying "`System resources low...`" or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.	You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and choose **Clear Messages from Window** (right button pop-up menu). Additional memory can be recovered by closing the Floorplan Editor.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus Workspace File (**.qws**) **<*project name*>.qws** from the project directory. If the problem persists, delete the **<*project directory*>\db** directory.
When you are setting phase shift and duty cycle values for clock signals using the `altpll` megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.

The **Use Fitter Timing Information** setting has been removed from the **Netlist Optimizations** page of the **Settings** dialog box (Assignments menu) in the Quartus II software version 3.0.	The Quartus II software version 3.0 supports this netlist optimization setting only in the form of a flow. This flow is called the two-pass optimization flow. You can run this with the following command-line command:
	`quartus_sh –flow two_pass_optimization` <*project*> `[-c` <*csf/ssf*>`]` <Enter>
	It can also be embedded in a Tcl script run using the following command:
	`quartus_sh -t your_script.tcl` <Enter>
	The Tcl script named **your_script.tcl** should then contain the following commands:
	`package require ::quartus::flow`
	`project_open` <*project*>
	`execute_flow -two_pass_optimization`
	`project_close`

Issue	Workaround
During compilation or simulation, the Quartus II software may "hang" and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes its execution.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.
The global **Preserve Hierarchical Boundary** logic option assignment has been removed from the user interface in the Quartus II software version 3.0.	If you need to set the **Preserve Hierarchical Boundary** logic option to **Firm**, you can do so on an entity-by-entity basis with the Assignment Editor, or you can use the following Tcl command to make the assignment: `set_global_assignment -entity <entity_name> -name PRESERVE_HIERARCHICAL_BOUNDARY FIRM`
Running individual Quartus II software executables (**quartus_map**, **quartus_fit**, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	You should run individual executables either from within the Quartus II scripting shell (**quartus_sh**) or directly at a command prompt.
If you have chosen migration devices in the **Compatible Migration Devices** dialog box, which is available from the **Device** page in the **Settings** dialog box (Assignments menu), the Timing Closure Floorplan and the Last Compilation Floorplan will display only the pins and PLLs that are common to all the selected devices. However, the Chip Editor will display all the pins and PLLs available for the device specified for compilation.	
Under certain circumstances, if you remove LogicLock assignments with the **Remove Assignments** dialog box (Assignments menu), the assignments will not be removed from your project.	Use the **LogicLock Regions** window (Assignments menu) to remove LogicLock assignments.
When specifying an entity name in the Look in box in the Node Finder, the case of the entity name must match the case of the Compilation focus entity name and the actual design file entity name.	

Issue	Workaround
The online Help for Minimum Timing Analysis does not describe the device families that support this feature.	Minimum Timing Analysis is supported for the following device families: APEX 20KE, APEX 20KC, APEX II, Mercury, Stratix, Stratix GX, Stratix HardCopy.
Changing devices while the critical path(s) are shown in the Timing Closure Floorplan can cause the Quartus II software to crash.	Turn off the **Routing > Show Critical Paths** option (View menu) before changing devices for compilation.
IP licenses that were issued earlier than June, 2002 will not work in the Quartus II version 3.0 software.	Licenses that will work contain a "`SIGN =`" portion in the feature line. If the Feature line for your IP does not contain a "SIGN =" portion, then you must obtain a new license from Altera by logging onto **www.altera.com/support/licensing/ip/lic-ipm-purchased.jsp**
If you import LogicLock regions after running the **HardCopy Files** wizard (Project menu), the Quartus II software may crash.	Import any LogicLock regions (or other entity settings) before running the **HardCopy Files** wizard. *or* Close, then reopen your project in the Quartus II software before importing LogicLock regions or other settings.
Under certain circumstances, the Quartus II software may crash if you change device after compiling your design but before opening the Resource Property Editor.	Be sure to change back to the last device you specified for compilation before opening the Resource Property Editor.
Turning **Physical Synthesis** on in the Netlist Optimizations page of the Settings dialog box on average will cause compilation time to double and peak memory usage to increase by approximately 20%. For large designs, the Progress Bar for the Fitter may appear to be stuck in the 50-70% range while the elapsed time continues to increase. Provided that compilation time has not increased over 10X, this is normal and the compilation should be allowed to finish. In rare cases, the compilation time may increase by more than 10X. In these cases, it is appropriate to apply the workaround if you cannot tolerate such a long compilation time.	If compilation time is excessive with Physical Synthesis turned on, you can either remove or convert LogicLock Regions to "soft" before recompiling, or you can turn off **Physical Synthesis**.

Issue	Workaround

The following Altera megafunctions do not have simulation models in the **altera_mf** library:
`altmemmult`
`altpll_reconfig`
`altremote_update`
`altdqs`
`altclkbuf`
	Add the corresponding **<*device*>_atoms.v** or **.vhd** file to your design for compilation. These files are located in the **\quartus\eda\sim_lib** directory.

Platform-Specific Issues

PC Only

Issue	Workaround
Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.	Reinstall the **stdole32.tlb** file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.) **Windows NT:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter> **Windows 2000:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter> **Windows XP:** <*CD-ROM drive letter*>`:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb` <Enter>
It is possible that one of the Quartus II executable files (**quartus.exe**, **quartus_cmd.exe**, **quartus_swb.exe**, **quartus_dbc.exe**, or **quartus_old_sim.exe**) may not terminate properly after an error.	Use the Windows Task Manager to end the process before running the Quartus II software again.

Issue	Workaround
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.
A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.	To use the Japanese online Help, copy the **quartus.chm** file from the **jhelp** directory of the CD-ROM to your **\quartus\bin** directory.
If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the **\quartus\bin** directory.	You must share the **quartus** directory, not the **\quartus\bin** directory.
If you are running the ZoneAlarm personal firewall software, you may receive a message saying, "`Can't start or continue to run database creator`" when you launch the Quartus II Simulator.	The Quartus II software is not compatible with the ZoneAlarm software. The ZoneAlarm software mistakenly determines that the Quartus II Simulator is accessing the Internet when it uses TCP/IP for its inter-process communication. You must disable the ZoneAlarm software to run the Quartus II Simulator.
Under some circumstances, the Quartus II software crashes when using the "X" button to close the Print Preview window if a project is open.	Use the **Close** button to close the Print Preview window if you have a project open.
If you disconnect your network connection while the Quartus II software is open, you may receive an error message saying "`Can't start or continue to run the db creator`."	Close the Quartus II software before disconnecting the network connection and wait for the "`LAN is disconnected`" message in the Windows Taskbar before restarting the Quartus II software.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the **Services Control Panel** (Start menu) before running the Quartus II software.
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear.	The registry settings controlling the position of the Quartus II windows may have become corrupted. Type the following command at a command prompt: `quartus -reset_desktop` <Enter>

Issue	Workaround
Path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters.
Under some circumstances, the Quartus II software may run correctly the first time it is started after installation, then fail to run with a "`License Not Found`" error thereafter.	If you have specified multiple license servers in either your `LM_LICENSE_FILE` environment variable or on the **License Setup** page of the **Options** dialog box (Tools menu), you must make the license server that serves the Quartus II software license the first server specified on the line.
Opening the Quartus II software by dropping a Quartus II project file (.**quartus**) or Quartus II Archive file (.**qar**) onto a shortcut to the Quartus II software will cause the Quartus II software to crash when the project is compiled.	Start the Quartus II software before opening a Quartus II project file or QAR file.
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "`JTAG Server -- internal error code 82 occurred`" when you click the **Add Hardware** button in the **Hardware Setup** dialog box (Edit menu). This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the **jtagserver.exe** program and at a command prompt for that directory, type `jtagserver --install` <Enter>

Solaris, HP-UX & Linux

Issue	Workaround
The Quartus II Help is not available if you have set either the `MWNO_RIT` or the `MWDONT_XINITTHREAD` environment variables before running the Quartus II software.	Remove the variables from your environment and allow the Quartus II software to set these variables automatically, if needed.
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.

Issue	Workaround
Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.	To display the hidden windows, choose **Cascade** (Window menu).
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the **Internet Connectivity** page of the **Options** dialog box (Tools menu). If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
The **Colors** list in the **Block & Symbol Editor Color Options** page of the **Options** dialog box (Tools menu) or **Format** tab of the **Properties** dialog box (Edit menu) for any object in the Block or Symbol Editors may remain open, and may cause an internal error if you click anywhere else in the Quartus II software before closing the **Colors** list box.	Select a color to close the **Color** list box.
You cannot run the Innoveda BLAST software automatically from within the Quartus II software, even if the **Run this tool automatically after compilation** option is turned on.	Run the Innoveda BLAST software manually outside the Quartus II software.
You cannot run the Mentor Graphics LeonardoSpectrum software from within the Quartus II software even if the **Run this tool automatically after compilation** option is turned on.	Run the LeonardoSpectrum software manually outside the Quartus II software.
You cannot run the Model Technology ModelSim software from the **EDA Tool Post-Compilations Options > Run Simulation Tool** command (Processing menu) from within the Quartus II software.	Run the ModelSim software outside the Quartus II software.
You can access the Quartus II online Help by typing `hh quartus.chm` <Return> at a command prompt.	
If you attempt to exit from the Quartus II software while the Tutorial window is open, the Tutorial window may remain open and may not respond to your commands.	Close the Tutorial window before exiting from the Quartus II software.

Issue	Workaround
When the LogicLock Regions window is floating, you cannot drag and drop node names to it from the Node Finder.	Dock the LogicLock Regions window before dragging node names to it from the Node Finder.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1 or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at **www.hummingbird.com** for a patch for the Exceed software.
Spaces in directory paths or file names used in the Quartus II command-line executables will cause an error.	Rename the file or directory such that it does not contain spaces.
Semicolons in command-line arguments, such as in the following example: `quartus_map -l path1;path2;path3`, will cause an error because the software interprets the arguments as separate commands.	Enclose command-line arguments that use (or require) semicolons (for example, `quartus_map -l` and `quartus_pgm -o`) in quotes. For example, `"quartus_map -l path1;path2;path3"` To intentionally perform multiple commands on a single line, enclose the semicolons in quotation marks. For example: `quartus_sh --tcl_eval puts Hello ";" puts World`
Spaces in command-line arguments, even when enclosed in quotes, such as in the following example `--family="APEX II"` will be seen as two separate arguments and will cause an error. Additionally, the command `quartus_sh --tcl_eval puts "Hello World"` will not work on UNIX or Linux.	The recommended usage in this example is `--family=APEXII`. You can use escaped quotation marks (`\"`) to enclose strings for Tcl, but any whitespace characters within the string will be reduced to a single space. Example: `quartus_sh --tcl_eval puts \"Hello World\"`

Issue	Workaround
Portions of the SOPC Builder may not function correctly if you perform a cross-platform installation (for example, from a Solaris workstation to a Linux workstation).	Install the software from the same platform as that on which you will run it. *or* Type the following command at a command prompt on either platform (note the command must all be on one line): <*path to perl*>/`perl -x` <*path to Quartus II*>`/sopc_builder/bin/regsopc.pl --quartus_root_dir=`<*path to Quartus II*> <Enter>

Solaris Only

Issue	Workaround
The **ARM-based Excalibur MegaWizard Plug-In**, which is available from the **MegaWizard Plug-In Manager** requires the Java Runtime Environment (JRE) version 1.3, which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for JRE 1.3 to function properly.	Check the web site **java.sun.com/j2se/1.3/install-solaris-patches.html** for information about any patches that might be needed.
A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.	To use the Japanese online Help, copy the **quartus.chm** file from the **jhelp** directory of the CD-ROM to your **/quartus/solaris** directory.
If you attempt to exit from the Quartus II software while the Tutorial window is open, the Tutorial window may remain open and may not respond to your commands.	Close the Tutorial window before exiting from the Quartus II software.
If you attempt to use the Excalibur Stripe Simulator (ESS) with the ModelSim software, you may receive an error message saying that the ModelSim software cannot locate the ESS libraries.	Add the following setting to your environment: `QESS_PLATFORM solaris`. In addition, if your designs are in Verilog HDL, you must set your **veriuser** path as follows: `veriuser = $QESS_ROOTDIR/ $QESS_PLATFORM/libess_sspli.so`

Issue	Workaround

If you are running the FLEXlm license server software on a Solaris server, the **alterad** daemon may fail to start and you may receive the following message:
`"Vendor daemon can't talk to lmgrd"`
	Use the following script to start the **lmgrd** daemon:
	`#!/bin/sh`
	`ulimit -n 1024`
	`ulimit -H -n 1024`
	`lmgrd $*`

Launching the SOPC Builder without certain run-time patches to the operating system may cause you to receive a message indicating that it "`Could not create the Java virtual machine`."	Visit the web site at the following URL to determine and download the appropriate patches for your system: **sunsolve.sun.com/pub-cgi /show.pl?target=patches/patch-access**.
If you double-click or click and hold on drop-down list boxes in the Property Resource Editor the Quartus II software may crash.	

HP-UX Only

Issue	Workaround
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: **/etc/passwd** and **/etc/group**.
Attempting to convert your device SRAM Object Files (**.sof**) to Programmer Output Files (**.pof**) for use with a configuration device, such as an EPC2 device, causes the Quartus II software to "hang" when you open the Conversion Setup File (**.cof**).	Create the POF as usual and add it to your project with the **Add Files to Project** command (Project menu).
A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.	To use the Japanese online Help, copy the **quartus.chm** file from the **jhelp** directory of the CD-ROM to your **/quartus/hp11** directory.
Programming EPC16 configuration devices causes the Quartus II software to crash.	

Issue	Workaround
If you float any Utility window (Change Manager, Node Finder, Project Navigator, Status Window, etc.) in the main window with the **Restrict to Main Window** command (right-button popup menu), and then maximize that window after the Report window has been opened, the Quartus II software may crash.	Do not maximize Utility windows after restricting them to the main window.

Linux Only

Issue	Workaround
A Japanese-language version of the online Help file for the Quartus II software version 1.0 is included on the Quartus II software CD-ROM. You can use the Japanese online Help with the current version of the Quartus II software, but not all Help information will be up-to-date.	To use the Japanese online Help, copy the **quartus.chm** file from the **jhelp** directory of the CD-ROM to your **/quartus/linux** directory.
If the MasterBlaster™ download cable is not listed in the **Available hardware items** list in the **Hardware Settings** tab of the **Hardware Setup** dialog box, but it is connected properly, you may not have read/write permission for the serial (`dev/ttyS`*x*) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the "`uucp`" group, or by giving read/write permission for the serial port to everyone, using the following command: `chmod o+rw /dev/ttyS`*x* where *x* is the serial port affected.
This release of the Quartus II software supports the ByteBlaster II and ByteBlasterMV download cables using either Passive Serial or JTAG modes. Although you can generate Jam Files (**.jam**) and Jam Byte-Code Files (**.jbc**), these file types are not supported for device configuration on Red Hat Linux version 7.1. Additionally, the EPC4, EPC8, and EPC16 configuration devices are not supported at this time, and programming times of EPC2 devices may be extremely slow.	For information about using a ByteBlaster II or ByteBlasterMV download cable with the Quartus II software on the Linux operating system, refer to the *Quartus II Installation & Licensing Manual for UNIX and Linux Workstations*, or contact Altera Customer Applications.

Issue	Workaround
If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the `QUARTUS_MWWM` environment variable to `allwm` and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: `setenv QUARTUS_MWWM allwm` <Enter> `quartus -no_splash` <Return>
Running a Tcl script with the Tcl Scripts command or from within the Tcl Console while a process (compilation, simulation, software build) is running in the background can cause the Quartus II software to crash with an internal error.	Run Tcl scripts only when compilation, simulation, or software build processes are not running.
If you double-click or click and hold on drop-down list boxes in the Resource Property Editor the Quartus II software may crash.	
When running the Quartus II software under the Red Hat Linux 8.0 operating system, the **LogicLock Regions Properties** dialog box may not be shown completely.	
When running the Quartus II software under the Red Hat Linux 8.0 operating system, the Insert Symbol dialog box and the MegaWizard Plug-In Manager window cannot be closed using the Window Close (**X**) button in the top right corner.	Right-click on the title bar of the dialog box or window and choose **Close** (right-button pop up menu).
If you float any Utility window (Change Manager, Node Finder, Project Navigator, Status Window, etc.) in the main window with the **Restrict to Main Window** command (right-button popup menu), and then maximize that window after the Report window has been opened, the Quartus II software may crash.	Do not maximize Utility windows after restricting them to the main window.
Under certain circumstances, the Quartus II software may not start properly.	Ensure that the **/etc/hosts** file has an entry for the hostname of the machine on which you are running. For example, if the workstation is named “orange”, there should be an entry in **/etc/hosts** with the IP address of the “orange” workstation as shown below: *<IP address of orange>* `orange`

Issue	Workaround
The Quartus II software may crash if you have the Graphic Editor open on a Block Design File (**.bdf**) and the Programmer open and you type out of range values for **Number of Words** and **Word Size** in the **Number of Words & Word Size** dialog box in the Memory Editor.	Enter positive integers only (no negative numbers or alphabetic characters) in the **Number of Words** and **Word Size** boxes.

Device Family Issues

Mercury

Issue	Workaround
If your Quartus II version 1.0 or 1.1 design for a Mercury device uses the `altlvds_tx` or `altlvds_rx` megafunction, and you archived the design, you may have functional problems in your design, including inverted signals.	Delete the `altlvds_tx` or `altlvds_rx` megafunction from the design and replace it with the version included with the current version of the Quartus II software before compiling your design in the Quartus II software version 2.1 or later.

Excalibur

Issue	Workaround
You may receive the message "`System Build Descriptor File missing parameter programming_clock_frequency`" for System Build Descriptor Files (**.sbd**) generated in the Quartus II software version 2.0 and earlier, after selecting the **Boot from Serial** option in the **ARM-based Excalibur MegaWizard Plug-In**.	Rerun the **ARM-based Excalibur MegaWizard Plug-In** in the current version of the Quartus II software to regenerate the SBD File and correct the error.

Issue	Workaround
If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software: **Remove Redundant Logic Cells** **Perform WYSIWYG Primitive Resynthesis** Please refer to the EPXA10 Device Errata Sheet for details on the device errata.	To avoid bridge lock-up, ensure that the **Remove Redundant Logic Cells** option is turned off for the project. If the **Perform WYSIWYG Primitive Resynthesis** option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the **MegaWizard Plug-In Manager** in the Quartus II version 2.2 software. This procedure will create an additional settings file (**alt_exc_stripe.esf**) to ensure that the required logic elements are implemented.

Cyclone, Stratix & Stratix GX

Issue	Workaround
Inverting the clock signal of a logic cell that has a clock enable signal with the Resource Property Editor when other logic cells in the same LAB share both the clock and clock enable signals will pass the netlist checks run by choosing the **Check and Save All Netlist Changes** command (Edit menu) but may cause the Quartus II software to crash with an internal error in the Assembler.	Invert the clock signal on all logic cells with common clock & clock enable signals. Inverting only one clock signal in the LAB requires that you change your source.
Under certain circumstances, a LogicLock region in the design appears after compilation as a 1 x 1 block in the lower-left corner of the device floorplan.	This problem can occur when both the **Automatically route signal probe signals** option and the **Smart Compilation/More disk space** option on the **Mode** page in the **Settings** dialog box (Assignments menu) are turned on. To prevent this problem from occurring in the future, perform the following steps: Turn off the **Smart Compilation/More disk space** option *or* 1. Turn on the Preserve fewer node names option. 2. Turn off the **Automatically route signal probe signals** option. 3. Recompile your design. 4. Create the desired LogicLock regions.

Issue	Workaround
The Quartus II software may perform register duplication into I/O cells even though you have set the **Netlist Optimizations** option to **Never Allow** for that register.	Turn off the **Auto Packed Registers** option for the affected register.
When you use a Routing Constraints File (**.rcf**) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.	
If you use the SignalProbe feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown "X" in the Quartus II Simulator.	The signal will be correct in actual operation, the error only appears in the Quartus II Simulator.
In the **SignalProbe Source to Output Delays** table of the Timing Analyzer Report, the following right-button menu commands are not available that are available in other similar Timing Analyzer Report tables: • **List Paths** • **Locate in Chip Editor** • **Locate in Timing Closure Floorplan** • **Locate in Last Compilation Floorplan**	You can use other Timing Analyzer Report tables to list and locate the affected paths.
Under certain circumstances, the Quartus II software can crash with an internal error at about 28% complete in the Fitter module.	Open the **LogicLock Regions** window (Assignments menu) and right-click on each LogicLock region that is highlighted in red. Choose **Repair Branch** on the right-button pop-up menu to fix the corrupted LogicLock region. After all corrupted regions are fixed, recompile your design.
The new automatic hold time optimization algorithm may increase your compilation times significantly.	In the **Fitting** page of the **Settings** dialog box (Assignments menu), turn off **Optimize Hold Timing**.
When compiling Stratix, Stratix GX and Cyclone designs with tight t_{SU} requirements, the Quartus II software may choose I/O delay chain settings to meet the t_{SU} constraint such that $t_H = 0$ is not guaranteed at I/Os, if the user had no $t_H = 0$ constraint set on these I/Os.	If your design requires $t_H = 0$ on some or all of the I/Os, you should make appropriate t_H assignments so that the Quartus II software will optimize and analyze them.

Stratix and Stratix GX

Issue	Workaround
Designs that make use of the DQS, Fast Clock, or corner LVDS PLLs in Stratix and Stratix GX devices *and* have back-annotated routing in the Quartus II software version 2.2 or earlier may generate warnings in version 3.0. The warning will indicate that back-annotated routing will be ignored for these connections. As result, the routing for these resources may be different from the routing when compiled with the Quartus II software version 2.2 SP2.	These warnings can be ignored safely. You should back-annotate the routing achieved using the Quartus II software version 3.0 to create a new Routing Constraints file (**.rcf**). Only the routing constraints for DQS, corner LVDS PLL, and fast clocks should change.

Stratix

Issue	Workaround
Versions of the Quartus II software earlier than version 2.2 did not correctly implement the following functions in DSP blocks in Stratix devices: • Mixed sign multiplications of 19 bits and greater • Dynamic sign multiplications of 19 bits and greater • Signed multiplications greater than 36 bits	Designs that implement DSP functions must be recompiled in the Quartus II software version 2.2 or later. The Quartus II software version 2.2 will implement the design correctly, but will use more resources and have reduced performance from earlier versions.
Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.	
Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.	Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.

Changes to Stratix PLL Timing:

Enhanced PLL Maximum Clock Frequency (MHz)			
Speed Grade	**-5**	**-6**	**-7**
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	800	800	800
Quartus II Ver. 2.2 SP1	800	800	600

Fast PLL Maximum Clock Frequency (MHz)			
Speed Grade	**-5**	**-6**	**-7**
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	840	840	840
Quartus II Ver. 2.2 SP1	1000	1000	700

For Enhanced PLLs (EPLLs):

The Quartus II software version 2.2 SP1 and later will enforce the 300–800 MHz clock frequency range as specified in the Stratix device family data sheet for -5 and -6 speed grades. The clock frequency range for the -7 speed grade is 300–600 MHz.

For Fast PLLs (FPLLs):

The Quartus II software version 2.2 SP1 and later will continue to support the 300–1000 MHz clock frequency range when the FPLL is used as a general purpose PLL. The higher clock frequency range enables more flexibility in choosing multiplication and division factors in the Quartus II software. When the FPLL is used in Source Synchronous mode, the clock frequency range is unchanged from the data sheet specification of 300–840 MHz.

Stratix GX

Issue	Workaround
Currently the simulation models provided for the `altgxb` megafunction do not model the power-up condition correctly for simulation in other EDA simulation tools.	You must manually set the `pll_areset` signal to power up high in your test bench or simulation vector file. Refer to “Perform a Functional Simulation...” topics in the “Using Other EDA Simulation Tools” section of the Quartus II Help for more information.

Issue	Workaround
The Quartus II software version 3.0 also supports PowerGauge™ simulation-based power estimation for the Stratix GX device family. The power estimation includes approximately 450 mA for each Stratix GX transceiver block in the design.	

Cyclone

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The Cyclone EP1C3T100 device does not support the **LVDS** I/O standard on any pins.	Use the Cyclone EP1C3T144 device instead. It supports the **LVDS** I/O standard.

APEX II

Issue	Workaround
If you use the `altddio_in` or `altddio_bidir` megafunction and do not connect the `dataout_h` and `dataout_l` ports, you will receive an error message and the design will fail to compile.	Connect the `dataout_h` and `dataout_l` ports.

Design Flow Issues

Verification

Issue	Workaround
Node names for module outputs that are directly connected to inferred objects (counters, and so forth) cannot be added to a SignalTap II File (**.stp**).	To add such node names to an STP File, you should first assign those names to a signal bus and then add the bus to the STP File.
If you select **SignalTap II: pre-synthesis or SignalTap II: post-fitting** in the **Filter** list of the Node Finder and select a bus to add to the STP File, the Quartus II software may expand the bus into individual nodes that may be removed during synthesis, resulting in an error.	Delete the nodes and recompile the project. You can select individual nodes in the Node Finder and group them in the SignalTap II window using the **Group** command (Edit menu).

Simulation

Issue	Workaround

The PLLs in designs targeted to Stratix devices sometimes do not simulate correctly in other EDA simulation tools. The PLLs do not lock when you are driving the `altlvds_tx` megafunction with the `altlvds_rx` clock, or if you are driving the `altlvds_rx` megafunction with the `altlvds_tx` clock.	Make the following changes to the VHDL or Verilog HDL files generated by the **MegaWizard Plug-In Manager** and the `altlvds_tx` or `altlvds_rx` megafunctions.
	When using the `altlvds_tx` clock output to drive the `altlvds_rx` PLL, make the following changes:
	
	For VHDL :
	`COMPONENT altlvds_rx`
	`GENERIC (clk_src_is_pll : STRING`
	and
	`altlvds_rx_component : altlvds_rx`
	`GENERIC MAP (clk_src_is_pll > “on”`
	
	For Verilog HDL:
	`altlvds_rx_component.clk_src_is_pll = “on”;`
	
	Or when using the `altlvds_rx` clock output to drive the `altlvds_tx` PLL, make the following changes:
	For VHDL :
	`COMPONENT altlvds_tx`
	`GENERIC (clk_src_is_pll : STRING`
	and
	`altlvds_tx_component : altlvds_tx`
	`GENERIC MAP (clk_src_is_pll > “on”`
	
	For Verilog HDL:
	`altlvds_tx_component.clk_src_is_pll = “on”;`

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
The Verilog and VHDL extractors now support the `translate_off` and `translate_on` pragmas. This change in support may cause problems in some designs that relied on the behavior of the Quartus II software versions earlier than version 2.1, which ignore pragmas. A common case is where you have a MegaWizard-generated VHDL or Verilog HDL megafunction and have added `translate_off` and `translate_on` pragmas to hide the internal details from your EDA synthesis tool. If you use those pragmas, the details will also be hidden from the Quartus II software, and as a result, the megafunctions will not be implemented when you compile using the Quartus II software version 2.1 and later.	
Some designs that compiled successfully using the Quartus II software version 2.0 may not compile successfully using the Quartus II software version 2.1 and later. Common issues are: • Assigning to a single register in multiple Always Constructs or Process Constructs. The Quartus II software version 2.1 and later will give a multiply-driven signal error. • Width mismatches in VHDL that were not caught in the Quartus II software version 2.0. • Referring to another generic within a generic list in VHDL, for example having generic `WIDTH` and generic `DATA(WIDTH downto 0)`. This feature is not officially supported in VHDL, but it is supported in many tools including the Quartus II software version 2.0. It is not supported in the Quartus II software version 2.1 and later.	

Issue	Workaround
If you have an IP core in VHDL or Verilog HDL and your license is not set up correctly, you will get a "`Can't open design file`" error.	Refer to *Application Note 205: Altera Licensing* and *Application Note 229: Troubleshooting Altera Software Licensing* for more information on setting up your license.
The Quartus II software version 2.1 and later connect all nets driven by `GND` together, and all nets driven by `VCC` together. This can cause confusing error messages, as an electrical conflict on one `GND` net may be reported on any `GND` net, not necessarily the one that is actually causing the problem.	
The Quartus II software version 3.0 gives the message "`Error: Duplicate entity <name> found in file <filename1> colliding with the one found in file <filename2>`," for a project that compiled successfully with Quartus II 2.2 or earlier.	The Quartus II software version 2.2 and earlier versions gave a Warning when they encountered a duplicate definition of a VHDL or Verilog entity and ignored the duplicate. The Quartus II software version 3.0 will give an error message when it finds two or more definitions of a VHDL or Verilog entity in the same project. To avoid this error in the future, remove the duplicate entity or entities.
The Quartus II software version 3.0 gives the message "`Error: illegal Procedural Assignment to nonregister data type <name>`," or "`Error: illegal continuous assignment to non-net data type <name>`," for a project that compiled successfully with the Quartus II software version 2.2 or earlier.	The Quartus II software version 3.0 enforces the distinction between `reg` data types and `wire` data types, as required in the Verilog standard. The Quartus II software version 2.2 and earlier did not enforce this distinction. To avoid receiving this error in the future, declare the variable as a `wire` when you use a continuous assignment, and as a `reg` when you use a procedural assignment.
The Quartus II software version 3.0 gives the message "`Error: unsupported choice with meta-value 'X'`" (or `'-'`) for a project that compiled successfully with the Quartus II software version 2.2 or earlier. This occurs in a case statement which uses the meta-values `'X'` or `'-'`.	Previous versions of the Quartus II software ignored a `case` item with a meta-value and printed a Warning message. However, this can cause simulation-synthesis mismatches and this design style can also be synthesized differently with other synthesis tools. To match the behavior of the Quartus II software version 2.2, delete the `case` item with the meta-value. If this is not the behavior you want, re-code your design to avoid the use of `'X'` in the `case` statement.

Verilog HDL Integrated Synthesis

Issue	Workaround
Verilog-2001 mode is enabled by default. This mode can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as `config`.	Do not use Verilog-2001 reserved words as identifiers or select **Verilog-1995** on the **Verilog HDL** input page under **HDL Input Settings** of the **Settings** dialog box (Assignments menu).
The Quartus II software version 2.1 and later looks for files in an `` `include `` compiler directive in the project root directory and the user library directories. If there is a path specified, it is interpreted as being relative to the project root directory or the user library directory.	
A function call in a vector range specification causes an Internal Error.	
Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single-bit component port named `\my_vector_port[3:0]`, the Quartus II software versions 2.1 and later will treat it as an array port.	You should avoid using escaped port names in the Quartus II software version 2.1 and later.
The Quartus II software version 2.1 and later does not allow two parameter value overrides (Defparam Statements) for a parameter. This behavior is different from the IEEE Std. 1364-2001 *IEEE Standard Verilog Hardware Description Language* manual, in which the last Defparam Statement is used if there are multiple Defparam Statements.	
Recursive Verilog HDL functions or modules, such as a module that instantiates itself, are not supported by the Quartus II software.	

VHDL Integrated Synthesis

Issue	Workaround
The Quartus II software version 2.1 and later does not synthesize `a < b` for user-defined enums.	

SOPC Builder Issues

Issue	Workaround
If the Quartus II software is installed in a directory having space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.
When adding an Excalibur Stripe component in conjunction with Avalon peripherals, you may encounter SOPC Builder errors indicating too many masters are present.	If the master-connection patch-panel is not visible, choose **Show Master Connections** (View menu). Then click on the master/slave intersection indicated by the error message. This will remove the connection. Click again to restore the connection and the error will not reappear.
After specifying a Motorola S-Record file (**.srec**) or a binary file (**.bin**) containing on-chip memory contents, the resulting generated files do not contain the memory data.	The problem occurs only when the base address specified in the SREC file or implied in the binary file does not explicitly match the base address of the targeted memory. To avoid this problem, you can use one of the following techniques: • Use a binary file, and base the target memory at address 0 *or* • Use an SREC file as input, and base it at the same address as the target memory *or* • Initialize the memory at run-time
You installed Nios 3.x and don't see your Nios-related components in SOPC Builder 3.0, or you see them as inaccessible white dots (unlicensed components). This includes the Nios core itself as well as the Timer, PIO, UART, SPI, and other items.	1. Choose **SOPC Builder Setup** (File menu) 2. In the **Pre 3.0 SOPC Builder Installation** box, type the path to your existing Nios 3.x installation. 3. Click **OK** 4. Exit and restart SOPC Builder. Your components should be accessible.

Issue	Workaround
Only 'bash' and 'sh' are supported for SOPC Builder SDK Shell. The 'csh' support previously available in Nios kits is not present in SOPC Builder version 3.0. This does not affect the use of SOPC Builder from within the Quartus II software.	Contact Altera Applications for updates on the status of 'csh' support. Users can set up their own environment to operate SOPC Builder under 'csh', by setting PATH and other variables using the script: **<*quartus*>/sopc_builder/bin/nios_sh** as an example.

SOPC Builder Compatibility

Nios version 3.0x / SOPC Builder 2.8x

You can use your existing Nios components and they will be recognized automatically by the SOPC Builder integrated into the Quartus II version 3.0 software.

Nios version 2.2 / SOPC Builder 2.7

Your Nios components are not compatible with the SOPC Builder integrated with the Quartus II version 3.0 software. You will receive upgraded Nios components as part of a new Nios Development Kit. You can run your earlier version of SOPC Builder by following these steps:

1. If Altera SOPC Builder 2.7 is not shown in the MegaWizard Plug-In Manager, reinstall the SOPC Builder version 2.7 software, or copy the **sopc_builder_2_7_wizard.lst** file into your **quartus\libraries\megafunctions** directory.
2. When you open a system that uses the Nios version 2.2 embedded processor, you will be given the choice of using the Altera SOPC Builder or the Altera SOPC Builder 2.7. Choose the 2.7 version. If you choose the version without a number (version 3.0) your components will be disabled.

SOPC Builder Project Files

When you open a project created in a version of SOPC Builder earlier than version 3.0 in the SOPC Builder included in the Quartus II version 3.0 software, you will be given a choice to update your project or cancel the operation.

If you choose to update your project, the software will make a backup copy of your SOPC Builder Project file (**.ptf**) and will modify your PTF to make it compatible with the current version of the software.

If you choose to cancel the operation, you can open your project with the earlier version of the SOPC Builder software by following the steps shown above.

EDA Integration Issues

Issue	Workaround
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for ATOPS mode, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
The directory containing the ARM-based Excalibur stripe models changed in the Quartus II software version 2.0. This change may cause compilation scripts that were created for earlier versions of the Quartus II software to fail.	Edit your compilation scripts so that the models and simulation wrapper files are located in the following directory: **\quartus\eda\sim_lib\ excalibur\ stripe_model_<*operating system*> \ModelGen\models\epxa<*1* | *4* | *10*>\r0\<*simulator_language*>**
There is not an option in the installation program to install the EDA tool interface for the Cadence Concept software, even though the software is supported by the Quartus II software version 2.2.	Select Cadence Verilog-XL in the installation to install the **cadence.tcl** interface script in your **<*Quartus II installation*>/eda/cadence** directory.
The Cadence NC-VHDL version 3.4 software requires the s013 patch, which contains a more stable version of the NC-VHDL software.	Install the s013 patch, available from Cadence, for the NC-VHDL software before simulating designs.
Wildcard cut timing assignments made in the Quartus II software are not included in the Quartus II-generated TCL Script File for performing timing analysis in the Synopsys PrimeTime software.	Add the wildcard cut timing assignments directly in the PrimeTime software, add the assignments to the Synopsys Design Constraints (SDC) File for the project, or modify the Quartus II-generated Tcl Script File to include the assignments before performing timing analysis in the PrimeTime software.

Issue	Workaround
The Quartus II software may duplicate some registers during fitting, which can cause unmapped points between the golden and revised netlists when performing formal verification with the Verplex Conformal LEC software.	To flatten the revised netlist in the LEC software and merge the duplicated registers, add the following command to the Quartus II-generated **<*design name*>.vlc** script file. `flatten model -all_seq_merge` If you are performing formal verification manually in the LEC software, you can type the command at the LEC prompt.
The `altdqs` files generated by the MegaWizard Plug-In Manager will not simulate with other EDA simulation tools correctly.	You must edit each instantiation of the `altdqs` megafunction in your design. 1. Inside the **stratix_dll** section, locate the **phase_shift** parameter. Convert the value of that parameter to an integer by removing the quotation marks (“) from around it. 2. Locate the **input_frequency** parameter. Convert the value to picoseconds and type it without quotation marks. 3. Comment out any lines that contain the following code: `lpm_type`. 4. Inside each of the **stratix_io** sections, locate the **sim_dll_phase_shift** parameter. Convert the value of that parameter to an integer by removing the quotation marks (**“**) from around it. 5. Locate the **sim_dqs_input_frequency** parameter. Convert the value to picoseconds and type it without quotation marks. 6. Comment out any lines that contain the following code: `lpm_type`. 7. In addition, for VHDL instantiations, you must locate the corresponding Component Declarations and change them as shown in the example below: *(continued on next page)*

Issue	Workaround

Continued from previous page	`COMPONENT stratix_dll`
	`GENERIC`
	`(`
	`INPUT_FREQUENCY : STRING;`
	`PHASE_SHIFT : STRING := "90";`
	should be modified to
	`INPUT_FREQUENCY : INTEGER;`
	`PHASE_SHIFT : INTEGER := 90;`
	and
	`SIM_DLL_PHASE_SHIFT : STRING := "unused";`
	`SIM_DQS_INPUT_FREQUENCY : STRING;`
	should be modified to
	`SIM_DLL_PHASE_SHIFT : INTEGER := 0;`
	`SIM_DQS_INPUT_FREQUENCY : INTEGER;`

Simulation Model Changes

altera_mf Models

RAM Models

Model	Change
`altqpram`	• Improved checking for 'write enabled' under BIDIR mode. (VHDL & Verilog HDL) • Enabled simultaneous write at different address and rectify port B write operation under BIDIR mode. (VHDL & Verilog HDL)
`altdpram`	• Fixed inconsistent read from RAM with VCS simulator. (Verilog HDL)
`altsyncram`	• Added `width_byteena` to support Clearbox flow. (VHDL)
`dcfifo`	• Fixed bit shifting operation to avoid race condition reported by VCS. (Verilog HDL) • Added ADD_RAM_OUTPUT_REGISTER parameter to support for registered output. (VHDL & Verilog HDL)
`scfifo`	• Fixed `almost_full` and `almost_empty` ports when ALMOST_FULL(EMPTY)_VALUE=0/1. (VHDL & Verilog HDL)
`altcam`	• Standardized unconnected port `inaclr` to value `'0'` to avoid inconsistent result from different simulators. (Verilog HDL)

DSP Models

Model	Change
altmult_add	• Added two parameters (dedicated_multiplier_circuitry and intended_device_family) to support wizard flow. (VHDL & Verilog HDL)

I/O Models

Model	Change
altpll	• Corrected external feedback mode. (VHDL & Verilog HDL) • Fixed counter initial value to match post place and route dynamic value. (VHDL & Verilog HDL) • Fixed output '0' instead of 'X' when areset is high. (VHDL & Verilog HDL) • Fixed type mismatch error that's only observed in SCIROCCO. (VHDL)
altcdr	• Synchronous changes with gate-level model. (VHDL & Verilog HDL) • Fixed reset connection in HSSI_TX. (VHDL)
altclklk	• Used time variable (64bits) to store simulation time instead of using integer (32 bits). (Verilog HDL)
altfp_mult	• Status ports ZERO, DENORMAL, and INDEFINITE will not be used. (VHDL & Verilog HDL)
altlvds_rx	• Fixed incorrect output in Stratix device LVDS receiver when the input clock was slipped by one bit. (VHDL & Verilog HDL) • Added support for x1 and x2 mode for APEX II devices. (VHDL & Verilog HDL) • For Stratix GX devices, DPA is now registered with Global clock instead of being connected to the reset port. (Verilog HDL)
altlvds_tx	• Added support for x1 and x2 mode for APEX II devices. (VHDL & Verilog HDL)

220 Models

Model	Change
lpm_clshift	• Fixed overflow output for "arithmetic shift" operation. (Verilog HDL)
lpm_divide	• Modified the model to support > 32 bit division. (Verilog HDL) • Changed quotient and remainder output to undefined if denominator is zero. (Verilog HDL)

Latest Known Quartus II Software Issues

For known software issues after publication of this version of the Quartus II Software Release Notes, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Knowledge Database at the following URL:
www.altera.com/support/kdb/kdb-sw_quartus2.jsp