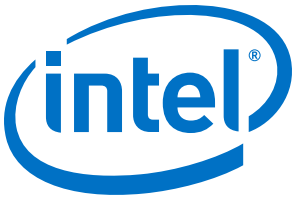

Low Latency 40G ASIC Proto for Ethernet Intel® FPGA IP Release Notes

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1. Low Latency 40G ASIC Proto for Ethernet Intel FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- Low Latency 40G ASIC Proto for Ethernet Intel FPGA IP User Guide
- Low Latency 40G ASIC Proto for Ethernet Intel FPGA IP Design Example User Guide

1.1. Low Latency 40G ASIC Proto for Ethernet Intel FPGA IP v19.1.0

Table 1. v19.1.0 2020.07.07

Intel Quartus Prime Version	Description	Impact
20.2	Initial Release.	—