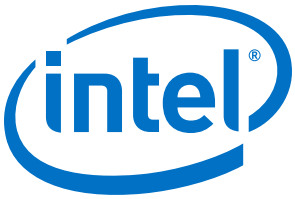

Serial Digital Interface (SDI) II Intel FPGA IP Release Notes

RN-1091 | 2019.04.01
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Contents

1. Serial Digital Interface (SDI) II Intel FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- SDI II Intel FPGA IP User Guide
  Refer to the SDI II Intel FPGA IP User Guide Archives section for previous versions.
- SDI II Intel Arria 10 FPGA IP Design Example User Guide
  Refer to the SDI II Intel Arria 10 FPGA IP Design Example User Guide Archives section for previous versions.
- SDI II Intel Cyclone 10 GX FPGA IP Design Example User Guide
  Refer to the SDI II Intel Cyclone 10 GX FPGA IP Design Example User Guide Archives section for previous versions.
- SDI II Intel Stratix 10 FPGA IP Design Example User Guide
  Refer to the SDI II Intel Stratix 10 FPGA IP Design Example User Guide Archives section for previous versions.
- Errata for SDI II Intel FPGA IP in the Knowledge Base

1.1. SDI II Intel FPGA IP v19.1

Table 1. v19.1 April 2019

Description	Impact
Enabled final support for Intel Stratix® 10 L-tile and H-tile devices. The design examples now target Intel Stratix 10 production devices.	If you want to target your designs to use Intel Stratix 10 L-tile devices, you must upgrade your IP core.

1.2. SDI II Intel FPGA IP v18.1 Update 2

18.1.2 February 2019

- For Intel Stratix 10 H-tile devices, updated the design examples.

1.3. SDI II Intel FPGA IP v18.1 Update 1

18.1.1 January 2019

- For Intel Stratix 10 H-tile devices, added VID_OPERATION_MODE "PMBUS MASTER" and PWRMGMT settings to the video connectivity design example IP `.qsf` file to enable Intel Stratix 10 SmartVID and power management capabilities.

Related Information

- Introduction to Intel FPGA IP Cores
- SDI II Intel FPGA IP User Guide
- SDI II Intel Arria 10 FPGA IP Design Example User Guide
- SDI II Intel Cyclone 10 GX FPGA IP Design Example User Guide
- SDI II Intel Stratix 10 FPGA IP Design Example User Guide
- Errata for SDI II Intel FPGA IP in the Knowledge Base

1.4. SDI II Intel FPGA IP v18.1

Table 2. v18.1 September 2018

Description	Impact
Enabled payload ID insertion into chroma streams and 6G-SDI with 8 streams interleaved for the IP core.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Enhanced TRS detection in 6G-SDI and 12G-SDI for better performance for the IP core.	
Fixed payload ID insertion issues on 1080p50/60 on 3G Level A and SD 525i video formats in the Intel Arria® 10, Intel Cyclone® 10 GX, and Intel Stratix 10 design examples.	
Improved robustness in the serial loopback design during standard switching in the Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10 design examples.	

Related Information

- Introduction to Intel FPGA IP Cores
- SDI II Intel FPGA IP User Guide
- SDI II Intel Arria 10 FPGA IP Design Example User Guide
- SDI II Intel Cyclone 10 GX FPGA IP Design Example User Guide
- SDI II Intel Stratix 10 FPGA IP Design Example User Guide
- Errata for SDI II Intel FPGA IP in the Knowledge Base

1.5. SDI II Intel FPGA IP v18.0

Table 3. v18.0 May 2018

Description	Impact
Renamed Intel FPGA SDI II IP to SDI II Intel FPGA IP as part of standardizing and rebranding exercise.	–
Added support for Xcelium* Parallel simulator.	These changes are optional. If you do not upgrade your IP core, it does not have

continued...

Description	Impact
Added a new parameter, **Rx core clock (rx_coreclk) frequency**. This parameter is available only when you select **Multi rate (up to 12G)** and **Receiver** or **Bidirectional** direction in the Intel Quartus Prime Pro Edition software.	these new features.
Updated the `rx_coreclk_is_ntsc_paln` signal to include 297.0 MHz and 296.70 MHz options.	
Added **Parallel loopback without external VCXO** option for Intel Stratix 10 design example.	
Added the following files: • `pid_controller.v` • `rcfg_pll_frac.v` • `modelsim_files.tcl` • `ncsim_files.tcl` • `riviera_files.tcl` • `vcs_files.tcl` • `vcsmx_files.tcl` • `xcelium_files.tcl` • `tb_ln_check.v` • `cds.lib` • `hdl.var` • `xcelium_setup.sh` • `xcelium_sim.sh`	
Added final support for Intel Cyclone 10 GX devices.	The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.
Added new design examples for Intel Cyclone 10 GX devices in version 17.1.1 release. Refer to the *SDI II Intel Cyclone 10 GX FPGA IP Design Example User Guide* for more information.	

Table 4. Design Files Required for IP Upgrade

The implementation of the IP on hardware requires additional components specific to the device targeted.

These additional components, such as Native PHY, TX PLL, reconfiguration controller, are not included as part of the Intel Quartus Prime IP Upgrade flow. Upgrading an IP core would require the inclusion of these files generated as part of the IP design example.

Design Example	Required Files
Intel Arria 10	• `sdi_ii_a10_demo.v` • `sdi_ii_a10_demo.sdc` • `edge_detector.sv` • `clock_heartbeat.sv` • `a10_reconfig_arbiter.sv` • Files inside the <*vid_pattgen*> folder • Files inside <*loopback*> folder • Files inside <*du*>, or <*rx*> and <*tx*> folders
Intel Cyclone 10 GX	• `sdi_ii_a10_demo.v` • `sdi_ii_a10_demo.sdc` • `edge_detector.sv` • `clock_heartbeat.sv` • `a10_reconfig_arbiter.sv`

continued...

Design Example	Required Files
	• Files inside the <*vid_pattgen*> folder • Files inside <*loopback*> folder • Files inside <*du*>, or <*rx*> and <*tx*> folders
Intel Stratix 10	• `sdi_ii_a10_demo.v` • `sdi_ii_a10_demo.sdc` • `edge_detector.sv` • `clock_heartbeat.sv` • `a10_reconfig_arbiter.sv` • Files inside the <*vid_pattgen*> folder • Files inside <*loopback*> folder • Files inside <*du*>, or <*rx*> and <*tx*> folders • Files inside <*mr_phy_adapter*> folder

Related Information

- Introduction to Intel FPGA IP Cores
- SDI II Intel FPGA IP User Guide
- SDI II Intel Arria 10 FPGA IP Design Example User Guide
- SDI II Intel Cyclone 10 GX FPGA IP Design Example User Guide
- SDI II Intel Stratix 10 FPGA IP Design Example User Guide
- Errata for SDI II Intel FPGA IP in the Knowledge Base

1.6. Intel FPGA SDI II IP Core v17.1

Table 5. v17.1 November 2017

Description	Impact
Renamed the following as per Intel rebranding: • SDI II IP core to Intel FPGA SDI II IP core • Qsys to Platform Designer	–
Added preliminary support for Intel Stratix 10 (H-Tile) devices.	The Intel Stratix 10 devices are only available in the Intel Quartus Prime Pro Edition software.
Added new design examples for Intel Stratix 10 devices. Refer to the *Intel FPGA SDI II Design Example User Guide for Intel Stratix 10 Devices* for more information.	
In previous versions of the Intel FPGA SDI II design example for Intel Arria 10 devices, the IOPLL and transceiver PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in the Intel Quartus Prime software version 17.1.	If you are upgrading designs that have these additional constraints from the previous versions of the Intel Quartus Prime software to version 17.1, you must revise the constraints. Refer to the KDB page for more information.

Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA SDI II IP Core User Guide
- Intel FPGA SDI II Design Example User Guide for Intel Stratix 10 Devices
- Intel FPGA SDI II Design Example User Guide for Intel Arria 10 Devices
- Errata for Intel FPGA SDI II IP Core in the Knowledge Base

1.7. SDI II IP Core v17.0

Table 6. v17.0 May 2017

Description	Impact
Available in both Quartus Prime Pro Edition and Quartus Prime Standard Edition.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated the existing SDI II design examples to be more dynamic and added a new design example for serial loopback.	
Fixed a bug in 6G 8 streams interleave where sync bit is not inserted correctly for ADF words.	

Related Information

- Introduction to Intel FPGA IP Cores
- SDI II IP Core User Guide
- Intel Arria 10 SDI II IP Core Design Example User Guide
- Errata for SDI II IP Core in the Knowledge Base

1.8. SDI II IP Core v16.1

Table 7. v16.1 October 2016

Description	Impact
The 16.1 version of the SDI II IP core is available only in Quartus Prime Standard Edition.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added new **Design Example** tab in the SDI II IP core parameter editor. The design examples are for Arria 10 devices. Refer to the *SDI II IP Core Design Example User Guide* for more information.	
Removed HD dual link support for Arria 10 devices.	

Related Information

- Introduction to Intel FPGA IP Cores
- SDI II IP Core User Guide
- SDI II IP Core Design Example User Guide
- Errata for SDI II IP Core in the Knowledge Base

1.9. SDI II IP Core v16.0

Table 8. v16.0 May 2016

Description	Impact
Added the fPLL option for the Arria 10 TX PLL parameter and removed the ATX PLL option for Arria 10 device.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Removed `rx_pll_locked` and `rx_pll_locked_b` signals for Arria V, Cyclone V, and Stratix V devices. These signals are redundant and no longer required after the switch to Native PHY.	
Updated the reconfig management files for Arria 10 devices (in generated designs).	

Related Information

- Introduction to Intel FPGA IP Cores

- SDI II IP Core User Guide
- Errata for SDI II IP Core in the Knowledge Base

1.10. SDI II IP Core v15.1

Table 9. v15.1 November 2015

Description	Impact
Redefined the `rx_format` signal. Each stream of 6G-SDI and 12G-SDI interfaces reports its own detected rx format. For example, when receiving 2160p60 in 12G-SDI, all 4 streams are expected to report 1080p60.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added new interface signals for Arria V, Cyclone V, and Stratix V devices: • `rx_trs_in` • `pll_powerdown_in` • `pll_ powerdown_out`	
Added new reconfiguration management parameters for Arria 10 devices: • `VIDEO_STANDARD` • `ED_TXPLL_SWITCH` • `XCVR_RCFG_IF_TYPE`	
Fixed jitter tolerance reduction issue when receiving SD-SDI video standards.	
Updated the `sdc` constraint for the dual-clock FIFO (DCFIFO) component instantiated in the core.	

Related Information

- Introduction to Altera IP Cores
- SDI II IP Core User Guide
- Errata for SDI II IP Core in the Knowledge Base

1.11. SDI II IP Core v15.0

Table 10. v15.0 May 2015

Description	Impact
Added the following parameters: • Added new video standard **Multi rate (up to 12G)** for Arria 10 devices. • Added TX PLL reference clock switching option for **Dynamic Tx clock switching** parameter.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Included design example for TX PLL reference clock switching. *Note:* Tx PLL reference clock switching is not supported for ATX PLL in Arria V GZ and Stratix V devices.	

Related Information

- Introduction to Altera IP Cores
- SDI II IP Core User Guide
- Errata for SDI II IP Core in the Knowledge Base

1.12. SDI II IP Core v14.1

Table 11. v14.1 December 2014

Description	Impact
The `run_sim` script for each simulator is now located in its respective folder.	-
`rx_format` signal now reports video transport format instead of picture format. The signal reports 3G Level A RGB or YCbCr 4:4:4 format.	If you update to the Quartus II software version 14.1, you must update your SDI II IP core to incorporate this fix.
Changed the names of the following parameters: • **Convert Level A to Level B (SMPTE 372M)** changed to **Convert HD-SDI dual link to 3G-SDI (level B)** • **Convert Level B to Level A (SMPTE 372M)** changed to **Convert 3G-SDI (level B) to HD-SDI dual link**	-

Related Information

- Introduction to Altera IP Cores
- SDI II IP Core User Guide
- Errata for SDI II IP Core in the Knowledge Base