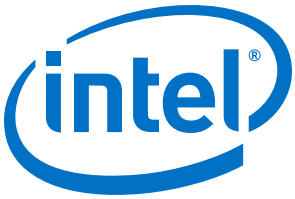

Clock Control Intel FPGA IP Core Release Notes

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Contents

1. Clock Control Intel FPGA IP Core Release Notes (Intel® Stratix® 10 Devices)

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Stratix® 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

1.1. Clock Control Intel FPGA IP v20.0.0

Table 1. v20.0.0 2020.09.28

Intel Quartus Prime Version	Description	Impact
20.3	• Updated the SDC for the clock divider to specify master clocks and exclusive clock groups. • Allow IP to be connected within the Platform Designer using the standard Platform Designer interfaces.	—

1.2. Clock Control Intel FPGA IP v19.1.0

Table 2. v19.1.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	IP name changed from Clock Control Intel Stratix 10 FPGA IP core to Clock Control Intel FPGA IP core.	—

1.3. Clock Control Intel Stratix 10 FPGA IP v18.0

Table 3. v18.0 May 2018

Description	Impact
Renamed Stratix 10 Clock Control IP core to Clock Control Intel Stratix 10 FPGA IP core as per Intel rebranding.	—
Renamed 'falling edge' mode to 'negative latch' mode.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix® 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

1.4. Stratix 10 Clock Control v17.1

Table 4. v17.1 November 2017

Description	Impact
Initial release for Intel Stratix® 10 devices.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

1.5. Intel Stratix 10 Clocking and PLL User Guide Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
19.3	Intel Stratix 10 Clocking and PLL User Guide
19.2	Intel Stratix 10 Clocking and PLL User Guide
18.1	Intel Stratix 10 Clocking and PLL User Guide
18.0	Intel Stratix 10 Clocking and PLL User Guide
17.1	Intel Stratix 10 Clocking and PLL User Guide

2. Clock Control Intel FPGA IP Core Release Notes (Intel Agilex™ Devices)

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel Quartus Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Agilex™ Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

2.1. Clock Control Intel FPGA IP v2.0.0

Table 5. v2.0.0 2020.09.28

Intel Quartus Prime Version	Description	Impact
20.3	• Updated the SDC for the clock divider to specify master clocks and exclusive clock groups. • Allow IP to be connected within the Platform Designer using the standard Platform Designer interfaces.	—

2.2. Clock Control Intel FPGA IP v1.0.0

Table 6. v1.0.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Initial release for Intel Agilex™ devices.	—

2.3. Intel Agilex Clocking and PLL User Guide Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
20.1	Intel Agilex Clocking and PLL User Guide
19.3	Intel Agilex Clocking and PLL User Guide