



Temperature Sensor Intel[®] Stratix[®] 10 FPGA IP Release Notes



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Temperature Sensor Intel® Stratix® 10 FPGA IP Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Information

[Intel Quartus Prime Design Suite Update Release Notes](#)

Temperature Sensor Intel® Stratix® 10 FPGA IP v18.0

Table 1. v18.0 May 2018

Description	Impact
Renamed the IP core from "Intel® FPGA S10 Temperature Sensor" to "Temperature Sensor Intel Stratix® 10 FPGA IP".	—
Added support for sampling the internal temperature sensing diodes (TSDs) in the high-bandwidth DRAM memory (HBM2) stacks.	The cmd_data signal is now 9-bits width.
Added response value to the rsp_data signal to indicate invalid data.	0x80000000 indicates invalid data.

Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [Intel Stratix 10 Analog to Digital Converter User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

Intel FPGA S10 Temperature Sensor IP Core v17.1

Table 2. v17.1 November 2017

Description	Impact
Initial release. This IP is available for Intel Stratix 10 devices only.	—

Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [Intel Stratix 10 Analog to Digital Converter User Guide](#)
- [Errata for other IP cores in the Knowledge Base](#)

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