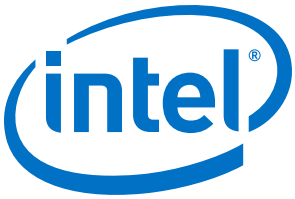

P-Tile IP for PCI Express IP Core Release Notes

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Contents

1. P-Tile IP for PCI Express IP Core Release Notes

1.1. P-Tile IP for PCI Express IP Cores v4.0.0

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IPs have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel® Quartus® Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 1. v4.0.0 2020.12.14

Intel Quartus Prime Version	Description	Impact
20.4	Migrating a design using a P-tile Avalon® Streaming or Avalon Memory-mapped IP from an earlier Intel Quartus Prime version to the 20.4 version requires an IP upgrade.	You must regenerate any design using a P-tile Avalon Streaming or Avalon Memory-mapped IP when moving from an earlier Intel Quartus Prime version to the 20.4 version.
	Parameters to enable independent resets for the ports in the bifurcated x8x8 Endpoint mode have been added to the IP Parameter Editor of the P-tile Avalon Streaming and Avalon Memory-mapped IPs.	Each port in the bifurcated x8x8 Endpoint mode can be reset independently of the other port. Two new reset signals (`p0_pld_clrpcs_n`, `p1_pld_clrpcs_n`) are exported to the top-level block symbol when independent resets are enabled. These signals can be assigned to GPIO pins. Contact your local Field Applications Engineer (FAE) for more details.
	The parameter to enable the MSI-X capability has been removed from the IP Parameter Editor when the P-tile Avalon Streaming or Avalon Memory-mapped IP is in Root Port (RP) mode.	The P-tile Avalon Streaming or Avalon Memory-mapped IP is not required to support sending MSI-X in RP mode.
	The parameter to enable extended tag support has been added to the IP Parameter Editor of the P-tile Avalon Streaming IP.	The P-tile Avalon Streaming IP can support extended tag in this release.
	Options to set acceptable Power Management latencies for Endpoints were added to the IP Parameter Editor of the P-tile Avalon Memory-mapped IP.	L0s and L1s acceptable latencies can now be configured in the IP Parameter Editor of the P-tile Avalon Memory-mapped IP in Endpoint mode.

continued...

Intel Quartus Prime Version	Description	Impact
	Options to configure the VSEC parameters in Endpoint mode were added to the IP Parameter Editor of the P-tile Avalon Memory-mapped IP.	VSEC parameters can now be configured in the IP Parameter Editor of the P-tile Avalon Memory-mapped IP in Endpoint mode.
	The parameter to enable VirtIO and SR-IOV capabilities have been removed from the IP Parameter Editor when the P-tile Avalon Streaming IP is in Root Port (RP) mode.	The P-tile Avalon Streaming IP is not required to support VirtIO or SR-IOV in RP mode.
	Options for BAR configuration, Multi-function and SR-IOV support have been removed from the IP Parameter Editor when the P-tile Avalon Streaming IP is in TLP Bypass mode.	The P-tile Avalon Streaming IP is not required to support these features in TLP Bypass mode.
	Options for Multi-function and SR-IOV support support are now visible for Port 1 when the P-tile Avalon Streaming IP is in a bifurcated mode.	Multi-function and SR-IOV support can be enabled for Port 1 when the P-tile Avalon Streaming IP is in a bifurcated mode.
	The IP Parameter Editor response time has been improved for the P-tile Avalon Streaming IP.	The turnaround time after each user input in the IP Parameter Editor is significantly reduced for the P-tile Avalon Streaming IP in this release.

Table 2. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	400 MHz	400 MHz	N/A
Gen3 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Table 3. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	500 MHz	500 MHz	N/A
Gen3 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Table 4. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	350 MHz	350 MHz	N/A
Gen4 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	200 MHz	200 MHz	N/A
Gen4 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	200 MHz	200 MHz	N/A
Gen3 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	250 MHz	250 MHz	N/A
Gen3 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	125 MHz	125 MHz	N/A
Gen3 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	125 MHz	125 MHz	N/A

Note: (†) The design example available in the 20.4 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (††) This support may be available in a future release of Intel Quartus Prime.

Table 5. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	400 MHz	400 MHz	N/A
Gen4 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	250 MHz	250 MHz	N/A
Gen4 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	250 MHz	250 MHz	N/A
Gen3 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	250 MHz	250 MHz	N/A
Gen3 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	125 MHz	125 MHz	N/A
Gen3 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	125 MHz	125 MHz	N/A

Note: (†) The design example available in the 20.4 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (††) This support may be available in a future release of Intel Quartus Prime.

1.2. P-Tile IP for PCI Express IP Cores v3.1.0

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IPs have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 6. v3.1.0 2020.10.05

Intel Quartus Prime Version	Description	Impact
20.3	The BFM for Endpoint mode simulations is not available in this release. It may be available in a future release.	Use a third-party BFM for Endpoint mode simulations.
	For the P-Tile Avalon Streaming IP, configurations with the Adapter enabled are not available in this release.	For the P-Tile Avalon Streaming IP, Gen4 x8 512-bit and Gen4 x4 256-bit configurations are not available in this release.
	The Parameter Editor of the P-Tile Avalon Streaming IP indicates support for a 125 MHz application clock frequency in some configurations of the IP. However, this frequency is not supported. If selected, the IP will be generated using a 250 MHz application clock.	For more details, refer to the following entry in the Intel Knowledge Base page: https://www.intel.com/content/www/us/en/programmable/support/support-resources/knowledge-base/ip/2020/when-using-the-intel--fpga-p-tile-avalon-streaming-ip-for-pci--e.html

Table 7. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	400 MHz	400 MHz	N/A
Gen3 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Table 8. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A

continued...

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	500 MHz	500 MHz	N/A
Gen3 x16 512-bit	S C T H	S C T H	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Table 9. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	350 MHz	350 MHz	N/A
Gen4 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	200 MHz	200 MHz	N/A
Gen4 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	200 MHz	200 MHz	N/A
Gen3 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	250 MHz	250 MHz	N/A
Gen3 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	125 MHz	125 MHz	N/A
Gen3 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	125 MHz	125 MHz	N/A

Note: (†) The design example available in the 20.3 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (††) This support may be available in a future release of Intel Quartus Prime.

Table 10. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	400 MHz	400 MHz	N/A
Gen4 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	250 MHz	250 MHz	N/A
Gen4 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	250 MHz	250 MHz	N/A

continued...

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen3 x16 512-bit	S C T H	(††)	S C T H (†)	(††)	250 MHz	250 MHz	N/A
Gen3 x8/x8 512-bit	S C T H	N/A	S C T H (†)	N/A	125 MHz	125 MHz	N/A
Gen3 x4/x4/x4/x4 256-bit	N/A	S C T H	N/A	(††)	125 MHz	125 MHz	N/A

Note: (†) The design example available in the 20.3 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (††) This support may be available in a future release of Intel Quartus Prime.

1.3. P-Tile IP for PCI Express IP Cores v3.0.0

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IPs have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 11. v3.0.0 2020.07.10

Intel Quartus Prime Version	Description	Impact
20.2	The VirtIO feature has timing issues in this release of Intel Quartus Prime.	Only compilation and simulation are supported for the VirtIO feature in this release.
	The Eye Plot feature in the Debug Toolkit is only available for Channel 0.	Eye Plot support for Channels other than Channel 0 may be available in a future release of Intel Quartus Prime.
	The P-Tile Avalon-ST and Avalon-MM IPs for PCIe support the PCIe Link Inspector in this release.	The PCIe Link Inspector allows you to monitor the PCIe link status at the Physical, Data Link and Transaction Layers.
	The P-Tile Avalon-ST IP adds Modelsim support for design example simulation in this release.	The P-Tile Avalon-ST IP can support Modelsim and VCS simulators in the 20.2 release of Intel Quartus Prime. The P-Tile Avalon-MM IP still only supports VCS. Other simulators may be supported in a future release.
	The independent `pin_perst` option is no longer available in the P-Tile Avalon-ST IP in this release.	When a x16 port is bifurcated into two x8 ports, a reset via `pin_perst` impacts both x8 ports.

continued...

Intel Quartus Prime Version	Description	Impact
	The P-Tile Avalon-MM IP for PCIe does not support 10-bit tags for the x16 core in this release.	The x16 core of the P-Tile Avalon-MM IP for PCIe only supports up to 64 outstanding Non-Posted Requests (NPRs) in this release.
	The Root Port (RP) BFM for Endpoint configurations is not available in this release. It may be available in a future release.	Use a third-party BFM to simulate the P-Tile Root Port design examples.
	Configurations with the Adapter enabled are not available in this release.	Gen4 x8, 512-bit and Gen4 x4 256-bit configurations are not available in this release.
	You cannot change the PCIe SerDes pin allocations for the P-Tile Avalon-ST and Avalon-MM IPs for PCIe in the Intel Quartus Prime project.	To ease PCB routing, you can take advantage of the lane reversal and polarity inversion features supported by the P-Tile Avalon-ST and Avalon-MM IPs for PCIe.

Table 12. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16	S C T H	S C T H	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	400 MHz	400 MHz	N/A
Gen3 x16	S C T H	S C T H	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8	S C T H	N/A	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Table 13. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16	S C T H	S C T H	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A

continued...

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	500 MHz	500 MHz	N/A
Gen3 x16	S C T H	S C T H	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8	S C T H	N/A	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Table 14. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16	S C T H	(**)	S C T H (*)	(**)	350 MHz	350 MHz	N/A
Gen4 x8/x8	S C T H	N/A	S C T H (*)	N/A	350 MHz	350 MHz	N/A
Gen4 x4/x4/x4/x4	N/A	S C T H	N/A	(**)	350 MHz	350 MHz	N/A
Gen3 x16	S C T H	(**)	S C T H (*)	(**)	250 MHz	250 MHz	N/A
Gen3 x8/x8	S C T H	N/A	S C T H (*)	N/A	250 MHz	250 MHz	N/A
Gen3 x4/x4/x4/x4	N/A	S C T H	N/A	(**)	250 MHz	250 MHz	N/A

Note: (*) The design example available in the 20.2 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (**) This support may be available in a future release of Intel Quartus Prime.

Table 15. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16	S C T H	(**)	S C T H (*)	(**)	400 MHz	400 MHz	N/A
Gen4 x8/x8	S C T H	N/A	S C T H (*)	N/A	400 MHz	400 MHz	N/A
Gen4 x4/x4/x4/x4	N/A	S C T H	N/A	(**)	400 MHz	400 MHz	N/A

continued...

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen3 x16	S C T H	(**)	S C T H (*)	(**)	250 MHz	250 MHz	N/A
Gen3 x8/x8	S C T H	N/A	S C T H (*)	N/A	250 MHz	250 MHz	N/A
Gen3 x4/x4/x4/x4	N/A	S C T H	N/A	(**)	250 MHz	250 MHz	N/A

Note: (*) The design example available in the 20.2 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (**) This support may be available in a future release of Intel Quartus Prime.

1.4. P-Tile IP for PCI Express IP Cores v2.0.0

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IPs have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 16. v2.0.0 2020.04.20

Intel Quartus Prime Version	Description	Impact
20.1	The VirtIO feature has timing issues in this release of Intel Quartus Prime.	Only compilation and simulation are supported for the VirtIO feature in this release.
	The Eye Plot feature in the Debug Toolkit is only available for Channel 0.	Eye Plot support for Channels other than Channel 0 may be available in a future release of Intel Quartus Prime.
	The P-Tile Avalon-ST and Avalon-MM IPs for PCIe only support VCS for design example simulation in this release.	Use VCS for design example simulation in the 20.1 release of Intel Quartus Prime. Other simulators may be supported in a future release.
	The P-Tile Avalon-ST and Avalon-MM IPs for PCIe do not support parallel PIPE simulations in this release.	Only Serial data interface simulations are supported in the 20.1 release of Intel Quartus Prime, which will result in longer simulation time. Parallel PIPE simulations may be supported in a future release.

continued...

Intel Quartus Prime Version	Description	Impact
	The independent `pin_perst` option is only available in the P-Tile Avalon-ST IP in this release.	For guidelines on implementing two independent `pin_perst`, contact Factory Applications.
	The P-Tile BFM is not supported in this release. It may be available in a future release.	Use a third-party BFM to simulate the P-Tile design examples.
	Parity is supported in this release. However, it is not supported when the Adapter is enabled.	Configurations with the Adapter enabled (i.e., Gen4 x8, 512-bit and Gen4 x4 256-bit) do not have parity support.

Table 17. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16	S C T H	S C T H	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x8/x8 512-bit	S C T	N/A	S C T H	S C T	N/A	N/A	400 MHz (*)	400 MHz (*)	N/A
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	400 MHz	400 MHz	N/A
Gen4 x4/x4/x4/x4 256-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	400 MHz (*)	400 MHz (*)	N/A
Gen3 x16	S C T H	S C T H	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8	S C T H	N/A	S C T H	S C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Note: (*) User Application will see a clock frequency of 200 MHz with double the data bus width.

Table 18. P-Tile Avalon Streaming (Avalon-ST) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support			Design Example Support			Timing Support		
	EP	RP	BP	EP	RP	BP	-1	-2	-3
Gen4 x16	S C T H	S C T H	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A
Gen4 x8/x8 256-bit	S C T H	N/A	S C T H	S C T H	N/A	N/A	500 MHz	500 MHz	N/A
Gen4 x8/x8 512-bit	S C T	N/A	S C T H	S C T	N/A	N/A	500 MHz (*)	500 MHz (*)	N/A
Gen4 x4/x4/x4/x4 128-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	500 MHz	500 MHz	N/A
Gen4 x4/x4/x4/x4 256-bit	N/A	S C T H	S C T H	N/A	N/A	N/A	500 MHz (*)	500 MHz (*)	N/A
Gen3 x16	S C T H	S C T H	S C T H	C T H	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x8/x8	S C	N/A	S C T	C	N/A	N/A	250 MHz	250 MHz	250 MHz
Gen3 x4/x4/x4/x4	N/A	S C T H	S C T H	N/A	N/A	N/A	250 MHz	250 MHz	250 MHz

Note: (*) User Application will see a clock frequency of 250 MHz with double the data bus width.

Table 19. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Stratix® 10 DX Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16	S C	(**)	(**)	(**)	(**)	(**)	N/A
Gen4 x8/x8	(**)	N/A	(**)	N/A	(**)	(**)	N/A
Gen4 x4/x4/x4/x4	N/A	(**)	N/A	(**)	(**)	(**)	N/A
Gen3 x16	S C T H	(**)	C T H (*)	(**)	250 MHz	250 MHz	N/A
Gen3 x8/x8	(**)	N/A	(**)	N/A	(**)	(**)	N/A
Gen3 x4/x4/x4/x4	N/A	(**)	N/A	(**)	(**)	(**)	N/A

Note: (*) The design example available in the 20.1 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (**) This support may be available in a future release of Intel Quartus Prime.

Table 20. P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCIe Support Matrix for Intel Agilex™ Devices

Support level keys: S = simulation, C = compilation, T = timing, H = hardware, N/A = configuration not supported

Configuration	PCIe IP Support		Design Example Support		Timing Support		
	EP	RP	EP	RP	-1	-2	-3
Gen4 x16	S C	(**)	(**)	(**)	(**)	(**)	N/A
Gen4 x8/x8	(**)	N/A	(**)	N/A	(**)	(**)	N/A
Gen4 x4/x4/x4/x4	N/A	(**)	N/A	(**)	(**)	(**)	N/A
Gen3 x16	S C T	(**)	C T (*)	(**)	250 MHz	250 MHz	N/A
Gen3 x8/x8	(**)	N/A	(**)	N/A	(**)	(**)	N/A
Gen3 x4/x4/x4/x4	N/A	(**)	N/A	(**)	(**)	(**)	N/A

Note: (*) The design example available in the 20.1 release supports the DMA mode with Data Movers. A design example supporting the Bursting Slave mode may be available in a future release.

Note: (**) This support may be available in a future release of Intel Quartus Prime.

1.5. P-Tile IP for PCI Express IP Cores v1.1.0

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IPs have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 21. v1.1.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	The VirtIO feature still has timing issues in this release of Intel Quartus Prime.	Only compilation and simulation are supported for the VirtIO feature in this release.
	An SR-IOV design example has been added for the P-Tile Avalon-ST IP for PCIe.	This design example supports Gen3 x16 and Gen4 x16 Endpoint configurations.

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Intel Quartus Prime Version	Description	Impact
	No P-Tile IP upgrade is supported in the 19.4 release of Intel Quartus Prime.	Users cannot upgrade a 19.3 P-Tile Avalon-ST or Avalon-MM IP to a 19.4 version.
	The P-Tile Avalon-MM IP for PCIe does not support design example simulation in this release.	The P-Tile Avalon-MM IP for PCIe may support design example simulation in a future release of Intel Quartus Prime.
	A high-bandwidth Adapter has been introduced for the P-Tile Avalon Streaming IP.	This Adapter allows the application logic to run Gen4 x8 and Gen4 x4 configurations with an application clock frequency of 250 MHz by doubling the Avalon Streaming data bus width. The Adapter is enabled automatically by Intel Quartus Prime when either the 512-bit Gen4 x8 or 256-bit Gen4 x4 configuration is selected.
	The P-Tile Avalon Streaming IP for PCI Express does not support parity protection for the RX and TX Avalon Streaming interfaces in this release of Intel Quartus Prime.	Parity protection for the RX and TX Avalon Streaming interfaces will be supported in a future release of Intel Quartus Prime.

1.6. P-Tile IP for PCI Express IP Cores v19.3

Table 22. 19.3 September 2019

Description	Impact
Initial release of the P-Tile Avalon-MM IP for PCI Express. This IP supports both Intel Stratix® 10 DX and Intel Agilex™ devices.	Added this new IP component to enable Avalon-MM support for P-Tile in the Gen3 x16 for Endpoint configuration. The support level is Advance. Other configurations may be supported in a future release of Intel Quartus Prime.
The P-Tile Avalon-MM IP for PCI Express includes internal Read Data Mover and Write Data Mover to support DMA operations.	This IP includes Data Mover interfaces to communicate with an external DMA Controller. The Intel Quartus Prime 19.3 release includes a PCIe DMA design example, which provides a DMA Controller that can interface with the internal Data Movers of the P-Tile Avalon-MM IP for PCI Express to perform DMA operations. Alternatively, you can build your custom DMA Controller in your application logic.
Added support for the Debug Toolkit for both P-Tile Avalon-MM and P-Tile Avalon-ST IPs for PCI Express.	The P-Tile Debug Toolkit is a System Console-based tool that provides real-time control, monitoring and debugging of the PCIe links at the Physical Layer.
Clocking topologies with Separate Reference Clock architectures are supported in this release.	P-Tile IPs for PCI Express support the Separate Reference Clock with no Spread Spectrum Clocking (SRNS) architecture by default, and the Separate Reference Clock with Independent Spread Spectrum (SRIS) Clocking architecture, which can be enabled from the IP Parameter Editor.
The P-Tile Avalon-MM IP for PCI Express does not support the Interrupt Interface, Error Interface and Configuration Intercept Interface in this release.	The P-Tile Avalon-ST IP for PCI Express does support these interfaces. The P-Tile Avalon-MM IP for PCI Express may support these interfaces in a future release of Intel Quartus Prime.
The P-Tile Avalon-MM IP for PCI Express does not support design example simulation in this release.	The P-Tile Avalon-ST IP for PCI Express does support design example simulation. The P-Tile Avalon-MM IP for PCI Express may support design example simulation in a future release of Intel Quartus Prime.

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Description	Impact
	You can still simulate the P-Tile Avalon-MM IP for PCI Express by using a third-party Bus Functional Model (BFM).

Related Information

- P-Tile Avalon Streaming (ST) IP for PCI Express User Guide
  For the Avalon-ST Interface to the Application Layer.
- Errata for the Hard IP for PCI Express IP Core in the Knowledge Base
- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.

1.7. P-Tile IP for PCI Express IP Cores v19.2

Table 23. 19.2 June 2019

Description	Impact
Initial release of the P-Tile Avalon-ST IP for PCI Express. This IP supports both Intel Stratix 10 DX and Intel Agilex devices.	Added this new IP component to enable Avalon-ST native support for P-Tile in the Gen3 x16/x8 for Endpoint, Gen4 x16/x8 for Endpoint, Gen3 x16/x4 for Root Port and Gen4 x16/x4 for Root Port configurations. The support level is Advance. Other configurations can be supported through link negotiations.
Support for Single-Root I/O Virtualization (SR-IOV) is available.	The P-Tile Avalon-ST IP for PCI Express supports up to 8 physical functions (PFs) and 2048 virtual functions (VFs) in SR-IOV mode.
Port bifurcation is supported.	This IP can support one x16 or two x8 interfaces in Endpoint mode, and four x4 interfaces in Root Port mode.
TLP Bypass mode is supported.	This IP supports a TLP Bypass mode for both upstream and downstream ports, thus allowing the implementation of advanced features such as: • The upstream port or downstream port of a switch. • A custom implementation of a Transaction Layer to meet specific user requirements.

1.8. P-Tile IPs for PCI Express User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

Quartus Version	User Guide
20.2	P-Tile Avalon Streaming (Avalon-ST) IP for PCI Express User Guide
20.2	P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCI Express User Guide
20.1	P-Tile Avalon Streaming (Avalon-ST) IP for PCI Express User Guide
20.1	P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCI Express User Guide
19.4	P-Tile Avalon Streaming (Avalon-ST) IP for PCI Express User Guide
19.4	P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCI Express User Guide

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Quartus Version	User Guide
19.3	P-Tile Avalon Memory Mapped (Avalon-MM) IP for PCI Express User Guide
19.3	P-Tile Avalon Streaming (Avalon-ST) IP for PCI Express User Guide
19.2	P-Tile Avalon Streaming (Avalon-ST) IP for PCI Express User Guide