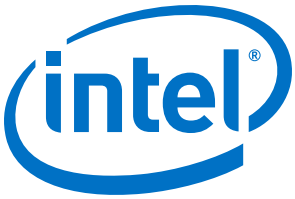

eSRAM Intel® FPGA IP Release Notes

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Contents

1. eSRAM Intel® Agilex™ FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Agilex™ Embedded Memory User Guide
- Errata for the eSRAM Intel Agilex™ FPGA IP in the Knowledge Base

1.1. eSRAM Intel Agilex™ FPGA IP v19.2.0

Table 1. v19.2.0 2020.12.14

Intel Quartus Prime Version	Description	Impact
19.4	Removed the dynamic ECC encoder and decoder bypass feature.	—

1.2. eSRAM Intel Agilex™ FPGA IP v19.1.1

Table 2. v19.1.1 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	Initial release for Intel Agilex™ devices.	—

1.3. Intel Agilex Embedded Memory User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
19.3	Intel Agilex Embedded Memory User Guide

2. eSRAM Intel FPGA IP Release Notes (Intel Stratix® 10 Devices)

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel Quartus Prime Design Suite Update Release Notes*.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Stratix® 10 Embedded Memory User Guide
- Errata for the eSRAM Intel FPGA IP in the Knowledge Base

2.1. eSRAM Intel FPGA IP v19.1.5

Table 3. v19.1.5 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Updated the description for **Enable Low Power Mode** in the eSRAM Intel FPGA IP parameter editor.	—

2.2. eSRAM Intel FPGA IP v19.1.4

Table 4. v19.1.4 2020.08.03

Intel Quartus Prime Version	Description	Impact
20.2	Renamed the I/O PLL filename to waive the warning message from the IOPLL file.	—

Intel Quartus Prime Version	Description	Impact
	If the two eSRAMs have the same PLL parameters (PLL reference clock frequency and PLL desired clock frequency), the warning message can be ignored. If the two eSRAMs have different PLL parameters, after compilation they will be set to the same PLL frequencies taken from one of the eSRAM Intel FPGA IP parameters. Refer to the **Quartus Fitter report ➤ Plan Stage ➤ PLL Usage Summary** to observe the implemented eSRAM IOPLL frequencies. IP update is needed when the PLL parameter for both eSRAM is different.	

2.3. eSRAM Intel FPGA IP v19.1.3

Table 5. v19.1.3 2019.10.11

Intel Quartus Prime Version	Description	Impact
19.3	Updated the description for **PLL Reference Clock Frequency** in the eSRAM Intel FPGA IP parameter editor.	—

2.4. eSRAM Intel FPGA IP v18.1

Table 6. v18.1 2018.10.03

Intel Quartus Prime Version	Description	Impact
18.1	Removed the HIPI register for `iopll_lock2core_reg`.	You may upgrade your IP core.

2.5. eSRAM Intel FPGA IP v18.0

Table 7. v18.0 May 2018

Description	Impact
Renamed Native eSRAM IP core to eSRAM Intel FPGA IP as per Intel rebranding.	—
Added a new interface signal: • `iopll_lock2core` eSRAM IOPLL lock status.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix® 10 Embedded Memory User Guide
- Errata for other IP cores in the Knowledge Base

2.6. Native eSRAM IP Core v17.1

Table 8. v17.1 November 2017

Description	Impact
Initial release. This IP core is available only in Intel Stratix® 10 devices.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Embedded Memory User Guide
- Errata for other IP cores in the Knowledge Base

2.7. Intel Stratix 10 Embedded Memory User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
20.1	Intel Stratix 10 Embedded Memory User Guide
19.1	Intel Stratix 10 Embedded Memory User Guide
18.1	Intel Stratix 10 Embedded Memory User Guide
18.0	Intel Stratix 10 Embedded Memory User Guide
17.1	Intel Stratix 10 Embedded Memory User Guide
17.0	Intel Stratix 10 Embedded Memory User Guide