



JESD204C Intel® FPGA IP Release Notes



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1. JESD204C Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- [Intel Quartus Prime Design Suite Update Release Notes](#)
- [Introduction to Intel FPGA IP Cores](#)
- [JESD204C Intel FPGA IP User Guide](#)
- [JESD204C Intel Agilex™ FPGA IP Design Example User Guide](#)
- [JESD204C Intel Stratix® 10 FPGA IP Design Example User Guide](#)
- [Errata for the JESD204C Intel FPGA IP in Knowledge Base](#)

1.1. JESD204C Intel FPGA IP v1.1.0

Table 1. v1.1.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
20.1	Updated the supported data rates for FPGA fabric speed grades for Intel Stratix® 10 and Intel Agilex™ E-tile devices.	-
	Added a new GUI parameter, Multilink mode . When enabled, the multilink mode implements synchronization between multiple JESD204C RX IP instances.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
	Added the following signals for multilink mode: <ul style="list-style-type: none"> • j204c_rx_dev_emblock_align • j204c_rx_alldev_emblock_align 	



Table 2. v1.1.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	Updated the supported maximum data rate to 28.9 Gbps for Intel Stratix 10 and Intel Agilex E-tile devices.	-
	Optimized area utilization for JESD204C RX IP.	
	Enabled hardware design example for Intel Agilex devices.	You can generate the design example using the Intel Agilex Signal Integrity development kit.

1.2. JESD204C Intel FPGA IP v1.0.0

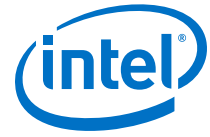
Table 3. v1.0.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Added advance support for Intel Agilex E-tile devices.	The Intel Agilex E-tile devices are now supported in the 19.3 version of the Intel Quartus Prime Pro Edition software. Upgrade your IP to use the new features.
	Added the following presets for Intel Agilex devices: <ul style="list-style-type: none">LMF = 2812, 24.333 GbpsLMF = 484, 16.222 Gbps You can simulate these presets through the Example Design tab in the JESD204C IP parameter editor.	

1.3. JESD204C Intel FPGA IP v1.0.0

Table 4. v1.0.0 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	Initial release for Intel Stratix 10 E-tile devices.	—



2. JESD204C Intel FPGA IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
19.4	1.1.0	JESD204C Intel FPGA IP User Guide
19.3	1.0.0	JESD204C Intel FPGA IP User Guide



3. JESD204C Intel Agilex FPGA IP Design Example User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
19.3	1.0.0	JESD204C Intel Agilex FPGA IP Design Example User Guide



4. JESD204C Intel Stratix 10 FPGA IP Design Example User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
19.2	1.0.0	JESD204C Intel Stratix 10 FPGA IP Design Example User Guide