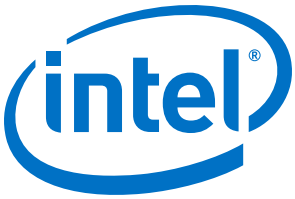

IOPLL Reconfig Intel FPGA IP Core Release Notes

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IOPLL Reconfig Intel FPGA IP Core Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Agilex™ Clocking and PLL User Guide
- Intel Stratix® 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

IOPLL Reconfig Intel FPGA IP v19.4.0

Table 1. v19.4.0 2020.06.22

Intel Quartus Prime Version	Description	Impact
20.2	Edited the `mgmt_waitrequest` signal to flip to the correct value when performing dynamic phase shift using the IOPLL Reconfig IP core for Intel Stratix® 10 devices.	You may upgrade your IP core.

IOPLL Reconfig Intel FPGA IP v19.3.0

Table 2. v19.3.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Added support for Intel Agilex™ devices.	—

IOPLL Reconfig Intel FPGA IP v18.0

Table 3. v18.0 May 2018

Description	Impact
Renamed Intel FPGA IOPLL Reconfig IP core to IOPLL Reconfig Intel FPGA IP core as per Intel rebranding.	—
Added advanced reconfiguration mode to dynamically reconfigure specific I/O PLL addresses.	Any incorrect settings may cause damage to the device.

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA IOPLL Reconfig v17.1

Table 4. v17.1 November 2017

Description	Impact
Initial release. This IP is available only in Intel Stratix 10 devices.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Clocking and PLL User Guide
- Errata for other IP cores in the Knowledge Base

Intel Stratix 10 Clocking and PLL User Guide Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
19.2	Intel Stratix 10 Clocking and PLL User Guide
18.1	Intel Stratix 10 Clocking and PLL User Guide
18.0	Intel Stratix 10 Clocking and PLL User Guide
17.1	Intel Stratix 10 Clocking and PLL User Guide

Intel Agilex Clocking and PLL User Guide Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
19.3	Intel Agilex Clocking and PLL User Guide