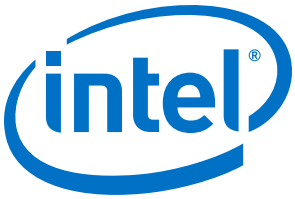

Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Version 2.0 Release Notes

For the Intel FPGA Programmable Acceleration Card D5005

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **2.0**

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Latest document on the web: **PDF** | **HTML**

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Notice

Please note that the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs DOES NOT include mitigations for the exploits known as Spectre (CVE-2017-5753, CVE-2017-5715) and Meltdown (CVE-2017-5754). These exploits require that malware runs locally on the system, which is not normally possible in a closed environment where the system's software is centrally controlled. Intel does not recommend that an un-mitigated version of the Intel Acceleration Stack for Intel Xeon CPU with FPGAs be used in an environment that is not a closed system environment.

Intel Acceleration Stack for Intel Xeon CPU with FPGAs Version 2.0 Release Notes for the Intel FPGA PAC D5005

This document provides up-to-date information about the Intel Acceleration Stack for Intel Xeon CPU with FPGAs version 2.0 release for the Intel FPGA PAC D5005.

Acceleration Acronym List

Use the following table as a reference when reviewing the release notes.

Table 1. Acronyms

Acronyms	Expansion	Description
AFU	Accelerator Functional Unit	Hardware Accelerator implemented in FPGA logic which offloads a computational operation for an application from the CPU to improve performance.
AF	Accelerator Function	Compiled Hardware Accelerator image implemented in FPGA logic that accelerates an application. An AFU and associated AFs may also be referred to as GBS (Green-Bits, Green BitStream) in the Acceleration Stack installation directory tree and in source code comments.
ASE	AFU Simulation Environment	Co-simulation environment that allows you to use the same host application and AF in a simulation environment. ASE is part of the Intel Acceleration Stack for FPGAs.
FIM	FPGA Interface Manager	The FPGA hardware containing the FPGA Interface Unit (FIU) and external interfaces for memory, networking, etc. The FIM may also be referred to as BBS (Blue-Bits, Blue BitStream) in the Acceleration Stack installation directory tree and in source code comments. The Accelerator Function (AF) interfaces with the FIM at run time.
HSSI	High-speed Serial Interface	Reference to the multi-gigabit serial transceiver I/O in the FIM and the corresponding interface to the Accelerator Functional Unit (AFU).

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Acronyms	Expansion	Description
OPAE	Open Programmable Acceleration Engine	The OPAE is a software framework for managing and accessing AFs.
PIM	Platform Interface Manager	An abstraction layer for managing top-level device ports and system-provided clock crossing.
PR	Partial Reconfiguration	The ability to dynamically reconfigure a portion of an FPGA while the remaining FPGA design continues to function.

Minimum Requirements

The minimum requirements for the Intel FPGA Programmable Acceleration Card D5005 must include:

- Intel Xeon Scalable processor
- A PCI Express* x16 Slot
- 128 GB of free memory is a requirement only if you are compiling a hardware design
- Operating System:
  - Red Hat* Enterprise Linux* (RHEL) version 7.6 Kernel 3.10.0-957

Intel Acceleration Stack Reference Table

Table 2. Intel Acceleration Stack Best Known Configuration

Note: When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as bfac4d85-1ee8-56fe-8c95-865ce1bbaa2d.

Intel Acceleration Stack Version	Platform	FPGA Interface Manager (FIM) Version: Partial Reconfiguration (PR) Interface ID	Open Programmable Acceleration Engine (OPAE) Version	Intel Quartus® Prime Pro Edition	Board Management Controller (BMC) RTL version	BMC firmware version
2.0	Intel FPGA PAC D5005	bfac4d85-1ee8-56fe-8c95-865ce1bbaa2d	1.1.4-3	18.1.2	1.0.15	1.0.12
2.0 Pre-Beta	Intel FPGA PAC D5005	a9f2d0f3-b398-57b0-b34fd226bf364fee	1.1.4-1	18.1	1.0.6	1.0.6

Intel Acceleration Stack v2.0 Features

Table 3. Features of the Intel Acceleration Stack v2.0

Feature	Description
PCIe Gen3x16	The FPGA communicates with the host CPU through PCIe Gen3x16 interface provided by the Intel Stratix® 10.
Partial Reconfiguration Support	Provides the ability to dynamically swap out an AFU within the FIM.
Remote Signal Tap	Provides the ability to debug over the PCIe link. This feature combines virtual JTAG IP and the system console remote debugging capability.
Remote Flash Update	Supports in-band updates of board management controller image on the board management controller and updates to the FPGA image in QSPI flash.
Multi-card Support	Allows for more than one Intel FPGA PAC D5005 card to be inserted into the system.
Virtualization	The Intel Stratix 10 provides virtualization capability by being SR-IOV enabled PCIe endpoint.
Interrupts	Supports physical function (PF) to virtual function (VF) communication through interrupts.
Networking Support	High-Speed Serial Interface (HSSI) PHY support for 8x10GbE.
Telemetry support through OPAE	Provides telemetry data using the OPAE `fpgainfo` command.
Board sensor, thermal and power monitoring	Provides board sensor, temperature and power data using the OPAE `fpgainfo` command and graceful thermal and power handling using the OPAE `pacd` service.
Sample AFUs	The following AFUs examples are provided with the Intel Acceleration Stack for Intel Xeon CPU with FPGAs: • dma_afu • streaming_dma_afu • eth_e2e_e10 • hello_afu • hello_mem_afu • hello_intr_afu • nlb_mode_0 • nlb_mode_0_stp • nlb_mode_3
DDR4 memory	32GB DDR4 divided into 4 banks of 8GB with error checking and correction (ECC).
Operating System	Supports Red Hat* Enterprise Linux (RHEL) 7.6 Kernel version 3.10.0-957.
OPAE	Provides integrated OPAE APIs. • Support for fpgaflash command • Support for fpgainfo command with telemetry
Intel Accelerator Functional Unit (AFU) Simulation Environment (ASE)	Co-simulation environment support for validating AFU compliance to protocols and APIs.

Known Issues for the Intel Acceleration Stack v2.0

Table 4. Known Issues for the Intel Acceleration Stack v2.0

Known Issue	Details
The system is unable to recover after a corrupted AFU is loaded onto the Intel FPGA PAC D5005.	• Workaround: To recover after loading a corrupted AFU onto the Intel FPGA PAC D5005, power cycle the card. • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack.
OPAE does not verify the images it loads on the Intel FPGA PAC D5005.	• Workaround: You must ensure that the images you program on the Intel FPGA PAC D5005 come from a known and trusted source. • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack.

A partial reconfiguration (PR) compile using OpenCL* may produce hold time violations in the static regions.	• Workaround: Recompile using a different seed with the command:
	`aoc <kernal_name.cl> -seed=<integer>`
	For example:
	`aoc hello_world.cl -seed=5`
	• Status: This limitation will be fixed in a future version of the Intel Acceleration Stack.

Invalid memory read fault may cause FIM to lock.	• The FIM locks after the AFU sends a memory read to invalid address. • Workaround: Power cycle the system to reinitialize the Intel FPGA PAC and recover from this issue. Refer to the Knowledge Base entry for more information. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
At boot, the Intel FPGA PAC D5005 may respond to configuration read requests with non-fatal PCIe errors.	• The Intel FPGA PAC D5005 responds to configuration read requests to functions that do not exist by returning `NonFatalErr+` error responses. You can clear and ignore these errors after boot. • Workaround: Clear the relevant errors at boot: `sudo setpci -s BDF ECAP_AER+0x10.L=0xFFFFFFFF` • Status: Fix targeted for a future version of the Intel Acceleration Stack.
When a `pacd` sensor trips and continues to be be tripped, `pacd` prints the state of the sensor at a cadence exponential to the configured polling interval.	• Sensor output data results do not print in synchronization with the polling frequency. The frequency of the result output is equal to (*polling_interval_value*) multiplied by 256 seconds. For example, if the polling interval is 0, results print every second. If the interval is 1, results print every 256 seconds. • Workaround: Use `fpgainfo` command to read sensor data when required. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
The `fpgainfo` command returns non-critical errors that can be ignored.	• When you run the `fpgainfo` command you can ignore the following results: — `Last Power Down Cause: unavailable` — `Last Reset Cause: unavailable (can't open)` — `Socket Id : 0x00` • Workaround: None available. • Status: Fix targeted for a future version of the Intel Acceleration Stack.

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Known Issue	Details
The `fpgaflash` BDF value is case sensitive.	• Workaround: When specifying BDF for card identification, you must use lowercase letters. For example, use `0000:d8:00.0` instead of `0000:D8:00.0`. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
The Intel FPGA PAC D5005 does not support optical module cables that require the `ResetL` pin to be driven high for link up to complete.	• Workaround: None available. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
The `/var/log/message` file includes error messages on invalid rules that are not active.	• You can ignore the following invalid rules: — `invalid rule '/etc/udev/rules.d/40-intel-fpga.rules:1'` — `invalid ACTION operation` — `invalid rule '/etc/udev/rules.d/40-intel-fpga.rules:2'` • Workaround: None available. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
After a cold boot, SPI reads from the host to the BMC using the OPAE `fpgainfo bmc` command may not complete.	• Workaround: Power cycle the system. • Status: This limitation will be fixed in a future version of the board management controller firmware.
QSFP link and activity LEDs do not reflect Ethernet link status.	• Workaround: None available. • Status: This limitation will be fixed in a future version of the board management controller firmware.

Known Issues for the Intel Acceleration Stack v2.0 AFU Design Examples

Table 5. Known Issues for the Intel Acceleration Stack v2.0 AFU Design Examples

Known Issue	Details

Compilation of `nlb_mode_3` AFU from source produces incorrect `nlb_400.gbs` output.	• Workaround:
	1. Change the default setting in `$OPAE_PLATFORM_ROOT/hw/samples/nlb_mode_3/hw/rtl/filelist.txt` from
	`C:filelist_mode_0.txt`
	to
	`C:filelist_mode_3.txt`
	2. Follow the AFU compilation steps as detailed in the *Accelerator Functional Unit (AFU) Developer's Guide*.
	• Status: This limitation will be fixed in a future version of the Intel Acceleration Stack.

The `streaming_dma_afu` may contain timing violations.	• Workaround: No workaround available. • Status: This limitation will be fixed in a future version of the Intel Acceleration Stack.
The `dma_afu` may access an invalid host memory address causing a Translation Layer Packet Completion Status error (`TLP CPL status error`).	• The `dma_afu` may attempt to fetch descriptors after the driver has deallocated memory. • Workaround: None available. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
When you test the 10Gbps Ethernet AFU in loopback mode, it loses a single packet after hot plug.	• Workaround: Reset the Intel FPGA Low Latency 10GbE MAC IP core before transmitting data as described in the *Accelerator Functional Unit (AFU) Developer's Guide for the Intel FPGA Programmable Acceleration Card*. • Status: Fix targeted for a future version of the Intel Acceleration Stack.
After initial programming of the `dma_afu` subsequent partial reconfigurations may cause the kernel message to report errors.	• You can ignore the kernel messages because they do not affect functionality of the `dma_afu`. • Workaround: None available. • Status: Fix targeted for a future version of the Intel Acceleration Stack.

Revision History for the Intel Acceleration Stack for Intel Xeon CPU with FPGAs v2.0 Production Release Notes

Date	Acceleration Stack Version	Changes
2019.08.05	2.0 (compatible with Intel Quartus Prime Pro Edition 18.1.2)	Initial Public Release.