Hybrid Memory Cube Controller IP Core Release Notes

2016.05.02

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If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Altera Complete Design Suite Update Release Notes*.

Related Information

Altera Complete Design Suite Update Release Notes

Hybrid Memory Cube Controller IP Core v16.0

Table 1: Version 16.0 May 2016

Description	Impact	Notes
Added support for multiple (2, 3, or 4) data interfaces in full-width variations. • New **Ports** parameter specifies the number of ports (1, 2, 3, or 4). • New signals for the additional interfaces. Signal names on data path interfaces, in the case of more than one port, are `dp<n>_req_*` and `dp<n>_rsp_*` where `<n>` is the port number (0, 1, 2, 3).	The IP core has new signals to support multiple data interfaces for full-width variations.	You must upgrade to the 16.0 version of the IP core if you use the Quartus® Prime software v16.0.
Added new **Response re-ordering** parameter for full-width variations, to specify that the IP core should return responses on each data response interface in the order it received the original requests on the corresponding data request interface.	When you turn on this new option, the IP core implements tag management internally, and the tags are not visible on the data interfaces.	
Expanded list of supported transactions by adding non-power of two payload sizes for READ, WRITE, and Posted WRITE transactions in full-width variations.	Full-width variations now support all transaction types that half-width variations support.	
Changed name of **Enable Altera Debug Master Endpoint (ADME)** parameter to **Enable ADME and Optional Reconfiguration Logic**. Added list of PHY debugging features the parameter sets.	The IP core no longer supports the ODI acceleration logic feature.	

Description	Impact	Notes
Restricted list of allowed values for the **CDR reference clock** parameter to standard HMC reference clock frequencies.	Supported CDR clocks: • 125, 156.25, and 166.67 Mhz (10G) • 125 and 156.25 Mhz (12.5G)	
Added new data path response interface signal `dp<n>_rsp_errstat[6:0]`.	This signal holds the value of the `ERRSTAT` field of the response packet from the external HMC.	
Removed `pll_powerdown` output signal.		
Updated description of `dp<n>_rsp_error` signal to indicate that the IP core now maintains the value of `dp<n>_rsp_error` for the duration of a multi-cycle transaction. Previously this behavior was not guaranteed.		
Added new Limit Outstanding FLITs feature for full-width variations to mitigate read response congestion. Added new `LIMIT_OUTSTANDING_PACKET` register to control the feature.	The IP core supports the Limit Outstanding FLITs feature for full-width variations.	
Added software control for reset, link reinitialization, fatal error recovery, and power management. Added the following fields to the `CONTROL` register: • `P_RST_N` in bit [17]: software controlled reset of the HMC. • `TXPS` in bit [16]: Power management field. • `SoftReset` in bit [2]: software-controlled reset of the IP core. • `Retrain` in bit [0]: Restart IP core link initialization sequence.		
Design Example Errata		
During compilation, the Quartus Prime Pro Edition software issues the following critical warning: Critical Warning(18226): Physical Synthesis has been replaced by Spectra-Q Physical Synthesis for the Arria 10 device family, but there are still Physical Synthesis assignments in the project's Quartus Settings File (.qsf). Support for these assignments will be discontinued in the next release of the Quartus Prime software.	This message is a warning, not a critical warning.	
The design example asserts the `registers_loaded` trigger too late, causing an Init Continue ERI status 0x12 (initialization timeout).	Designers can ignore the initialization error.	

Description	Impact	Notes
After you make the design example simulation scripts, the directory structure contains directories for VCSMX and Aldec, however, the IP core does not support these simulators.		
During compilation, the Fitter may issue base clock assignment warnings.	Designers can ignore the Fitter base clock assignment warning.	
The design example contains unconstrained output ports.	Designers can ignore these unconstrained ports.	

Related Information

- **Hybrid Memory Cube Controller IP Core User Guide**
- **Hybrid Memory Cube Controller Design Example User Guide**
- **Errata for Hybrid Memory Cube Controller IP core in the Knowledge Base**

Hybrid Memory Cube Controller IP Core v15.1

Table 2: Version 15.1 November 2015

Description	Impact	Notes
Enhanced ADME feature. When you turn on the **Enable Altera Debug Master Endpoint (ADME)** parameter the IP core enables an additional Arria 10 Transceiver PHY IP core feature. In the 15.0 release, turning on the parameter turned on these Arria 10 PHY features: • **Enable capability registers** • **Enable control and status registers** • **Enable prbs soft accumulators** In the 15.1 release, the parameter also turns on this Arria 10 PHY feature: • **Enable odi acceleration logic**	This feature does not affect the top-level signals of the IP core.	You must upgrade to the 15.1 version of the IP core if you use the Quartus Prime software v15.1.

Related Information

- **Hybrid Memory Cube Controller IP Core User Guide**
- **Errata for Hybrid Memory Cube Controller IP core in the Knowledge Base**

Hybrid Memory Cube Controller IP Core v15.0

Table 3: Version 15.0 May 2015

Description	Impact	Notes
Initial public release.		

Related Information

- Hybrid Memory Cube Controller IP Core User Guide
- Errata for Hybrid Memory Cube Controller IP core in the Knowledge Base