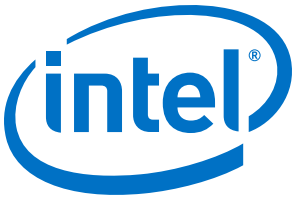

High-Definition Multimedia Interface (HDMI) Intel FPGA IP Release Notes

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1. Intel FPGA HDMI IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- HDMI Intel FPGA IP User Guide
- HDMI Intel Arria 10 FPGA IP Design Example User Guide
- HDMI Intel Cyclone 10 GX IP FPGA Design Example User Guide
- HDMI Intel Stratix 10 FPGA IP Design Example User Guide
- Errata for HDMI Intel FPGA IP in the Knowledge Base

1.1. HDMI Intel FPGA IP v19.6.0

Table 1. v19.6.0 2020.12.14

Intel Quartus Prime Version	Description	Impact
20.4	Added support for HDMI 2.1 with fixed rate link (FRL) enabled for Intel Stratix® 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.

1.2. HDMI Intel FPGA IP v19.5.0

Table 2. v19.5.0 2020.09.28

Intel Quartus Prime Version	Description	Impact
20.3	The HDMI Intel FPGA IP is repackaged. Added the following new parameters to include a RAM for storing EDID and I^2C master or slave depending on the selected direction. • Include I2C • Include EDID RAM • EDID RAM size • RAM file path • HPD polarity	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
	Made changes in the interface as a result of the repackaging. Refer to the *Source Interfaces* and *Sink Interfaces* section in the *HDMI Intel FPGA IP User Guide* for more information.	

1.3. HDMI Intel FPGA IP v19.4.0

Table 3. v19.4.0 2020.06.22

Intel Quartus Prime Version	Description	Impact
20.2	Added support for High-bandwidth Digital Content Protection (HDCP) feature for Intel Stratix 10 devices. This feature has also been available for Intel Arria® 10 devices since the Intel Quartus Prime Pro Edition software version 19.3 and later.	The HDCP feature is not included in the Intel Quartus Prime Pro Edition software. To access the HDCP feature, contact Intel at https://www.intel.com/content/www/us/en/broadcast/products/programmable/applications/connectivity-solutions.html.

Table 4. v19.4.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
20.1	Added support for deep color implementation for HDMI 2.1 with fixed rate link (FRL) enabled. HDMI 2.1 is available only for Intel Arria 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
	Enabled a DIP switch (`dipsw`) for HDMI 2.1 design examples. The switch enables you to toggle between passthrough mode and independent RX and TX mode, which can operate at different link rates.	

1.4. HDMI Intel FPGA IP v19.3.0

Table 5. v19.3.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	Added support for HDMI 2.1 with fixed rate link (FRL) enabled for Intel Arria 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
	Added the **Support FRL** parameter in the HDMI Intel FPGA IP parameter editor.	

1.5. HDMI Intel FPGA IP v19.1

Table 6. v19.1 April 2019

Description	Impact
Enabled final support for Intel Stratix 10 L-tile and H-tile devices. The design examples now target Intel Stratix 10 production devices.	If you want to target your designs to use Intel Stratix 10 L-tile devices, you must upgrade your IP core.

1.6. HDMI Intel FPGA IP v18.1 Update 1

18.1.1 December 2018

- For Intel Stratix 10 H-Tile devices, added VID_OPERATION_MODE "PMBUS MASTER" and PWRMGMT settings to the video connectivity design example IP `.qsf` file to enable Intel Stratix 10 SmartVID and power management capabilities.

Related Information

- Introduction to Intel FPGA IP Cores
- HDMI Intel FPGA IP User Guide
- HDMI Intel Arria 10 FPGA Design Example User Guide
- HDMI Intel Cyclone 10 GX FPGA Design Example User Guide
- HDMI Intel Stratix 10 FPGA Design Example User Guide
- Errata for HDMI Intel FPGA IP in the Knowledge Base

1.7. HDMI Intel FPGA IP v18.1

Table 7. v18.1 September 2018

Description	Impact
Improved the HDMI RX video lock time for HDMI 2.0 for Intel Stratix 10 design examples.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for Bitec HDMI FMC daughter card revision 11 in the Intel Arria 10, Intel Cyclone® 10 GX, and Intel Stratix 10 design examples.	

Related Information

- Introduction to Intel FPGA IP Cores
- HDMI Intel FPGA IP User Guide

- HDMI Intel Arria 10 FPGA Design Example User Guide
- HDMI Intel Cyclone 10 GX FPGA Design Example User Guide
- HDMI Intel Stratix 10 FPGA Design Example User Guide
- Errata for HDMI Intel FPGA IP in the Knowledge Base

1.8. HDMI Intel FPGA IP v18.0

Table 8. v18.0 May 2018

Description	Impact
Renamed Intel FPGA HDMI IP to HDMI Intel FPGA IP as part of standardizing and rebranding exercise.	–
Added preliminary support for Intel Stratix 10 (H-Tile) devices.	The Intel Stratix 10 devices are only available in the Intel Quartus Prime Pro Edition software.
Updated the HDMI Intel FPGA IP to support *HDMI Specification 2.0b*.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for Xcelium* Parallel simulator.	
Added the following files: • `xcelium_files.tcl` • `xcelium_setup.sh` • `xcelium_sim.sh`	
Added support for SCDC read request feature in the HDMI RX core.	
Added final support for Intel Cyclone 10 GX devices.	The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.
Added new design examples for Intel Cyclone 10 GX devices in version 17.1.1 release. Refer to the *HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide* for more information.	

Table 9. Design Files Required for IP Upgrade

The implementation of the IP on hardware requires additional components specific to the device targeted.

These additional components, such as Native PHY, TX PLL, reconfiguration controller, are not included as part of the Intel Quartus Prime IP Upgrade flow. Upgrading an IP core would require the inclusion of these files generated as part of the IP design example.

Design Example	Required Files
Intel Arria 10	• `quartus\a10_hdmi2_demo.qsf` • `rtl\gxb\gxb_tx_fpll.qsys`—regenerate before you compile in the Intel Quartus Prime software. • `rtl\hdmi_rx\hdmi_rx_top.v` • `rtl\hdmi_rx\mr_hdmi_rx_core_top.v` • `rtl\reconfig_mgmt\mr_reconfig_mgmt.v` • `rtl\sdc\a10_hdmi2.sdc` • `rtl\a10_hdmi2_demo.v`
Intel Cyclone 10 GX	• `quartus\c10_hdmi2_demo.qsf` • `rtl\sdc\c10_hdmi2.sdc` • `sdc\mr_clock_sync.sdc` • `rtl\sdc\mr_reconfig_mgmt.sdc`

continued...

Design Example	Required Files
	• rtl\sdc\rxtx_link.sdc • rtl\c10_hdmi2_demo.v • rtl\xcvr_transceiver_arbiter.v

Related Information

- Introduction to Intel FPGA IP Cores
- HDMI Intel FPGA IP User Guide
- HDMI Intel Arria 10 FPGA Design Example User Guide
- HDMI Intel Cyclone 10 GX FPGA Design Example User Guide
- HDMI Intel Stratix 10 FPGA Design Example User Guide
- Errata for HDMI Intel FPGA IP in the Knowledge Base

1.9. Intel FPGA HDMI IP Core v17.1

Table 10. v17.1 November 2017

Description	Impact
Renamed the following as per Intel rebranding: • HDMI IP core to Intel FPGA HDMI IP core • Qsys to Platform Designer	–
The **Support for deep color** parameter is now turned on by default.	–
Added advance support for Intel Cyclone 10 GX devices.	The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.
Added support for up to 32 audio channels.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for up to 1,536 kHz audio sample frequency.	
In previous versions of the Intel FPGA HDMI design example for Intel Arria 10 devices, the IOPLL and transceiver PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in the Intel Quartus Prime software version 17.1.	If you are upgrading designs that have these additional constraints from the previous versions of the Intel Quartus Prime software to version 17.1, you must revise the constraints. Refer to the KDB page for more information.

Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA HDMI User Guide
- Intel FPGA HDMI Design Example User Guide for Intel Arria 10 Devices
- Errata for Intel FPGA HDMI IP Core in the Knowledge Base

1.10. HDMI IP Core v17.0

Table 11. v17.0 May 2017

Description	Impact
Available in both Quartus Prime Pro Edition and Quartus Prime Standard Edition.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added demonstration for HDR InfoFrame insertion and filtering.	
Changed to FPLL direct for TX transceiver.	
Enabled TX PMA recalibration.	

Related Information

- Introduction to Intel FPGA IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- HDMI Design Example User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.11. HDMI IP Core v16.1

Table 12. v16.1 October 2016

Description	Impact
The 16.1 version of the HDMI IP core is available only in Quartus Prime Standard Edition.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added new **Design Example** tab in the HDMI IP core parameter editor. The design example is for Arria 10 devices. Refer to the *HDMI IP Core Design Example User Guide* for more information.	
Changed `audio_de` port width to 1 bit.	
Added EDID information pass trough from external sink to external source through the FPGA in the Arria 10 design example.	
Removed **Support 8-channel audio** parameter. The IP core supports 8-channel audio by default.	
Added version output port.	

Related Information

- Introduction to Intel FPGA IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- HDMI Design Example User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.12. HDMI IP Core v16.0

Table 13. v16.0 May 2016

Description	Impact
Added Audio Metadata Packet to comply to *HDMI Specification Version 2.0*.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added new interface ports: • HDMI source — `audio_metadata[164:0]` — `audio_format[4:0]` • HDMI sink — `audio_metadata[164:0]` — `audio_format[4:0]` — `vid_lock` — `aux_error`	

Related Information

- Introduction to Intel FPGA IP Cores
- Altera High-Definition Multimedia Interface User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.13. HDMI IP Core v15.1

Table 14. v15.1 November 2015

Description	Impact
Added the following new GUI parameters: • HDMI source — **Support for 8-channel audio** — **Support for deep color** • HDMI sink — **Support for 8-channel audio** — **Support for deep color** — **Manufacturer OUI** — **Device ID String** — **Hardware Revision**	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated the following interface ports: • HDMI source — Added `ctrl` — Removed `gcp_Set_AVMute` and `gcp_Clear_AVMute` • HDMI sink — Added `ctrl`, `mode`, `in_5v_power`, and `in_hpd` — Removed `gcp_Set_AVMute` and `gcp_Clear_AVMute`	

Related Information

- Introduction to Altera IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.14. HDMI IP Core v15.0 Update 1

Table 15. v15.0 Update 1 June 2015

Description	Impact
Fixed the timing violation on the oversampling block in the Arria V HDMI 2.0 design.	Upgrade if you are using the Arria V HDMI 2.0 design.

Related Information

- Introduction to Altera IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.15. HDMI IP Core v15.0

Table 16. v15.0 May 2015

Description	Impact
Upgraded support for HDMI specification compliance from version 1.4b to 2.0.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added 4 symbols per clock.	
Added Status and Control Data Channel (SCDC) for HDMI specification version 2.0.	
Added the following interface ports: • HDMI source — `TMDS_Bit_clock_Ratio` — `Scrambler_Enable` • HDMI sink — `TMDS_Bit_clock_Ratio` • Avalon-MM SCDC Management — `scdc_i2c_clk` — `scdc_i2c_addr[7:0]` — `scdc_i2c_r` — `scdc_i2c_rdata[31:0]` — `scdc_i2c_w` — `scdc_i2c_wdata[31:0]`	

Related Information

- Introduction to Altera IP Cores
- High-Definition Multimedia Interface (HDMI) User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.16. HDMI IP Core v14.1

Table 17. v14.1 December 2014

Description	Impact
Initial release.	-

Related Information

- Introduction to Altera IP Cores

- High-Definition Multimedia Interface (HDMI) User Guide
- Errata for HDMI IP Core in the Knowledge Base

1.17. HDMI Intel FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to 19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.2	19.4.0	HDMI Intel FPGA IP User Guide
20.1	19.4.0	HDMI Intel FPGA IP User Guide
19.4	19.3.0	HDMI Intel FPGA IP User Guide
19.3	19.1.0	HDMI Intel FPGA IP User Guide
19.1	19.1	HDMI Intel FPGA IP User Guide
18.1	18.1	HDMI Intel FPGA IP User Guide
18.0	18.0	HDMI Intel FPGA IP User Guide
17.1	17.1	HDMI IP Core User Guide
17.0	17.0	HDMI IP Core User Guide
16.1	16.1	HDMI IP Core User Guide
16.0	16.0	HDMI IP Core User Guide
15.1	15.1	HDMI IP Core User Guide
15.0	15.0	HDMI IP Core User Guide
14.1	14.1	HDMI IP Core User Guide

1.18. HDMI Intel Arria 10 FPGA IP Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to 19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.1	19.4.0	HDMI Intel Arria 10 FPGA IP Design Example User Guide
19.4	19.3.0	HDMI Intel Arria 10 FPGA IP Design Example User Guide
18.1	18.1	HDMI Intel Arria 10 FPGA IP Design Example User Guide
17.1	17.1	Intel HDMI IP Design Example User Guide for Intel Arria 10 Devices
17.0	17.0	Intel Arria 10 HDMI IP Core Design Example User Guide
16.1	16.1	HDMI IP Core Design Example User Guide

1.19. HDMI Intel Cyclone 10 GX FPGA IP Design Example User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
18.1	18.1	Intel FPGA HDMI Design Example User Guide for Intel Cyclone 10 GX Devices
17.1.1	17.1.1	Intel FPGA HDMI Design Example User Guide for Intel Cyclone 10 GX Devices

1.20. HDMI Intel Stratix 10 FPGA IP Design Example User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.3	19.5.0	HDMI Intel Stratix 10 FPGA IP Design Example User Guide
20.2	19.4.0	HDMI Intel Stratix 10 FPGA IP Design Example User Guide
19.1	19.1	HDMI Intel Stratix 10 FPGA IP Design Example User Guide
18.0	18.0	HDMI Intel Stratix 10 FPGA IP Design Example User Guide