



# Generic Serial Flash Interface Intel FPGA IP Release Notes



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## Generic Serial Flash Interface Intel® FPGA IP Release Notes

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If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

### Related Information

- [Intel Quartus Prime Design Suite Update Release Notes](#)
- [Generic Serial Flash Interface Intel FPGA IP User Guide Archives](#)
- [Errata for the Generic Serial Flash Interface Intel FPGA IP in the Knowledge Base](#)

## Generic Serial Flash Interface Intel FPGA IP v20.0.0

**Table 1. v20.0.0 2020.09.28**

Intel Quartus Prime Version	Description	Impact
20.3	<p>Added a new register setting for the Generic Serial Flash Interface Intel FPGA IP in the Intel Quartus Prime Pro Edition software:</p> <ul style="list-style-type: none"> <li>• tSHSL This register controls the tSHSL. <ul style="list-style-type: none"> <li>— 0: tSHSL is 3 IP_CLK.</li> <li>— n: tSHSL is 3+n IP_CLK.</li> </ul> </li> </ul>	—



## Generic Serial Flash Interface Intel FPGA IP v19.2.1

Table 2. v19.2.1 2020.04.13

Intel Quartus Prime Version	Description	Impact
20.1	Enhanced byteenable feature in the Generic Serial Flash Interface Intel FPGA IP: <ul style="list-style-type: none"> <li>Added a new GUI parameter—<b>Use byteenable for CSR</b>.</li> <li>Added a new CSR byte enable signal—<code>avl_csr_byteenable[3:0]</code>.</li> </ul>	—

## Generic Serial Flash Interface Intel FPGA IP v19.1.1

Table 3. v19.1.1 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	Enhanced the Generic Serial Flash Interface Intel FPGA IP byteenable feature on Avalon® memory-mapped interface: <ul style="list-style-type: none"> <li>Added additional support for Generic Serial Flash Interface byteenable patterns.</li> </ul>	—

## Generic Serial Flash Interface Intel FPGA IP v19.1.0

Table 4. v19.1.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Added support for the Intel Agilex™ device family.	This device is only available in Intel Quartus Prime Pro Edition software version 19.3 onwards.

## Generic Serial Flash Interface Intel FPGA IP Core v18.0

Table 5. v18.0 May 2018

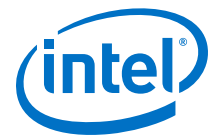
Description	Impact
Initial release	-

## Generic Serial Flash Interface Intel FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.1	19.2.1	<a href="#">Generic Serial Flash Interface Intel FPGA IP User Guide</a>
19.4	19.1.1	<a href="#">Generic Serial Flash Interface Intel FPGA IP User Guide</a>
<i>continued...</i>		



<b>Intel Quartus Prime Version</b>	<b>IP Core Version</b>	<b>User Guide</b>
19.3	19.1	<a href="#">Generic Serial Flash Interface Intel FPGA IP Core User Guide</a>
18.1	18.1	<a href="#">Generic Serial Flash Interface Intel FPGA IP Core User Guide</a>
18.0	18.0	<a href="#">Generic Serial Flash Interface Intel FPGA IP Core User Guide</a>