



E-Tile CPRI PHY Intel FPGA IP Release Notes



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1. E-Tile CPRI PHY Intel FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- [Intel Quartus Prime Design Suite Update Release Notes](#)
- [Introduction to Intel FPGA IP Cores](#)
- [E-tile Hard IP for Ethernet and CPRI PHY Intel FPGA IPs User Guide](#)
- [E-tile Hard IP Intel Stratix 10 FPGA IP Design Examples User Guide: Ethernet, CPRI PHY, and Dynamic Reconfiguration](#)
- [Errata for the E-Tile CPRI PHY Intel FPGA IP in the Knowledge Base](#)

1.1. E-Tile CPRI PHY Intel FPGA IP v19.4.0

Table 1. v19.4.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	Added support for Intel Agilex™ devices with E-tile transceivers	—
	Added support for the following CPRI line rates: <ul style="list-style-type: none"> • 3.0720 Gbps • 6.1440 Gbps • 10.1316 Gbps with RS-FEC • 12.1651 Gbps with and without RS-FEC 	—
	Added new parameter: RSFEC Clocking Mode	—



1.2. E-Tile CPRI PHY Intel FPGA IP v19.2.0

Table 2. v19.2.0 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	The IP supports the following new CPRI line rates: <ul style="list-style-type: none"> • 2.4376 Gbps • 4.9152 Gbps • 9.8304 Gbps • 24.33024 Gbps without RS-FEC 	—
	Added the following new parameters: <ul style="list-style-type: none"> • First RSFEC Lane • Enable reconfiguration to 8b/10b datapath 	—
	The IP now supports 8b/10b interface and status interface for the 8b/10b line rate.	—

1.3. E-Tile CPRI PHY Intel FPGA IP v19.1

Table 3. v19.1 April 2019

Description	Impact
Initial release for Intel Stratix® 10 devices.	—

1.4. E-tile Hard IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
19.3	E-tile Hard IP User Guide: E-tile Hard IP for Ethernet and E-Tile CPRI PHY Intel FPGA IPs
19.2	E-tile Hard IP User Guide: E-tile Hard IP for Ethernet and E-Tile CPRI PHY Intel FPGA IPs
19.1	E-tile Hard IP for Ethernet Intel FPGA IP User Guide
18.1.1	E-tile Hard IP for Ethernet Intel FPGA IP User Guide
18.0	E-tile Hard IP for Ethernet Intel FPGA IP User Guide