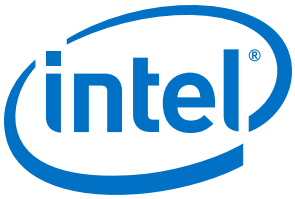

eCPRI Intel® FPGA IP Release Notes

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1. eCPRI Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- eCPRI Intel FPGA IP User Guide
- eCPRI Intel FPGA IP Design Example User Guide

1.1. eCPRI Intel FPGA IP v1.0.0

Table 1. v1.0.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
19.4	Initial release.	—

1.2. eCPRI Intel FPGA IP v1.1.0

Table 2. v1.1.0 2020.05.18

Intel Quartus Prime Version	Description	Impact
20.1	Added support for Intel Arria® 10 devices.	—
	The IP supports 10G data rate for Intel Stratix® 10 and Intel Arria 10 devices.	—
	Added following new parameters: • **Streaming** • **Pair with ORAN** • **One-way Delay Measurement Timer Bitwidth** • **Remote Memory Access Timer Bit-width** • **Remote Reset Timer Bit-width**	—

1.3. eCPRI Intel FPGA IP v1.2.0

Table 3. v1.2.0 2021.01.08

Intel Quartus Prime Version	Description	Impact
20.3	Added support for interworking function (IWF) type 0.	You can connect eCPRI node with one CPRI node.
	Supports pairing of eCPRI Intel FPGA IP with O-RAN Intel FPGA IP.	—
	Added following new IWF related parameters: • **Interworking Function (IWF) Support** • **Interworking Function (IWF) Type** • **Interworking Function (IWF) Number of CPRI**	Using these parameters, you can enable your eCPRI IP for IWF functionality.
	Added following IWF related interfaces: • IWF Type 0 eCPRI Source Interface • IWF Type 0 eCPRI Sink Interface • IWF Type 0 CPRI MAC Interface *Note:* Refer to *eCPRI Intel FPGA IP User Guide* for detailed information on signals related to these interfaces.	—
	Added following clock signals: • `iwf_gmii_rxclk[N]` • `iwf_gmii_txclk[N]` • `gmii_rxclk[N]` • `gmii_txclk[N]`	—
	Added following reset signals: • `iwf_rst_tx_n` • `iwf_rst_rx_n` • `rst_tx_n_sync` • `rst_rx_n_sync` • `iwf_gmii_rxreset_n[N]` • `iwf_gmii_txreset_n[N]` • `gmii_rxreset_n[N]` • `gmii_txreset_n[N]`	—
	The eCPRI IP design example for Intel Arria 10 device is now available.	—