



# DisplayPort Intel FPGA IP Release Notes



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## 1. DisplayPort Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

### Related Information

- [Intel Quartus Prime Design Suite Update Release Notes](#)
- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort Intel FPGA IP User Guide](#)
- [DisplayPort Intel Arria 10 FPGA IP Design Example User Guide](#)
- [DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide](#)
- [DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide](#)
- [Errata for DisplayPort Intel FPGA IP in the Knowledge Base](#)

### 1.1. DisplayPort Intel FPGA IP v19.3.0

**Table 1. v19.3.0 2020.06.22**

Intel Quartus Prime Version	Description	Impact
20.2	Added support for High-bandwidth Digital Content Protection (HDCP) feature for Intel Stratix® 10 devices. This feature has also been available for Intel Arria® 10 devices since the Intel Quartus Prime Pro Edition software version 19.4 and later.	The HDCP feature is not included in the Intel Quartus Prime Pro Edition software. To access the HDCP feature, contact Intel at <a href="https://www.intel.com/content/www/us/en/broadcast/products/programmable/applications/connectivity-solutions.html">https://www.intel.com/content/www/us/en/broadcast/products/programmable/applications/connectivity-solutions.html</a> .

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\*Other names and brands may be claimed as the property of others.



Table 2. v19.3.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
20.1	Enabled speed grade 3 (conditional support) for Intel Arria 10 and Intel Stratix 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
	Enabled multi-stream transport support up to 4 streams for Intel Cyclone® 10 GX devices.	

## 1.2. DisplayPort Intel FPGA IP v19.1

Table 3. v19.1 April 2019

Description	Impact
Enabled final support for Intel Stratix 10 L-tile and H-tile devices. The design examples now target Intel Stratix 10 production devices.	If you want to target your designs to use Intel Stratix 10 L-tile devices, you must upgrade your IP core.

## 1.3. DisplayPort Intel FPGA IP v18.1 Update 1

### 18.1.1 December 2018

- For Intel Stratix 10 devices, enabled Pixel Clock Recovery function.
- Changed Synopsys Design Constraints to entity-based Synopsys Design Constraints.
- Cleaned up compilation warnings found in Intel Stratix 10 design example with pixel clock recovery.
- Enabled Intel Stratix 10 design example with Pixel Clock Recovery variant.
- Enabled initiation of Tx in software regardless of the setting of DP\_SUPPORT\_EDID\_PASSTHRU.
- Fixed an Intel Arria 10 design example when no display output occurred in non GPU mode.
- Enabled extended receiver capabilities when the maximum link rate is HBR3.
- For Intel Stratix 10 H-tile devices, added VID\_OPERATION\_MODE "PMBUS MASTER" and PWRMGMT settings to the video connectivity design example IP .qsf file to enable Intel Stratix 10 SmartVID and power management capabilities.

### Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort Intel FPGA IP User Guide](#)
- [DisplayPort Intel Arria 10 FPGA Design Example User Guide](#)
- [DisplayPort Intel Cyclone 10 GX FPGA Design Example User Guide](#)
- [DisplayPort Intel Stratix 10 FPGA Design Example User Guide](#)
- [Errata for DisplayPort Intel FPGA IP in the Knowledge Base](#)



## 1.4. DisplayPort Intel FPGA IP v18.1

**Table 4. 18.1 September 2018**

Description	Impact
Added a new design example for Intel Stratix 10 devices in version 18.1 release. Refer to the <i>DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide</i> for more information.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated the design examples for Intel Arria 10 devices to support multi-stream transport (MST).	

### Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort Intel FPGA IP User Guide](#)
- [DisplayPort Intel Arria 10 FPGA Design Example User Guide](#)
- [DisplayPort Intel Cyclone 10 GX FPGA Design Example User Guide](#)
- [DisplayPort Intel Stratix 10 FPGA Design Example User Guide](#)
- [Errata for DisplayPort Intel FPGA IP in the Knowledge Base](#)

## 1.5. DisplayPort Intel FPGA IP v18.0

**Table 5. v18.0 May 2018**

Description	Impact
Renamed Intel FPGA DisplayPort IP to DisplayPort Intel FPGA IP as part of standardizing and rebranding exercise.	-
Added support for Xcelium* Parallel simulator.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added the following files: <ul style="list-style-type: none"> <li>• xcelium_files.tcl</li> <li>• xcelium_setup.sh</li> <li>• xcelium_sim.sh</li> </ul>	
Added final support for Intel Cyclone 10 GX devices.	The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.
Added new design examples for Intel Cyclone 10 GX devices in version 17.1.1 release. Refer to the <i>DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide</i> for more information.	

**Table 6. Design Files Required for IP Upgrade**

The implementation of the IP on hardware requires additional components specific to the device targeted.

These additional components, such as Native PHY, TX PLL, reconfiguration controller, are not included as part of the Intel Quartus Prime IP Upgrade flow. Upgrading an IP core would require the inclusion of these files generated as part of the IP design example.

Design Example	Required Files
Intel Arria 10	<ul style="list-style-type: none"> <li>• quartus\al0_dp_demo.qsf</li> <li>• rtl\rx_phy\rx_phy_top.v</li> <li>• rtl\tx\tx_phy_top.v</li> <li>• rtl\al0_dp_demo.v</li> <li>• rtl\bitec_reconfig_alt_al0.v</li> </ul>
<i>continued...</i>	



Design Example	Required Files
	<ul style="list-style-type: none"> <li>rtl\al0_reconfig_arbiter.sv</li> <li>software\main.c</li> <li>software\rx_utils.c</li> <li>software\tx_utils.c</li> <li>software\tx_utils.h</li> <li>software\config.h</li> </ul> <p>Execute script\build_sw.sh before project compilation to update Software API and regenerate the software .elf file.</p>
Intel Cyclone 10 GX	<ul style="list-style-type: none"> <li>quartus\c10_dp_demo.qsf</li> <li>rtl\rx_phy\rx_phy_top.v</li> <li>rtl\tx\tx_phy_top.v</li> <li>rtl\c10_dp_demo.v</li> <li>rtl\bitec_reconfig_alt_c10.v</li> <li>rtl\c10_reconfig_arbiter.sv</li> <li>software\main.c</li> <li>software\rx_utils.c</li> <li>software\tx_utils.c</li> <li>software\tx_utils.h</li> <li>software\config.h</li> </ul> <p>Execute script\build_sw.sh before project compilation to update Software API and regenerate the software .elf file.</p>

**Related Information**

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort Intel FPGA IP User Guide](#)
- [DisplayPort Intel Arria 10 FPGA Design Example User Guide](#)
- [DisplayPort Intel Cyclone 10 GX FPGA Design Example User Guide](#)
- [Errata for DisplayPort Intel FPGA IP in the Knowledge Base](#)

## 1.6. Intel FPGA DisplayPort IP Core v17.1

**Table 7. v17.1 November 2017**

Description	Impact
Renamed the following as per Intel rebranding: <ul style="list-style-type: none"> <li>• DisplayPort IP core to Intel FPGA DisplayPort IP core</li> <li>• Qsys to Platform Designer</li> </ul>	-
Added advance support for Intel Cyclone 10 GX devices.	The Intel Cyclone 10 GX devices are only available in the Intel Quartus Prime Pro Edition software.
YCbCr 4:2:0 color format is now supported.	These features are only available in the Intel Quartus Prime Pro Edition software.
The Intel FPGA DisplayPort IP core version 17.1 conforms to <i>Video Electronics Standards Association (VESA) DisplayPort Standard version 1.4</i> .	
Added data link rate support for HBR3 (8.10 Gbps). This rate is only available in quad symbols per clock for Intel Arria 10 and Intel Cyclone 10 GX devices.	
<b>continued...</b>	



Description	Impact
<p>Note: The clock recovery module in the Intel Arria 10 design examples only support up to 4Kp60 resolution.</p>	
<p>Updated the design examples to <b>DisplayPort SST Parallel Loopback With PCR</b> and <b>DisplayPort SST Parallel Loopback Without PCR</b>.</p>	
<p>In previous versions of the DisplayPort Intel FPGA IP design example for Intel Arria 10 devices, the IOPLL and transceiver PLL output may experience additional jitter. The additional jitter occurs if you source the reference clock from a cascaded PLL output, global clock, or core clock. To compensate for the jitter, the designs require additional constraints. This issue has been fixed in the Intel Quartus Prime software version 17.1.</p>	<p>If you are upgrading designs that have these additional constraints from the previous versions of Intel Quartus Prime to version 17.1, you must revise the constraints. Refer to the <a href="#">KDB page</a> for more information.</p>

**Related Information**

- [Introduction to Intel FPGA IP Cores](#)
- [Intel FPGA DisplayPort IP Core User Guide](#)
- [Intel FPGA DisplayPort IP Core Design Example User Guide for Intel Arria 10 Devices](#)
- [Errata for Intel FPGA DisplayPort IP Core in the Knowledge Base](#)

## 1.7. DisplayPort IP Core v17.0

**Table 8. v17.0 May 2017**

Description	Impact
<p>Available in both Quartus Prime Pro Edition and Quartus Prime Standard Edition.</p>	
<p>Added support for the following features:</p> <ul style="list-style-type: none"> <li>• Adaptive sync (preliminary)</li> <li>• YCbCr 4:2:0 color format (preliminary)</li> <li>• Proprietary video image format for DisplayPort source</li> </ul>	<p>These changes are optional. If you do not upgrade your IP core, it does not have these new features.</p>
<p>Added a new parameter: <b>TX Video IM Enable</b>. Turn on to enable the video image interface. Turn off to use the traditional HSYNC/ VSYNC/DE video input interface.</p>	
<p>Multi-stream transport (MST) feature supports audio data channel.</p>	

**Related Information**

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [DisplayPort IP Core Design Example User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)



## 1.8. DisplayPort IP Core v16.1

Table 9. v16.1 October 2016

Description	Impact
The 16.1 version of the DisplayPort IP core is available only in Quartus Prime Standard Edition.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Multi-stream transport (MST) feature does not support audio data channel.	
Added support for multiple TX instances in software API.	
Added new <b>Design Example</b> tab in the DisplayPort IP core parameter editor. The design example is for Arria 10 devices. Refer to the <i>DisplayPort IP Core Design Example User Guide</i> for more information.	

### Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [DisplayPort IP Core Design Example User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

## 1.9. DisplayPort IP Core v16.0

Table 10. v16.0 May 2016

Description	Impact
Removed the <b>Import fixed MSA</b> parameter and the <code>txN_msa_conduit</code> signal. The DisplayPort source core now automatically inserts the TX main stream attribute (MSA).	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for black video feature for DisplayPort sink core.	
Added support for Link Quality Analysis (LQA).	

### Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

## 1.10. DisplayPort IP Core v15.1

Table 11. v15.1 November 2015

Description	Impact
The <code>txN_vid_f</code> pin is removed from the DisplayPort IP core. The IP core handles the interface internally.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated multi-stream support: <ul style="list-style-type: none"><li>• 1, 2, 3, or 4 streams for Arria 10 and Stratix V devices</li><li>• 1 or 2 streams for Arria V devices</li></ul>	

### Related Information

- [Introduction to Intel FPGA IP Cores](#)





- [DisplayPort IP Core User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

## 1.11. DisplayPort IP Core v15.0

**Table 12. v15.0 May 2015**

Description	Impact
Added preliminary support for Arria 10 devices.	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Updated color support. <ul style="list-style-type: none"> <li>• RGB—18, 24, 30, 36, or 48 bpp</li> <li>• YCbCr 4:4:4—24, 30, 36, or 48 bpp</li> <li>• YCbCr 4:2:2—16, 20, 24, or 32 bpp</li> </ul>	
Added source-supported DPCD locations.	
Added new bits for DPTX_TEST_80BIT_PATTERN bits.	
Removed the Link Quality Generation register bits and combined these bits into the DPTX_TX_CONTROL register. <ul style="list-style-type: none"> <li>• 0000 = Normal video</li> <li>• 0001 = Training pattern 1</li> <li>• 0010 = Training pattern 2</li> <li>• 0011 = Training pattern 3</li> <li>• 0111 = Video idle pattern</li> <li>• 1001 = D10.2 test pattern (same as training pattern 1)</li> <li>• 1010 = Symbol error rate measurement pattern</li> <li>• 1011 = PRBS7</li> <li>• 1100 = 80-bit custom pattern</li> <li>• 1101 = HBR2 compliance test pattern (CP2520 pattern 1)</li> </ul>	
Added new sink-supported DPCD location bits: TEST_REQUEST, TEST_LINK_RATE, TEST_LANE_COUNT, PHY_TEST_PATTERN, and TEST_80BIT_CUSTOM_PATTERN.	
Added simulation testbench for Arria 10 devices.	

### Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

## 1.12. DisplayPort IP Core v14.1

**Table 13. v14.1 December 2014**

Description	Impact
Added multi-stream support (MST, 1 to 4 source and sink streams). You can access this feature using these parameters: <ul style="list-style-type: none"> <li>• <b>Support MST</b></li> <li>• <b>Max stream count</b></li> </ul>	These changes are optional. If you do not upgrade your IP core, it does not have these new features.
Added support for 4Kp60 resolution.	
Removed support for double reference clocks—162 MHz and 270 MHz—for transceiver clocking.	

*continued...*



Description	Impact
Updated the design example with pixel clock recovery feature and 4Kp60 support.	
Added new signals.	
Added new source registers: <ul style="list-style-type: none"> <li>• 0x00a0 (DPTX_MST_CONTROL1)</li> <li>• 0x00a2 (DPTX_MST_VCPTAB0)</li> <li>• 0x00a3 (DPTX_MST_VCPTAB</li> <li>• 0x00a3 (DPTX_MST_VCPTAB1)</li> <li>• 0x00a4 (DPTX_MST_VCPTAB2)</li> <li>• 0x00a5 (DPTX_MST_VCPTAB3)</li> <li>• 0x00a6 (DPTX_MST_VCPTAB4)</li> <li>• 0x00a7 (DPTX_MST_VCPTAB5)</li> <li>• 0x00a8 (DPTX_MST_VCPTAB6)</li> <li>• 0x00a9 (DPTX_MST_VCPTAB7)</li> <li>• 0x00aa (DPTX_MST_TAVG_TS)</li> </ul>	
Added new sink registers: <ul style="list-style-type: none"> <li>• 0x0006 (DPRX_BER_CNTI0)</li> <li>• 0x0007 (DPRX_BER_CNTI1)</li> <li>• 0x00a0 (DPRX_MST_CONTROL1)</li> <li>• 0x00a1 (DPRX_MST_STATUS1)</li> <li>• 0x00a2 (DPRX_MST_VCPTAB0)</li> <li>• 0x00a3 (DPRX_MST_VCPTAB1)</li> <li>• 0x00a4 (DPRX_MST_VCPTAB2)</li> <li>• 0x00a5 (DPRX_MST_VCPTAB3)</li> <li>• 0x00a6 (DPRX_MST_VCPTAB4)</li> <li>• 0x00a7 (DPRX_MST_VCPTAB5)</li> <li>• 0x00a8 (DPRX_MST_VCPTAB6)</li> <li>• 0x00a9 (DPRX_MST_VCPTAB7)</li> </ul>	
Changed the value of the following register bits: <ul style="list-style-type: none"> <li>• Source register               <ul style="list-style-type: none"> <li>– 0x0000 - Bits RX_LINK_RATE</li> <li>– 0x0001 - Bits RX_LINK_RATE</li> <li>– 0x0002 - Bits RSTI3, RSTI2, RSTI1, RSTI0</li> </ul> </li> <li>• Sink register               <ul style="list-style-type: none"> <li>– 0x0000 - Bits TX_LINK_RATE and ENHANCED_FRAME</li> </ul> </li> </ul>	

**Table 14. DisplayPort IP Core Signal Changes**

Signals added or modified in version 14.1.

Old Signal Name	New Signal Name	Notes
—	clk_cal	Calibration clock for transceiver management interface
—	tx_link_rate_8bits	Main link rate expressed in multiples of 270Mbps
—	rx_link_rate_8bits	
—	txN_video_in (N=1,2,3)	TX signals for Stream 1, 2 and 3
—	txN_vid_clk (N=1,2,3)	
—	txN_audio (N=1,2,3)	
—	txN_audio_clk (N=1,2,3)	
—	txN_ss (N=1,2,3)	

*continued...*



Old Signal Name	New Signal Name	Notes
—	txN_msa_conduit (N=1,2,3)	
—	rxN_video_out (N=1,2,3)	RX signals for Stream 1, 2 and 3
—	rxN_vid_clk (N=1,2,3)	
—	rxN_audio (N=1,2,3)	
—	rxN_ss (N=1,2,3)	
—	rxN_msa_conduit (N=1,2,3)	
—	rxN_stream (N=1,2,3)	
tx_xcvr_clkout	tx_ss_clk	—
rx_xcvr_clkout	rx_ss_clk	—

#### Related Information

- [Introduction to Intel FPGA IP Cores](#)
- [DisplayPort IP Core User Guide](#)
- [Errata for DisplayPort IP Core in the Knowledge Base](#)

### 1.13. DisplayPort Intel FPGA IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.1	19.3.0	<a href="#">DisplayPort Intel FPGA IP User Guide</a>
19.4	19.2.0	<a href="#">DisplayPort Intel FPGA IP User Guide</a>
19.1	19.1	<a href="#">DisplayPort Intel FPGA IP User Guide</a>
18.1	18.1	<a href="#">DisplayPort Intel FPGA IP User Guide</a>
18.0	18.0	<a href="#">DisplayPort Intel FPGA IP User Guide</a>
17.1	17.1	<a href="#">Intel FPGA DisplayPort IP Core User Guide</a>
17.0	17.0	<a href="#">DisplayPort IP Core User Guide</a>
16.1	16.1	<a href="#">DisplayPort IP Core User Guide</a>
16.0	16.0	<a href="#">DisplayPort IP Core User Guide</a>
15.1	15.1	<a href="#">DisplayPort IP Core User Guide</a>
15.0	15.0	<a href="#">DisplayPort IP Core User Guide</a>
14.1	14.1	<a href="#">DisplayPort IP Core User Guide</a>

### 1.14. DisplayPort Intel Arria 10 FPGA IP Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to 19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.



If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
19.2	19.1.0	<a href="#">DisplayPort Intel Arria 10 FPGA IP Design Example User Guide</a>
19.1	19.1	<a href="#">DisplayPort Intel Arria 10 FPGA IP Design Example User Guide</a>
17.1	17.1	<a href="#">Intel FPGA DisplayPort IP Core Design Example for Arria 10 Devices User Guide</a>
17.0	17.0	<a href="#">Intel Arria 10 DisplayPort IP Core Design Example User Guide</a>
16.1	16.1	<a href="#">DisplayPort IP Core Design Example User Guide</a>

## 1.15. DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to 19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
19.2	19.1.0	<a href="#">DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide</a>
19.1	19.1	<a href="#">DisplayPort Intel Cyclone 10 GX FPGA IP Design Example User Guide</a>
17.1.1	17.1.1	<a href="#">Intel FPGA DisplayPort IP Core Design Example User Guide for Intel Cyclone 10 GX Devices</a>

## 1.16. DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to 19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
20.1	19.3.0	<a href="#">DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide</a>
19.2	19.1.0	<a href="#">DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide</a>
19.1	19.1	<a href="#">DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide</a>
18.1	18.1	<a href="#">DisplayPort Intel Stratix 10 FPGA IP Design Example User Guide</a>