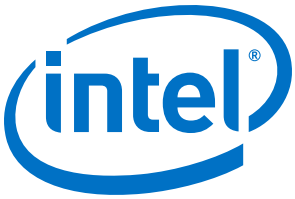

PHY Lite for Parallel Interfaces Intel FPGA IP Core Release Notes

RN-1204 | 2020.12.14
Latest document on the web: PDF | HTML

Contents

PHY Lite for Parallel Interfaces Intel FPGA IP Core Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- PHY Lite for Parallel Interfaces Intel FPGA IP Core User Guide
- Intel FPGA Knowledge Base Page
  More information on errata and known issues for the PHY Lite for Parallel Interfaces Intel FPGA IP core.

PHY Lite for Parallel Interfaces Intel Agilex FPGA IP v20.3.0

Table 1. v20.3.0 2020.12.14

Intel Quartus Prime Version	Description	Impact
20.4	• Added support for dynamic reconfiguration. • Added design example with dynamic reconfiguration. • Added **Pin Placement** tab in the parameter editor, to allow pin placement settings for all groups and graphical support of data/strobe pin placement within sub-bank. Removed pin placement settings in each group. • Added support for half-rate and full-rate. • Added support for I/O sub-bank pin 7 in each lane to be used as data pin. • Added sub-bank ID to facilitate pin placement at the IP generation stage.	—

PHY Lite for Parallel Interfaces Intel Agilex FPGA IP v20.3.0

Table 2. v20.3.0 2020.10.05

Intel Quartus Prime Version	Description	Impact
20.3	Initial release.	—

PHY Lite for Parallel Interfaces Intel FPGA IP Core v19.3.0

Table 3. v19.3.0 2020.06.22

Intel Quartus Prime Version	Description	Impact
20.2	• Added support for Intel Stratix® 10 GX 10M device variant.	—

PHY Lite for Parallel Interfaces Intel FPGA IP Core v18.1

Table 4. v18.1 September 2018

Description	Impact
Added **Fast simulation model** parameter to the IP core to reduce IP simulation time. *Note:* This option is preliminarily supported in the Intel Quartus Prime software v18.1.	—

Related Information

- Introduction to Intel FPGA IP Cores
- PHY Lite for Parallel Interfaces Intel FPGA IP Core User Guide
- Errata for other IP cores in the Knowledge Base

PHY Lite for Parallel Interfaces Intel FPGA IP Core v18.0

Table 5. v18.0 May 2018

Description	Impact
Added **First PHYLite Instance in the Avalon Chain** parameter to the IP core to determine the first PHY Lite for Parallel Interfaces Intel Stratix 10 FPGA IP core that is connected to the Avalon-MM master.	—
Renamed Intel FPGA PHYLite for Parallel Interfaces IP core to the following IP core names as per Intel rebranding: • Intel Stratix 10 devices: PHY Lite for Parallel Interfaces Intel Stratix 10 IP core • Intel Arria® 10 devices: PHY Lite for Parallel Interfaces Intel Arria 10 FPGA IP core • Intel Cyclone® 10 GX devices: PHY Lite for Parallel Interfaces Intel Cyclone 10 FPGA IP core	—

Related Information

- Introduction to Intel FPGA IP Cores
- PHYLite for Parallel Interfaces Intel FPGA IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA PHYLite for Parallel Interfaces IP Core v17.1

Table 6. v17.1 November 2017

Description	Impact
Added support for Intel Stratix 10 and Intel Cyclone 10 GX devices.	—
Added support dynamic reconfiguration and non dynamic reconfiguration design example for Intel Stratix 10 and Intel Cyclone 10 GX devices.	—
Renamed Altera PHYLite for Parallel Interfaces IP core to Intel FPGA PHYLite for Parallel Interfaces IP core as per Intel rebranding.	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Altera PHYLite for Parallel Interfaces IP Core v16.0

Table 7. v16.0 May 2016

Description	Impact
Added parameter, **VCO clock frequency**, to inform users on the internally calculated VCO clock.	—
Changed of IP maximum supported frequency per device speed grade.	—
Added `issp.tcl` file in Dynamic Reconfiguration with Debug Kit Design Example to enable users to reset the system and probe internal signals.	—

Related Information

- Introduction to Altera IP Cores
- Altera PHYLite for Parallel Interfaces IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Altera PHYLite for Parallel Interfaces IP Core v15.1

Table 8. v15.1 November 2015

Description	Impact
Added new debug kit example design using Nios II for dynamic reconfigurations.	-
Added parameter, **Copy parameters from another group**, to allow copying parameters from one DQ group to another DQ group.	-
Added new parameters group, **Group <x> Dynamic Reconfiguration Timing Settings**, for users to select dynamic reconfiguration algorithm for timing analysis.	-
Added parameter, **OCT enable size**, for users to specify the interpolator clock cycle delay required to ensure OCT is turned on before sampling any input data.	-
Added parameters, **Inter Symbol Interference of the Read Channel** and **Inter Symbol Interference of the Write Channel**, for users to specify the Inter Symbol Interference values for read and write channels for timing analysis.	-

Related Information

- Introduction to Altera IP Cores
- Altera PHYLite for Parallel Interfaces IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Altera PHYLite for Memory IP Core v14.1

Table 9. v14.1 December 2014

Description	Impact
Added internal PLL additional clock export parameter	-
Added setup delay constraint timing parameters in the **Group** tabs in the parameter editor	-

Related Information

- Altera PHYLite for Memory Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

Altera PHYLite for Memory IP Core v14.0 Arria 10 Edition

Table 10. v14.0 Arria 10 Edition August 2014

Description	Impact
Added dynamic reconfiguration	-
Added I/O standard and OCT settings	-
Added complementary strobe type	-
Changed `pll_locked` port name to `interface_locked`	-

Related Information

- Altera PHYLite for Memory Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

PHY Lite for Parallel Interfaces IP Core User Guide Document Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	User Guide
20.3	Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
20.2	Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
19.1	Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
18.1	Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
18.0	Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide

continued...

Intel Quartus Prime Version	User Guide
17.1	Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
17.0	Altera PHYLite for Parallel Interfaces IP Core User Guide
16.0	Altera PHYLite for Parallel Interfaces IP Core User Guide
15.1	Altera PHYLite for Parallel Interfaces IP Core User Guide
14.1	Altera PHYLite for Parallel Interfaces IP Core User Guide