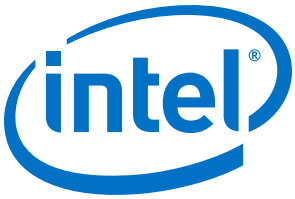

LVDS SERDES Intel® FPGA IP Release Notes

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If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Introduction to Intel FPGA IP Cores
- Intel Agilex General Purpose I/O and LVDS SERDES User Guide
- Intel Stratix® 10 High-Speed LVDS I/O User Guide
- LVDS SERDES Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base

LVDS SERDES Intel FPGA IP v19.5.0

Table 1. v19.5.0 2020.09.28

Intel Quartus Prime Version	Description	Impact
20.3	• Improved the power usage of the IP in Intel Agilex™ devices.	—

LVDS SERDES Intel FPGA IP v19.4.0

Table 2. v19.4.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
20.1	Add additional delay to the `pll_locked` signal assertion to ensure the IP is properly locked to the PLL before IP initialization in Intel Agilex devices.	—

LVDS SERDES Intel FPGA IP v19.3.0

Table 3. v19.3.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	Added support for Intel Agilex devices.	—

LVDS SERDES Intel FPGA IP v18.1

Table 4. v18.1 September 2018

Description	Impact
For Intel Stratix® 10 devices, the IP now supports using reference clock from other I/O banks but not from other IPs such as the IOPLL IP or the hard processor system (HPS). If you use reference clock from other I/O bank, you must manually promote the reference clock input using the following `.qsf` command: `GLOBAL_SIGNAL GLOBAL_CLOCK -to <name of top-level reference clock input port>`	You are no longer limited to using only the dedicated reference clock in the IP's I/O bank.

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 High-Speed LVDS I/O User Guide
- LVDS SERDES Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base

LVDS SERDES Intel FPGA IP v18.0

Table 5. v18.0 May 2018

Description	Impact
Renamed the IP core from "Intel FPGA LVDS SERDES" to "LVDS SERDES Intel FPGA IP".	-

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 High-Speed LVDS I/O User Guide
- LVDS SERDES Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA LVDS SERDES IP Core v17.1

Table 6. v17.1 November 2017

Description	Impact
Added support for Intel Stratix 10 devices: • Duplex feature to allow transmitter and receiver channels in the same I/O bank • Clock phase alignment (CPA) block for improved timing closure between the periphery and the core	—
Renamed Altera LVDS SERDES IP core to Intel FPGA LVDS SERDES IP core as per Intel rebranding.	—

Related Information

- Introduction to Altera IP Cores
- Intel Stratix 10 High-Speed LVDS I/O User Guide
- Intel FPGA LVDS SERDES IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Altera LVDS SERDES IP Core v17.0

Table 7. v17.0 May 2017

Description	Impact
Added support for Intel Cyclone® 10 GX devices.	-

Related Information

- Introduction to Altera IP Cores
- Altera LVDS SERDES IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Altera LVDS SERDES IP Core v14.1

Table 8. v14.1 December 2014

Description	Impact
Added internal PLL additional clock export parameter	-

Related Information

- Altera LVDS SERDES Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

Altera LVDS SERDES IP Core v14.0 Arria 10 Edition

Table 9. v14.0 Arria 10 Edition August 2014

Description	Impact
Added feature that creates `.sdc` file for generated designs (previously only for example designs)	-
Added support for external PLL mode	-
Added option to clock TX core registers using reference clock	-

Related Information

- Altera LVDS SERDES Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

Intel Agilex General-urpose I/O and LVDS SERDES User Guide Archives

If an IP version is not listed, the user guide for the previous IP version applies.

Intel Quartus Prime Version	User Guide
20.2	Intel Agilex General Purpose I/O and LVDS SERDES User Guide
20.1	Intel Agilex General Purpose I/O and LVDS SERDES User Guide
19.4	Intel Agilex General Purpose I/O and LVDS SERDES User Guide
19.3	Intel Agilex General Purpose I/O and LVDS SERDES User Guide

Intel Stratix 10 High-Speed LVDS I/O User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
19.4	Intel Stratix 10 High-Speed LVDS I/O User Guide
19.2	Intel Stratix 10 High-Speed LVDS I/O User Guide
19.1	Intel Stratix 10 High-Speed LVDS I/O User Guide
18.1	Intel Stratix 10 High-Speed LVDS I/O User Guide
18.0	Intel Stratix 10 High-Speed LVDS I/O User Guide
17.1	Intel Stratix 10 High-Speed LVDS I/O User Guide

LVDS SERDES Intel FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
19.3.0	LVDS SERDES Intel FPGA IP User Guide: Intel Arria® 10 and Intel Cyclone 10 GX Devices
19.1	LVDS SERDES Intel FPGA IP User Guide: Intel Arria 10 and Intel Cyclone 10 GX Devices

continued...

IP Core Version	User Guide
18.1	LVDS SERDES Intel FPGA IP User Guide: Intel Arria 10 and Intel Cyclone 10 GX Devices
18.0	LVDS SERDES Intel FPGA IP User Guide: Intel Arria 10 and Intel Cyclone 10 GX Devices
17.1	Intel FPGA LVDS SERDES IP Core User Guide
17.0	Altera LVDS SERDES IP Core User Guide
16.0	Altera LVDS SERDES IP Core User Guide
15.1	Altera LVDS SERDES IP Core User Guide
14.1	Altera LVDS SERDES IP Core User Guide
13.1	Altera LVDS SERDES Megafunction User Guide