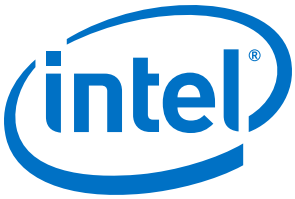

GPIO Intel® FPGA IP Release Notes

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GPIO Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Agilex™ General Purpose I/O and LVDS SERDES User Guide
- Intel Stratix® 10 General Purpose I/O User Guide
- GPIO Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base
- Intel Quartus Prime Design Suite Update Release Notes

GPIO Intel FPGA IP v19.3.0

Table 1. v19.3.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Added support for Intel Agilex™ devices.	—

GPIO Intel FPGA IP v18.0

Table 2. v18.0 May 2018

Description	Impact
Renamed the IP core from "Intel FPGA GPIO" to "GPIO Intel FPGA IP".	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix® 10 General Purpose I/O User Guide
- GPIO Intel FPGA IP User Guide
- Errata for other IP cores in the Knowledge Base

Intel FPGA GPIO IP Core v17.1

Table 3. v17.1 November 2017

Description	Impact
Added support for Intel Stratix® 10 devices.	—
Renamed Altera GPIO IP core to Intel FPGA GPIO IP core as per Intel rebranding.	—

Related Information

- Introduction to Altera IP Cores
- Intel Stratix 10 General Purpose I/O User Guide
- Intel FPGA GPIO IP Core User Guide
- Errata for other IP cores in the Knowledge Base

Altera GPIO IP Core v14.0 Arria 10 Edition

Table 4. v14.0 Arria 10 Edition August 2014

Description	Impact
Changed signal names	-

Table 5. Signal Name Changes

Old Name	New Name	Notes
core_ck_fr_in_export	ck_fr_in	
core_ck_fr_out_export	ch_fr_out	
core_ck_hr_in_export	ch_hr_in	
core_ck_hr_out_export	ch_hr_out	
core_dout_export	dout	
core_din_export	din	
core_oe_export	oe	
core_pad_io_export	pad_io	
core_pad_io_b_export	pad_io_b	
core_aclr_export	aclr	
core_sclr_export	sclr	
core_cke_export	cke	

continued...

Old Name	New Name	Notes
core_ck_export	ck	
core_ck_in_export	ck_in	
core_ck_out_export	ck_out	
core_ck_fr_export	ck_fr	
core_ck_hr_export	ck_hr	
core_pad_in_export	pad_in	
core_pad_in_b_export	pad_in_b	
core_pad_out_export	pad_out	
core_pad_out_b_export	pad_out_b	
core_aset_export	aset	
core_sset_export	sset	

Related Information

- Altera GPIO Megafunction User Guide
- Errata for other IP cores in the Knowledge Base

General Purpose I/O User Guide Archives

If the table does not list a software version, the user guide for the previous software version applies.

Intel Quartus Prime Version	User Guide
19.2	Intel Stratix 10 General Purpose I/O User Guide
18.1	Intel Stratix 10 General Purpose I/O User Guide
18.0	Intel Stratix 10 General Purpose I/O User Guide
17.1	Intel Stratix 10 General Purpose I/O User Guide

GPIO Intel FPGA IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.0	GPIO Intel FPGA IP User Guide: Intel Arria® 10 and Intel Cyclone® 10 GX Devices
17.1	Intel FPGA GPIO IP Core User Guide
17.0	Altera GPIO IP Core User Guide
16.1	Altera GPIO IP Core User Guide
16.0	Altera GPIO IP Core User Guide
14.1	Altera GPIO Megafunction User Guide
13.1	Altera GPIO Megafunction User Guide