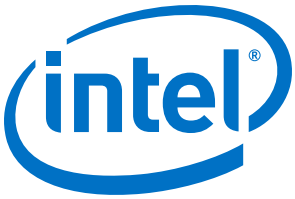

Intel® Arria® 10 and Intel® Cyclone® 10 GX Hard IP for PCI Express* IP Core Release Notes

Updated for Intel® Quartus® Prime Design Suite: **18.0**

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1. Intel® Arria® 10 and Intel® Cyclone® 10 GX Hard IP for PCI Express* IP Core Release Notes

1.1. Intel® Arria® 10 and Intel® Cyclone® 10 GX Hard IP for PCI Express* IP Core v18.0

Table 1. 18.0 May 2018

Description	Impact
Support for Root Port mode is preliminary in the 18.0 release.	You can enable the Root Port mode using the parameter editor. The Root Port supports basic simulation and compilation. However, the Root Port is not fully verified. You may find functional problems in the current release.
msi_control[15:0] are not wired correctly in the generated IP.	If you enable MSI/MSI-X functionality in the design, you need to connect this port to the top-level instantiation.
VHDL NCSim* simulation support.	For Intel® Quartus® Prime Standard Edition, NCSim* VHDL simulation is not supported in the 18.0 release.

1.2. Intel Arria® 10 and Intel Cyclone® 10 GX Hard IP for PCI Express* IP Core v17.1

Table 2. 17.1 November 2017

Description	Impact
Added support for Intel Cyclone® 10 GX devices. Intel Cyclone 10 GX devices support a single Gen1 and Gen2 IP core at up to the Gen2 x4 data rate.	You can use the lower cost Intel Cyclone 10 GX device to implement PCIe* for up to Gen2 x4 variants.
Added **Enable RX-polarity inversion soft logic** parameter to the **PHY Characteristics** tab of the component parameter editor.	This parameter mitigates a RX-polarity the following inversion problem. When the Intel Cyclone 10 GX or Intel Arria® 10 Hard IP core receives TS2 training sequences during the Polling.Config state, when you have not enabled the automatic polarity inversion parameter, automatic lane polarity inversion is not guaranteed. The link may train to a smaller than expected link width or may not train successfully. This problem can affect configurations with any PCIe speed and width. When you

continued...

Description	Impact
	include this parameter, polarity inversion is available for all configurations except Gen1 x1. This fix does not support CvP or autonomous mode Refer to the links below for additional information.
The Root Port is preliminary in the 17.1 release.	You can enable the Root Port using the parameter editor. The Root Port supports basic simulation and compilation. However, the Root Port is not fully verified. You may find functional problems in the current release.

Related Information

- Arria 10 or Cyclone 10 Avalon-ST Interface for PCIe Solutions User Guide
  For the Avalon-ST Interface to the Application Layer
- Arria 10 or Cyclone 10 Avalon-MM DMA Interface for PCIe Solutions User Guide
  For the Avalon-MM interface and DMA functionality
- Arria 10 or Cyclone 10 Avalon-MM Interface for PCIe Solutions User Guide
  For the Avalon-MM interface with no DMA
- Arria 10 Avalon-ST Interface with SR-IOV PCIe Solutions User Guide
  For the Avalon-ST interface with Single Root I/O Virtualization (SR-IOV)
- Errata for the Arria 10 Hard IP for PCI Express IP Core in the Knowledge Base
- Errata for the Cyclone 10 Hard IP for PCI Express IP Core in the Knowledge Base
- Why does my Arria 10 PCIe Hard IP link width downtrain?
- Why does my Cyclone 10 GX PCIe Hard IP link width downtrain?

1.3. Intel Arria 10 Hard IP for PCI Express* IP Core v17.0

Table 3. 17.0 May 2017

Description	Impact
Added **Enable soft DFE controller IP** parameter to the **PHY** tab of the component parameter editor.	When On, the PCIe Hard IP core includes a decision feedback equalization (DFE) soft controller in the FPGA fabric to improve the bit error rate (BER) margin. The default for this option is Off because DFE is typically not required. However, short reflective links may benefit from this soft DFE controller IP

1.4. Intel Arria 10 Hard IP for PCI Express* IP Core v16.1

Table 4. 16.1 October 2016

Description	Impact
Added parameter to select preset for Phase2 and Phase3 far-end TX equalization.	Better control of signal quality.
For the Avalon-MM with DMA interface, increased the maximum DMA transfer size to 1 megabyte (MB) for both the 128- and 256-bit interfaces.	Reduces the number of descriptors required to transfer data.
For the Single-Root I/O Virtualization (SR-IOV) interface, changed support for the 128-bit interface from preliminary to final.	You can use the 128-bit interface in production designs.
For the SR-IOV interface, added licensing requirement.	You must purchase a license to use this variant in hardware.
For the SR-IOV interface, added Intel FPGA IP Evaluation Mode support.	Allows you to generate time-limited device programming files for the SR-IOV interface.

1.5. Intel Arria 10 Hard IP for PCI Express* IP Core v16.0

Table 5. 16.0 May2016

Description	Impact
All variants now support for Gen3 PIPE mode using the ModelSim® , NCSIM, and VCS simulators	Better visibility for Gen3 simulations.
All variants now support generation of predefined Signal Tap files for IP core debugging.	Simplifies generation and configuration of Signal Tap files for debugging.
For the Avalon® Memory-Mapped (Avalon-MM) with DMA variant, rearchitected Write DMA module for the 128-bit interface to the Application Layer. This version is final in the 16.0 release.	Provides higher throughput for external memories.
For the Avalon-MM with DMA variant, the 256-bit interface to the Application Layer now supports a maximum transfer size of 64 kilobyte (KB).	Large transfers require fewer descriptor table entries.
For the Avalon Streaming (Avalon-ST) with Single Root I/O Virtualization (SR-IOV) variant, rearchitected the SR-IOV bridge to support 4 Physical Functions (PFs) and 2048 Virtual Functions (VFs). This new version is preliminary in the 16.0 release.	Improves support for designs requiring more PFs and VFs. This new version is not backwards compatible with the previous 15.1 release.
For the Avalon-ST with SR-IOV variant, added support for Address Translation Services (ATS) and TLP Processing Hints (TPH).	Support for SR-IOV.
For the Avalon-ST with SR-IOV variant, added Control Shadow interface to read the current settings for some of the VF Control Register fields in the PCI and PCI Express Configuration Spaces.	Improves visibility for VFs.
The Avalon-ST Streaming with SR-IOV variant now requires a license.	You must purchase a license for this variant to run in hardware that is not connected to a host computer running the Quartus Prime software.

1.6. Intel Arria 10 Hard IP for PCI Express* IP Core v15.1

Table 6. 15.1 November 2015

Description	Impact
Added **Example Designs** tab that automatically generates both simulation and hardware example designs with the parameters you specify.	You can now download an example design to the Altera Arria 10 GX FPGA Development Kit using only the automatically generated files.
Revised the component GUI. For example, is a new single parameter, **HIP mode** combines all supported data rates, interface widths and frequencies as a single parameter.	Improves usability of the component GUI.
Added support for optional Avalon-ST `clr_st` reset output port which has the same functionality as the `reset_status` in the `hip_rst` conduit interface.	This signal eliminates Avalon Streaming reset warnings.
Increased the number of tags supported to 256 from 64 for the Avalon-MM with DMA interface.	Enhances DMA throughput for high latency systems.
Added support for RX Completion buffer overflow monitoring.	Improves system visibility, resulting in better optimization of RX buffer.
Added preliminary support for Gen3 x4, Gen3 x8, and Gen2 x8 Root Port when you select the 256-bit Avalon-MM interface.	Extends Avalon-MM Root Port support to include 64-, 128-, and 256-bit interfaces.
Replaced the SR-IOV DMA example design with a target example design that includes 1 physical function and 3 virtual functions.	This design provides a simpler introduction to the SR-IOV functionality.
Added support for immediate writes when you select the Avalon-MM with DMA interface.	Provides an efficient mechanism for writing a single dword of data.

1.7. Intel Arria 10 Hard IP for PCI Express* IP Core v15.0

Table 7. 15.0 May 2015

Description	Impact
Added **Enable Altera Debug Master Endpoint (ADME)** parameter to support optional Native PHY register programming with the Altera System Console.	If you turn on this option, you can use the Altera System Console for enhanced debugging.
In IP core variations with the Avalon-MM DMA interface, added support for downstream burst read request for a payload of size up to 4 KBytes, if **Enable burst capability for RXM BAR2 port** is turned on in the Parameter Editor. Previous maximum downstream read request payload size was 512 bytes.	If you choose the Avalon-MM DMA interface, the IP core can receive and process a burst read request for a payload of any size supported by the PCI Express specification (up to 4 KBytes), if it receives such a burst read request on the PCI Express link.
In IP core variations with the Avalon-MM interface, added support to send message TLPs with data payload of any length from a Root Port.	If you choose the Avalon-MM interface, a Root Port IP core can send messages with payload greater than 1 dword.

continued...

Description	Impact
In IP core variations with the Avalon-MM interface, added support for dynamically generated Platform Designer example designs that reflect the parameters that you selected in the Parameter Editor. This feature was new in the IP core v14.1 with the Avalon-ST interface, and is now provided also with the Avalon-MM interface.	If you choose the Avalon-MM interface and click the Example Design button, the Quartus II software generates an example design that matches the current parameter settings, for most IP core variations,
In IP core variations with the Avalon-MM or Avalon-MM DMA interface, added **Enable Hard IP Status Bus when using the AVMM interface** parameter. This parameter makes visible or hides the link status signals, ECC error signals, TX and RX parity error signals, completion header and data signals, and currentspeed signal.	Refer to the Arria 10 HIP for PCI Express Signal Changes v15.0 table.
The IP core no longer generates with a Synopsys Design Constraints file (`.sdc`) that includes a derive_pll_clocks constraint. Instead, in compliance with Arria 10 design requirements, the user must add the timing constraint macro `derive_pll_clocks -create_base_clocks` to a top-level `.sdc` file.	User must add this constraint in a top-level Synopsys Design Constraints file. This constraint was previously included in the IP core SDC file.

Table 8. Arria 10 HIP for PCI Express Signal Changes v15.0

Signals added or modified in version 15.0.

Signal Name	New Behavior
`derr_cor_ext_rcv`	The presence or absence of these signals is now controlled by the new **Enable Hard IP Status Bus when using the AVMM interface** parameter. If the parameter is turned on, the signals are included. If the parameter is turned off, the signals are not available.
`derr_cor_ext_rpl`	
`derr_rpl`	
`dlup`	
`dlup_exit`	
`ev128ns`	
`ev1us`	
`hotrst_exit`	
`int_status[3:0]`	
`l2_exit`	
`lane_act[3:0]`	
`ltssmstate[4:0]`	
`rx_par_err`	
`tx_par_err[1:0]`	
`cfg_par_err`	
`ko_cpl_spc_header[7:0]`	
`ko_cpl_spc_data[11:0]`	
`currentspeed[1:0]`	

1.8. Intel Arria 10 Hard IP for PCI Express* IP Core v14.1

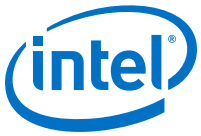
Table 9. 14.1 December 2014

Description	Impact
Reduced Quartus II compilation warnings by 50%.	Reduces time required to vet compilation warnings.
Added support for Single-Root I/O Virtualization (SR-IOV) interface.	If you choose to use the SR-IOV interface, you need to redesign your Application Layer.
Added support for dynamically generated Platform Designer example designs that reflects the parameters that you selected in the Parameter Editor.	If you choose the Avalon-ST interface, the automatically generated testbench has the parameters that you specified.
Added support for Configuration Space Bypass Mode when using the Avalon-ST interface.	If you choose to use Configuration Space Bypass Mode, you need to redesign your Application Layer.
Added Quartus II compilation support for the Avalon-MM with DMA interface.	You can now compile for the Avalon-MM with DMA interface and download the Programmer Object File `.pof` to a development board.
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	If you generate your IP core outside a Quartus II project, you must ensure that you specify a device for your Arria 10 IP core variation and regenerate it in the Quartus II software v14.1.

1.9. Intel Arria 10 Hard IP for PCI Express* IP Core v14.0 Intel Arria 10 Edition

Table 10. v14.0 Arria 10 Edition August 2014

Description	Impact
Changed the PIPE interface to 32 bits for all data rates.	This change requires you to recompile your v13.1 variant in 14.0a10 release
Added simulation log file, `altpcie_monitor_<dev>_dlhip_tlp_file_log.log` in your simulation directory. Generation of the log file requires the following simulation file, `<install_dir>altera/altera_pcie/altera_pcie_a10_hip/altpcie_monitor_a10_dlhip_sim.sv`, that was not present in earlier releases of the Quartus II software.	
Added option to enable 62.5 MHz application clock for Gen1 x1 data rate.	If you choose this option, you must regenerate your IP core.
Added third interface option, Avalon-MM with DMA, that includes a high performance DMA. If you choose this option, you must regenerate your IP core.	
Added option to integrate the Descriptor Controller in the variant for the Avalon-MM with DMA interface.	-



1.10. Intel Arria 10 Hard IP for PCI Express* IP Core v13.1 Arria 10 Edition

Table 11. v13.1 Arria 10 Edition December 2013

Description	Impact
Initial release.	-