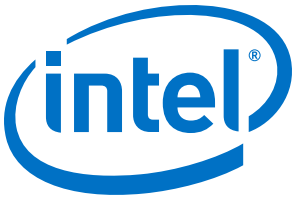

Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core Release Notes

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1 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Quartus Prime Design Suite Update Release Notes*.

Related Links

Quartus Prime Design Suite Update Release Notes

1.1 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v16.0 Revision History

Table 1. v16.0 May 2016

Description	Impact
Verified in Quartus Prime software v16.0	-
Made the following changes: • Changed descriptions in the register definitions.	-

Table 2. 10GBASE-KR IP Core Register Definition Changes v16.0

Register definitions added or modified in version 16.0 for word address 0x4D0.

Bit	RW	Old Register Name	New Register Name	Description
1	RW	dis_max_wait_tmr	—	When set to 1, disables the LT max_wait_timer. Used for characterization mode when setting much longer BER timer values. The default value is 0.
14:12	RW	equal_cnt [2:0]	—	Adds hysteresis to the error count to avoid local minimums. The following values are defined: • 000 = 0 • 001 = 2 • 010 = 4 • 011 = 8 • 100 = 16 • 101 = 32 • 110 = 64 • 111 = 128 The default value is 101.
21:20	RW	rx_ctle_vga_mode	dfe_freeze_mode	Defines the behavior of DFE taps at the end of link training

continued...

Bit	RW	Old Register Name	New Register Name	Description
				• 00 = do not freeze any DFE taps • 01 = Freeze all DFE taps • 10 = reserved • 11 = reserved The default value is 01. *Note:* These bits will be effective only when bit [19] is set to 0.
22	RW	adp_ctle_vga_mode	—	Defines whether or not CTLE/VGA adaptation is in adaptive or manual mode. The following values are defined: • 0 = CTLE sweep before start of TX-EQ during link training. • 1 = manual CTLE mode. Link training algorithm sets fixed CTLE value, as specified in bits [28:24]. The default value is 1 for simulation. The default value is 0 for hardware.
31:29	RW	Manual VGA	—	Defines the VGA value used by the link training algorithm when in manual VGA mode. These bits are only effective when 0x4D0[22] is set to 1. The default value is 4 for simulation. The default value is 7 for hardware.
22	RW	adp_ctle_vga_mode	—	Defines whether or not CTLE/VGA adaptation is in adaptive or manual mode. The following values are defined: • 0 = CTLE sweep before start of TX-EQ during link training. • 1 = manual CTLE mode. Link training algorithm sets fixed CTLE value, as specified in bits [28:24]. The default value is 1 for simulation. The default value is 0 for hardware.

Related Links

- Altera Transceiver PHY IP Core User Guide
- Errata for 10GBASE-R PHY in the Knowledge Base
- Introduction to Altera IP Cores

1.2 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v15.1 Revision History

Table 3. v15.1 November 2015

Description	Impact
Verified in Quartus Prime software v15.1	-
Made the following changes: • Changed the descriptions for tx_serial_clk_1g and rx_cdr_refclk_1g. • Added bit 12 to the 0x4B0 word address.	-

Table 4. 10GBASE-KR IP Core Register Definition Changes v15.1

Register definitions added or modified in version 15.1 for word address 0x4B0.

Bit	RW	Old Register Name	New Register Name	Description
12	RW	N/A	LT failure response	When set to 1, LT failure causes the PHY to go into data mode. When set to 0, LT failure restarts auto-negotiation (if enabled). If auto-negotiation is not enabled, the PHY will restart LT.

Related Links

- Altera Transceiver PHY IP Core User Guide
- Errata for 10GBASE-R PHY in the Knowledge Base
- Introduction to Altera IP Cores

1.3 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v15.0.1 Revision History

Table 5. v15.0.1 June 2015

Description	Impact
Verified in Quartus II software v15.0.1	-
Made the following improvements to the link training (LT) algorithm: • Support for manual VGA tuning • Added option to skip link partner VOD (main tap) adjustment during LT • Added option to enable decision feedback equalization (DFE) at the end of LT • General algorithm improvements for stability	-

Table 6. 10GBASE-KR IP Core Register Definition Changes v15.0.1

Register definitions added or modified in version 15.0.1 for word address 0x4D0.

Bit	RW	Old Register Name	New Register Name	Description
2	RW	quick_mode	Reserved	Reserved
3	RW	pass_one	Reserved	Reserved
18	RW	Ctle_depth	VOD Training Enable	Defines whether or not to skip adjustment of the link partner's VOD (main tap) during link training. The following values are defined: • 1 = Exercise VOD (main tap) adjustment during link training • 0 = Skip VOD (main tap) adjustment during link training The default value is 0.
19	RW	Ctle_depth	Bypass DFE	Defines whether or not Decision Feedback Equalization (DFE) is enabled at the end of link training. The following values are defined: • 1 = Bypass continuous adaptive DFE at the end of link training • 0 = Enable continuous adaptive DFE at the end of link training The default value for simulation is 1. The default value for hardware is 0.

continued...

Bit	RW	Old Register Name	New Register Name	Description
21:20	RW	rx_ctle_mode	rx_ctle_vga_mode	Defines the point at which to enable the RX CTLE in the adaptation algorithm. The following values are defined: • 00 = never, the RX CTLE isn't enabled or adjusted • 01 = trigger CTLE/VGA before starting TX-EQ • 10 = trigger CTLE/VGA after finishing TX-EQ • 11 = trigger CTLE/VGA, both before starting, and after finishing TX-EQ The default value is 00. *Note:* These bits are only effective when 0x4D0[22] is set to 0.
22	RW	Reserved	adp_ctle_vga_mode	Defines whether or not CTLE/VGA adaptation is in adaptive or manual mode. The following values are defined: • 1 = Manual CTLE/VGA mode. Link training algorithm sets fixed CTLE and VGA values as specified in bits 0x4D0[28:24] and 0x4D0[31:29], respectively. • 0 = adaptive CTLE mode. Bits in 0x4D0[21:20] are effective only when this bit is set to 0. The default value is 1.
28:24	RW	Reserved	Manual CTLE	Defines the CTLE value used by the link training algorithm when in manual CTLE mode. These bits are only effective when 0x4D0[22] is set to 1. The default value is 1.
31:29	RW	max_post_step[2:0]	Manual VGA	Defines the VGA value used by the link training algorithm when in manual VGA mode. These bits are only effective when 0x4D0[22] is set to 1. The default value is 4.

Related Links

- Altera Transceiver PHY IP Core User Guide
- Errata for 10GBASE-R PHY in the Knowledge Base
- Introduction to Altera IP Cores

1.4 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v15.0 Revision History

Table 7. v15.0 May 2015

Description	Impact
When adaptation is enabled, the 10GBASE-KR link training may not finish in the required 500 ms. This results in a Link Training Failure. When this occurs, equalization may not be trained optimally for the link.	You can disable adaptation and use a fixed CTLE value during link training. This is done by setting

continued...

Description	Impact
	0x4D0[22:20] to 4, and 0x4D0[28:24] to the desired CTLE value.
The 10GBASE-KR register, 0x4d2[0] Link Trained – Receiver status, is read incorrectly as 0 when testing on HW. It will be read back correctly during simulation.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base
- Introduction to Altera IP Cores

1.5 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v14.1 Revision History

Table 8. v14.1 December 2014

Description	Impact
Verified in Quartus II software v14.1	-
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base
- Introduction to Altera IP Cores

1.6 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v14.0 Revision History

Table 9. v14.0 August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-
Removed the following parameters from the **Link Training** tab: • **Enable daisy chain mode**. • **Enable microprocessor interface**.	-
Changed the default values of the following PMA parameters under the **Link Training** tab:	-

continued...

Description	Impact
• **VMAXRULE** • **VMINRULE** • **VODMINRULE** • **VPOSTRULE** • **VPRERULE** • **PREMAINVAL** • **INITMAINVAL** • **INITPOSTVAL** • **INITPREVAL**	
Changed Avalon Memory-Mapped (AVMM) clock frequency from 125 MHz to 161 MHz to support NIOS II. The AVMM slave interface provides access to the IP core registers.	-
IEEE 1588 Precision Time Protocols are not supported in backplane applications.	-
Link Training takes more time in simulation as NIOS command processing is slower.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base
- Introduction to Altera IP Cores

1.7 Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core v13.1 Revision History

Table 10. v13.1 December 2013

Description	Impact
Initial release	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for the Arria 10 1G/10GbE and 10GBASE-KR PHY MegaCore Function in the Knowledge Base
- Introduction to Altera IP Cores