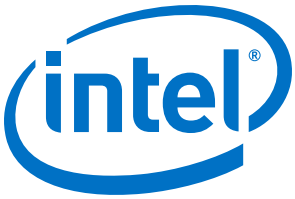

Ethernet Design Example Components Release Notes

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Contents

Ethernet Design Example Components Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Ethernet Design Example Components User Guide
- Errata for the Ethernet Design Example Components in the Knowledge Base

Ethernet Design Example Components v19.2.0

Table 1. v19.2.0 2020.12.14

Intel Quartus Prime Version	Description	Impact
20.4	Added a new SYNC_MODE for Ethernet IEEE 1588 Time of Day Clock Intel FPGA IP that synchronizes TOD from 125 MHz to 402.8 MHz.	—

Table 2. v19.2.0 2020.06.24

Intel Quartus Prime Version	Description	Impact
19.2	Added support for Intel Agilex™ devices for the following IPs: • Ethernet IEEE 1588 Time of Day Clock Intel FPGA IP • Ethernet IEEE 1588 Time-of-day Synchronizer Intel FPGA IP	—

Ethernet Design Example Components v18.0

Table 3. v18.0 2018.05.10

Intel Quartus Prime Version	Description	Impact
18.0	Renamed the following Ethernet design example component names as per Intel FPGA IP rebranding: • "Ethernet IEEE 1588 TOD Synchronizer" to "Ethernet IEEE 1588 TOD Synchronizer Intel FPGA IP" • "Ethernet IEEE 1588 Time of Day Clock" to "Ethernet IEEE 1588 Time of Day Clock Intel FPGA IP" • "Ethernet Packet Classifier" to "Ethernet Packet ClassifierIntel FPGA IP"	—
	Added support for higher fMAX of 402.83 MHz for Ethernet IEEE 1588 Time of Day Clock Intel FPGA IP.	—

Ethernet Design Example Components v17.1

Table 4. v17.1 2017.11.06

Intel Quartus Prime Version	Description	Impact
17.1	Added support for Intel Cyclone® 10 GX devices for the following IPs: • Ethernet IEEE 1588 Time of Day Clock Intel FPGA IP • Ethernet IEEE 1588 Time-of-day Synchronizer Intel FPGA IP	—

Ethernet Design Example Components v17.0

Table 5. v17.0 2017.05.08

Intel Quartus Prime Version	Description	Impact
17.0	Added support for Intel Stratix® 10 devices.	—

Ethernet Design Example Components v16.0

Table 6. v16.0 2016.05.02

Intel Quartus Prime Version	Description	Impact
16.0	Initial release in the Intel FPGA IP IP Library.	—

Ethernet Design Example Components User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

Intel Quartus Prime Version	IP Core Version	User Guide
19.3	19.2.0	Ethernet Design Example Components User Guide
18.0	18.0	Ethernet Design Example Components User Guide
16.0	16.0	Ethernet Design Example Components User Guide