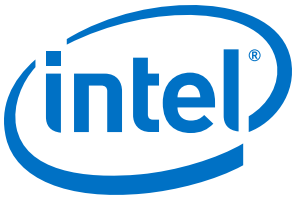

# Low Latency E-Tile 40G Ethernet Intel® FPGA IP Release Notes

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# Contents

# 1. Low Latency E-Tile 40G Ethernet Intel® FPGA IP Release Notes

IP versions are the same as the Intel® Quartus® Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

**Related Information**

- Intel Quartus Prime Design Suite Update Release Notes
- Low Latency E-Tile 40G Ethernet Intel FPGA IP User Guide
- Low Latency E-Tile 40G Ethernet Intel FPGA IP Design Example User Guide

## 1.1. Low Latency E-Tile 40G Ethernet Intel FPGA IP v21.0.0

**Table 1. v21.0.0 2020.09.28**

| Intel Quartus Prime Version | Description | Impact |
|---|---|---|
| 20.3 | Updated the `reconfig_address` signal width from 21-bit address to a 20-bit address. | Removed deprecated bit [21]. |

## 1.2. Low Latency E-Tile 40G Ethernet Intel FPGA IP v20.0.0

**Table 2. v20.0.0 2020.06.22**

| Intel Quartus Prime Version | Description | Impact |
|---|---|---|
| 20.2 | Added device support for Intel Agilex™ devices. | You can now use this IP in Intel Agilex devices. |

## 1.3. Low Latency E-Tile 40G Ethernet Intel FPGA IP v19.1.0

### Table 3. v19.1.0 2020.04.13

| Intel Quartus Prime Version | Description | Impact |
|---|---|---|
| 20.1 | Initial release in the Intel FPGA IP Library. | — |

## 1.4. Low Latency E-Tile 40G Ethernet Intel FPGA IP User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

| Intel Quartus Prime Version | IP Core Version | User Guide |
|---|---|---|
| 20.2 | 20.0.0 | Low Latency E-Tile 40G Ethernet Intel FPGA IP User Guide |
| 20.1 | 19.1.0 | Low Latency E-Tile 40G Ethernet Intel FPGA IP User Guide |

## 1.5. Low Latency E-Tile 40G Ethernet Intel FPGA IP Design Example User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

| Intel Quartus Prime Version | IP Core Version | User Guide |
|---|---|---|
| 20.2 | 20.0.0 | Low Latency E-Tile 40G Ethernet Intel FPGA IP Design Example User Guide |
| 20.1 | 19.1.0 | Intel Stratix 10 Low Latency E-Tile 40G Ethernet Design Example User Guide |