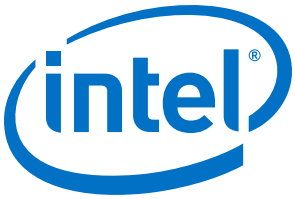

E-Tile Dynamic Reconfiguration Design Example Release Notes

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Contents

1. E-Tile Dynamic Reconfiguration Design Example Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- E-tile Hard IP for Ethernet and CPRI PHY Intel FPGA IPs User Guide
- E-tile Hard IP Intel Stratix® 10 Design Examples User Guide: Ethernet, CPRI PHY, and Dynamic Reconfiguration
- Errata for Intel FPGA IPs in the Knowledge Base

1.1. E-Tile Dynamic Reconfiguration Design Example v20.2.0

Table 1. v20.2.0 2020.06.22

Intel Quartus Prime Version	Description	Impact
20.2	• Added support for **new** dynamic reconfiguration transitions from high speed CPRI protocol to low PMA-D modes: — 24G CPRI with RS-FEC to 10G CPRI — 10G CPRI to 9.8G CPRI — 9.8G CPRI to 4.9G CPRI — 4.9G CPRI to 2.4G CPRI — 2.4G CPRI to 24G CPRI with RS-FEC	—

1.2. E-Tile Dynamic Reconfiguration Design Example v20.1.0

Table 2. v20.1.0 2020.04.13

Intel Quartus Prime Version	Description	Impact
20.1	Added support for deterministic latency in the 25G Ethernet to CPRI DR protocol.	—

1.3. E-Tile Dynamic Reconfiguration Design Example v19.4.0

Table 3. v19.4.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	Added **new** 9.8G CPRI dynamic reconfiguration design example with support for: • Dynamic reconfiguration switching between 2.4G, 3G, 4.9G, 6G, and 9.8G speed modes. • Any-to-any transition support for all available speed modes. • New hardware TEST_MODE parameter selection between the internal serial loopback with and without PMA adaptation and the external serial loopback with PMA adaptation.	—
	Updated 24G CPRI with RS-FEC dynamic reconfiguration design example: • Added support for 3G, 6G, 10G with RS-FEC 12G, and 12G with RS-FEC speed modes. • Added any-to-any transition support for all available speed modes. • Added new hardware TEST_MODE parameter to support internal serial loopback with and without PMA adaptation or external serial loopback with PMA adaptation.	—
	Added **new** 100G Ethernet dynamic reconfiguration example support for 100G to 4x25G and vice versa with optional RS-FEC.	—
	Updated PMA adaptation flow for all high-speed modes: • 10G/25G with optional RS-FEC and PTP • 10G/24G CPRI with optional RS-FEC • 9.8G CPRI Added new manual CTLE flow for low-speed CPRI modes: • 6G CPRI • 4.9G CPRI • 3G CPRI • 2.4G CPRI	—
	Updated release for Intel Agilex™ devices. Added hardware support for the following dynamic reconfiguration design examples: • 25G Ethernet with PTP and optional RS-FEC • 25G Ethernet with optional RS-FEC • 25G Ethernet to CPRI protocol • 24G CPRI with optional RS-FEC • 9.8G CPRI	—

1.4. E-tile Dynamic Reconfiguration Design Example v19.3.0

Table 4. v19.3.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Initial release for Intel Agilex devices. • Added support for the following dynamic reconfiguration design examples: — 10G/25G Ethernet (single-channel design only) — 25G Ethernet to CPRI	—

1.5. E-tile Dynamic Reconfiguration Design Example v19.2.0

Table 5. v19.2.0 2019.07.01

Intel Quartus Prime Version	Description	Impact
19.2	• Added new **25G Ethernet to CPRI Protocol** dynamic reconfiguration protocol design • Added new 25G Ethernet to CPRI dynamic reconfiguration design example	—

1.6. E-tile Dynamic Reconfiguration Design Example v19.1

Table 6. v19.1 April 2019

Description	Impact
Initial release for Intel Stratix® 10 devices. • Added support for the following dynamic reconfiguration design examples: — 10G/25G Ethernet (single-channel design only) — 10G/24G CPRI (single-channel design only)	—

1.7. E-tile Dynamic Reconfiguration Design Example User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.
If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	Intel Stratix 10 User Guide
20.1	E-tile Hard IP Intel Stratix 10 Design Examples User Guide
19.4	E-tile Hard IP Intel Stratix 10 Design Examples User Guide
19.3	E-tile Hard IP Intel Stratix 10 Design Examples User Guide
19.2	E-tile Hard IP Intel Stratix 10 Design Examples User Guide

continued...

IP Core Version	Intel Stratix 10 User Guide
19.1	E-tile Hard IP Intel Stratix 10 Design Examples User Guide
18.1.1	E-tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Design Example User Guide
18.0	E-tile Hard IP for Ethernet Intel Stratix 10 FPGA IP Design Example User Guide