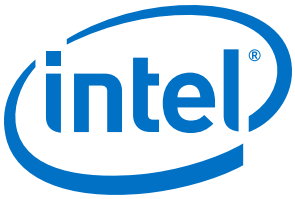

Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP Release Notes

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1. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel® FPGA IP Release Notes

If a release note is not available for a specific IP version, the IP has no changes in that version. For information on IP update releases up to v18.1, refer to the *Intel® Quartus® Prime Design Suite Update Release Notes*.

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Intel Quartus Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Related Information

- Intel Quartus Prime Design Suite Update Release Notes
- Intel Agilex™ Embedded Memory User Guide
- Intel Stratix® 10 Embedded Memory User Guide
- Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, ROM: 1-PORT, and ROM: 2-PORT) User Guide
- Errata for the Embedded Memory Intel FPGA IPs in the Knowledge Base

1.1. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP v20.2.0

1.1.1. RAM: 2-PORT Intel FPGA IP v20.2.0

Table 1. v20.2.0 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Removed support for the **Use Stratix M512 emulation logic cell style for the LCs memory block type** option for Intel Stratix® 10 and Intel Agilex™ devices.	You are required to either change to default logic cell style or switch to non-LCs memory block type.
	Removed the **Do not analyze the timing between write and read operation. Metastability issues are prevented by never writing and reading at the same address at the same time.** option for Intel Stratix 10 and Intel Agilex devices.	You are required to perform IP upgrade if you set the option to false (default is true).
	Updated the following parameter settings tab names: • **Output 1** to **Mixed Port Read-During-Write** • **Output 2** to **Same Port Read-During-Write**	—

1.2. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP v20.1.0

1.2.1. RAM: 1-PORT Intel FPGA IP v20.1.0

Table 2. v20.1.0 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Removed support for **Use Stratix M512 emulation logic cell style** for the LCs memory block type in the Intel Stratix 10 and Intel Agilex devices.	You are required to either change to default logic cell style or switch to non-LCs memory block type in the Intel Stratix 10 and Intel Agilex devices.
	Added "X" propagation support in simulation model for the Intel Stratix 10 devices.	—

Table 3. v20.1.0 2020.08.03

Intel Quartus Prime Version	Description	Impact
20.1	Enabled the In-System Memory Content Editor (ISMCE) support in the Intel Agilex devices.	This change is optional. If you do not upgrade your IP, it does not have this new feature.

1.2.2. RAM: 2-PORT Intel FPGA IP v20.1.0

Table 4. v20.1.0 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Added "X" propagation support in simulation model for Intel Stratix 10 devices.	—

Table 5. v20.1.0 2020.08.03

Intel Quartus Prime Version	Description	Impact
20.1	Disabled the low power (LP) option for the true dual port for Intel Agilex devices.	You are required to perform IP upgrade if you are setting the LP mode in the true dual port in the Intel Agilex devices.

1.2.3. RAM: 4-PORT Intel FPGA IP v20.1.0

Table 6. v20.1.0 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Added "X" propagation support in simulation model for the Intel Stratix 10 devices.	—

Table 7. v20.1.0 2020.08.03

Intel Quartus Prime Version	Description	Impact
20.1	Disabled the LP option in the Intel Agilex devices.	You are required to perform IP upgrade if you are setting the LP mode in the Intel Agilex devices.

1.2.4. ROM: 1-PORT Intel FPGA IP v20.1.0

Table 8. v20.1.0 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Removed support for **Use Stratix M512 emulation logic cell style** for the LCs memory block type in the Intel Stratix 10 and Intel Agilex devices.	You are required to either change to default logic cell style or switch to non-LCs memory block type in the Intel Stratix 10 and Intel Agilex devices.
	Added "X" propagation support in simulation model for the Intel Stratix 10 devices.	—

Table 9. v20.1.0 2020.08.03

Intel Quartus Prime Version	Description	Impact
20.1	Enabled the In-System Memory Content Editor (ISMCE) support in the Intel Agilex devices.	This change is optional. If you do not upgrade your IP, it does not have this new feature.

1.2.5. ROM: 2-PORT Intel FPGA IP v20.1.0

Table 10. v20.1.0 2020.10.12

Intel Quartus Prime Version	Description	Impact
20.3	Added "X" propagation support in simulation model for the Intel Stratix 10 devices.	—

Table 11. v20.1.0 2020.08.03

Intel Quartus Prime Version	Description	Impact
20.1	Disabled the LP option in the Intel Agilex devices.	You are required to perform IP upgrade if you are setting the LP mode in the Intel Agilex devices.

1.3. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP v20.0.0

Table 12. v20.0.0 2019.12.16

Intel Quartus Prime Version	Description	Impact
19.4	In the Intel Quartus Prime Pro Edition software version 19.3 version of the RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IPs, you may encounter `Error (272006): Parameter OPTIMIZATION_OPTION can only be set to AUTO for device family <device_family>` during synthesis. This error occurs in designs that include embedded memory IPs with the RAM_BLOCK_TYPE set to M20K and that have been upgraded from version 19.2. This issue has been fixed in Intel Quartus Prime Pro Edition version 19.4.1.	You are required to perform IP upgrade for this fix. Refer to the KDB page for more information.

Related Information

KDB Link: Error (272006): Parameter OPTIMIZATION_OPTION can only be set to AUTO for device family <device_family>

1.4. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP v19.2.0

Table 13. v19.2.0 2019.09.30

Intel Quartus Prime Version	Description	Impact
19.3	Initial release for Intel Agilex devices for the following embedded memory IP cores: • RAM: 1-PORT Intel FPGA IP • RAM: 2-PORT Intel FPGA IP • RAM: 4-PORT Intel FPGA IP • ROM: 1-PORT Intel FPGA IP • ROM: 2-PORT Intel FPGA IP	—

1.5. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP v19.1

Table 14. v19.1 2019.04.05

Intel Quartus Prime Version	Description	Impact
19.1	Enabled address clear in the Intel Agilex devices in the following IPs: • RAM: 2-PORT Intel FPGA IP • RAM: 4-PORT Intel FPGA IP. • ROM: 1-PORT Intel FPGA IP.	—

1.6. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP v18.1

Table 15. v18.1 2019.04.05

Intel Quartus Prime Version	Description	Impact
18.1	Fixed the emulated true dual port on `rden` and `valid` signal connection for the RAM: 2-PORT Intel FPGA IP.	—
	Disabled the options of `addressstall` for the Intel Stratix 10 devices for the ROM: 2-PORT Intel FPGA IP.	—

1.7. Embedded Memory (RAM: 1-PORT, RAM: 2-PORT, RAM: 4-PORT, ROM: 1-PORT, and ROM: 2-PORT) Intel FPGA IP v18.0

Table 16. v18.0 May 2018

Description	Impact
Renamed the following IP cores as per Intel rebranding: • RAM: 1-PORT IP core to RAM: 1-PORT Intel FPGA IP • RAM: 2-PORT IP core to RAM: 2-PORT Intel FPGA IP • RAM: 4-PORT IP core to RAM: 4-PORT Intel FPGA IP • ROM: 1-PORT IP core to ROM: 1-PORT Intel FPGA IP • ROM: 2-PORT IP core to ROM: 2-PORT Intel FPGA IP	—

Related Information

- Introduction to Intel FPGA IP Cores
- Intel Stratix 10 Embedded Memory User Guide
- Errata for other IP cores in the Knowledge Base