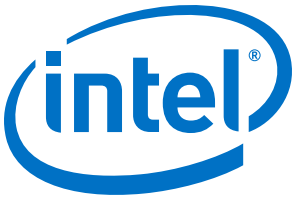

100G Interlaken IP Core Release Notes

RN-1106
2016.05.02

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Contents

1 100G Interlaken IP Core Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Intel Quartus Prime Design Suite Update Release Notes*.

Related Links

Intel Quartus Prime Design Suite Update Release Notes

1.1 100G Interlaken IP Core v16.0

Table 1. Version 16.0 May 2016

Description	Impact	Notes
Added **Example Designs** tab that automatically generates both simulation and hardware example designs with the parameters you specify.	You can now download an example design to the Altera Arria 10 GX FPGA Development Kit using only the automatically generated files.	

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.2 100G Interlaken IP Core v15.1

Table 2. Version 15.1 November 2015

Description	Impact	Notes
Added new **Enable Native XCVR PHY ADME** parameter for Arria 10 variations..	Upgrading the IP core to incorporate this feature is optional. This change does not affect the top-level signals of the IP core.	This parameter exposes control of transceiver configuration features.
Changed behavior of `irx_err` signal. Previously, if the IP core could not determine the burst in which the error occurred, it asserted the `irx_err` signal anyway, and the client could also not determine the associated burst. Now, if the IP core cannot determine the burst in which an error occurred, it does not assert the `irx_err` signal. If it can determine the burst in which an error occurred, it asserts the `irx_err` signal during the end of burst cycle (when it also asserts `irx_eob`).	This change ensures that apparent errors that occur during Idle cycles do not cause the `irx_err` signal to assert. Upgrading the IP core to incorporate this feature is optional. If you upgrade your IP core you should be aware of the change in signal behavior.	Refer to 100G Interlaken IP Core Signal Changes v15.1 table.
Added hardware design example for Arria 10 variations.	A hardware design example is now available with tArria 10 variations of the 100G Interlaken IP core.	
Modified instructions to generate legacy testbench.		

Table 3. 100G Interlaken IP Core Signal Changes v15.1

Signals added or modified in version 15.1.

Old Signal Name	New Signal Name	Notes
irx_err	irx_err	Changed behavior of irx_err signal. The IP core asserts the signal in a subset of the cases in which it asserted this signal in the previous release, and always asserts this signal synchronously with the irx_eob signal of the burst in which the error occurred.

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.3 100G Interlaken IP Core v15.0

Table 4. Version 15.0 May 2015

Description	Impact	Notes
Added new **TX scrambler seed** parameter.	This feature adds support for modification of the TX scrambler seed for Arria 10 variations. If your design includes multiple IP cores, you should ensure they have different TX scrambler seed values. Previously this functionality was not available for Arria 10 variations. In addition, starting in the IP core version 15.0, you must refrain from modifying the RTL parameter SCRAM_CONST in Stratix V and Arria V GZ variations, and use the new parameter in the Parameter Editor instead.	

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.4 100G Interlaken IP Core v14.1

Table 5. Version 14.1 December 2014

Description	Impact	Notes
The Quartus II software v14.1 requires that you specify a device if your IP core targets the Arria 10 device family. If you do not specify your target Arria 10 device, the IP Upgrade tool insists that your IP core requires upgrade, but does not clarify the reason.	You must ensure that you specify a device for your v13.1 Arria 10 Edition or v14.0 Arria 10 Edition IP core variation and regenerate it in the Quartus II software v14.1.	

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.5 100G Interlaken IP Core v14.0 Arria 10 Edition

Table 6. Version 14.0 Arria 10 Edition August 2014

Description	Impact	Notes
Verified in the Quartus II software v14.0 Arria 10 Edition.		

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.6 100G Interlaken IP Core v14.0

Table 7. Version 14.0 June 2014

Description	Impact	Notes
Removed `mm_clk_locked` input signal.	Port change.	
Removed hidden parameter `CNTR_BITS` from top level RTL files.		
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.		

Related Links

- Introduction to Altera IP Cores
- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.7 100G Interlaken IP Core v13.1 Arria 10 Edition

Table 8. Version 13.1 Arria 10 Edition December 2013

Description	Impact	Notes
Added support for Arria 10 devices. IP core variations that target an Arria 10 device have additional interfaces and design requirements.		

Table 9. 100G Interlaken IP Core Signal Changes

Signals added or modified in version 13.1 Arria 10 Edition.

Old Signal Name	New Signal Name	Notes
—	tx_serial_clk	New interface to external TX PLL. Relevant for Arria 10 variations only.
—	tx_pll_locked	
—	tx_pll_powerdown	
—	tx_cal_busy	
—	reconfig_clk	New Arria 10 transceiver reconfiguration interface. Relevant for Arria 10 variations only.
—	reconfig_reset	
—	reconfig_read	

continued...

Old Signal Name	New Signal Name	Notes
—	reconfig_write	
—	reconfig_address[13:0] or reconfig_address[14:0]	
—	reconfig_readdata[31:0]	
—	reconfig_waitrequest	
—	reconfig_writedata[31:0]	
reconfig_to_xcvr	Not present in Arria 10 variations.	Transceiver reconfiguration interface for Arria V and Stratix V variations. This interface is present only in Arria V and Stratix V variations (as supported in past and future versions of the Quartus II software). It is not present in Arria 10 variations.
reconfig_from_xcvr	Not present in Arria 10 variations.	

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.8 100G Interlaken IP Core v13.1

Table 10. Version 13.1 November 2013

Description	Impact	Notes
Added optional ECC feature on M20K blocks in Stratix V devices.		
Added bit error injection testing feature to check CRC24 error detection.		
Changed implementation of single segment mode: • Changed parameter name from **Received data format** to **Data format**. • If you select Single segment mode, the IP core can no longer handle incoming dual segment traffic on the TX client data interface.		
Added four new parameters to optionally include advanced error reporting and handling, Stratix V M20K block ECC feature, diagnostic features, and in-band flow control functionality. Excluding the features improves resource utilization.		
Changed the behavior of the management interface during read operations. The IP core asserts the `mm_rddata_valid` signal two `mm_clk` cycles after the `mm_read` signal is asserted, instead of one `mm_clk` cycle as in previous versions of the IP core.		

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base

1.9 100G Interlaken IP Core v13.0

Table 11. Version 13.0 May 2013

Description	Impact	Notes
Added dual segment mode.		
Added packet mode option in parameter editor.		

continued...

Description	Impact	Notes
Improved error handling.		
Added PRBS capability.		
Added CRC-32 error injection capability.		

Related Links

- 100G Interlaken MegaCore Function User Guide
- Errata for 100G Interlaken IP core in the Knowledge Base