

Quartus II Software and Device Support Release Notes Arria 10 Edition 14.0

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This document provides late-breaking information about the Altera® Quartus® II software release version 14.0 Arria® 10 edition.

For information about operating system support, refer to the **readme.txt** file in your **altera/<version number>/quartus directory**.

Release Description

The Quartus II software release version 14.0 Arria 10 edition provides support for Arria 10 devices only. All other Altera devices are supported by the Quartus II software release version 14.0. The Quartus II software release version 14.0 Arria 10 edition requires a subscription edition license.

Note: To migrate a design to an Arria 10 device, some IP cores must be removed and replaced with a new IP variant specific to the Arria 10 device family.

Memory Recommendations

A full installation of the Quartus II software requires up to 18 GB of available disk space.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

Note: Peak virtual memory may exceed these recommendations. These recommendations are based on the amount of physical memory required to achieve runtime within 10% of that achieved on hardware with an infinite amount of RAM.

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Table 1: Memory Requirements for Processing Designs

These requirements are the same for both Windows and Linux installations.

Family	Device	Recommended Physical RAM
Arria 10	10AS048, 10AX048	28 GB
	10AS057, 10AX057	30 GB
	10AS066, 10AX066	32 GB
	10AT090, 10AX090	44 GB
	10AT115, 10AX115	48 GB

Changes in Device Support

Table 2: Device Support Fixed

Description	Workaround
<p>Pin-Out File might contain incorrect voltages in Quartus II software release version 13.1 Arria 10 Edition</p> <p>The Pin-Out File (.pin) generated by the Quartus II software might contain incorrect voltages for some Arria 10 ES voltage rails. The voltage rails affected are:</p> <ul style="list-style-type: none"> • VCC • VCCL • VCCERAM • VCCL_HPS • VCCIOREF_HPS • VCCPLL_HPS 	<p>This issue is corrected in Quartus II software release version 14.0 Arria 10 Edition.</p>
<p>Default VCCIO voltage for 10AX115 devices is incorrect in Quartus II software release version 13.1 Arria 10 Edition</p> <p>On the Voltage page of the Quartus II software, the default voltage listed for VCCIO (2.5 V) is incorrect.</p>	<p>This issue is corrected in Quartus II software release version 14.0 Arria 10 Edition.</p>

Related Information

[Altera Knowledge Base](#)

For more information about known device issues and workarounds.

Changes in Software Behavior

This section documents instances in which the behavior and default settings of the Quartus II software have been changed from earlier releases of the software, and known issues with the software.

Refer to the Quartus II Default Settings File (.qdf), *<Quartus II installation directory>/quartus/bin/assignment_defaults.qdf*, for a list of all the default assignment settings for the latest version of the Quartus II software.

Description	Workaround
<p>Advanced Physical Optimization</p> <p>The Quartus II software release version 14.0 Arria 10 edition includes the new <code>ADVANCED_PHYSICAL_OPTIMIZATION</code> setting. <code>ADVANCED_PHYSICAL_OPTIMIZATION</code> is turned on by default.</p>	<p>The <code>ADVANCED_PHYSICAL_OPTIMIZATION</code> setting was not included in the Quartus II software release version 13.1 Arria 10 edition. You must turn the setting off to restore previous behavior.</p>
<p>Compilation Results in the Quartus II Software Release Version 14.0 Arria 10 Edition Differ When Using Different <code>num_parallel_processors</code> .qsf Values</p> <p>In the Quartus II software release version 14.0 Arria 10 edition, when you compile a design for an Arria 10 device or use the <code>ADVANCED_PHYSICAL_OPTIMIZATION</code> Quartus II Settings File (.qsf) setting, using different values for the <code>NUM_PARALLEL_PROCESSORS</code> .qsf setting might generate different compilation results. Note that <code>ADVANCED_PHYSICAL_OPTIMIZATION</code> is enabled as a default setting in the Arria 10 edition of the 14.0 Quartus II software so this issue impacts designs using default setting options.</p> <p>For example, if you compile an Arria 10 device design and enable <code>ADVANCED_PHYSICAL_OPTIMIZATION</code>, a Quartus II software compilation run with the <code>NUM_PARALLEL_PROCESSORS</code> .qsf setting set to 4 will not necessarily generate the same results if you compile the same design with the <code>NUM_PARALLEL_PROCESSORS</code> .qsf setting set to 8.</p>	<p>You must set a fixed value for the <code>NUM_PARALLEL_PROCESSORS</code> .qsf setting or leave the value unspecified.</p>

Device Support and Pin-Out Status

Table 3: Advance Device Support

Compilation, simulation, and timing analysis support is provided for these devices. The Compiler generates pin-out information for these devices in this release, but does not generate programming files.

Device Family	Devices
Arria 10	10AX057, 10AS057, 10AX066, 10AS066, 10AX090, 10AT090, 10AX115, 10AT115

Table 4: Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for these devices. Programming files and pin-out information are not generated for these devices in this release.

Device Family	Devices
Arria 10	10AX048, 10AS048

Timing and Power Models

Table 5: Timing and Power Model Status for Arria 10 Devices

Device Family	Device	Timing Model Status ⁽¹⁾	Power Model Status
Arria 10	10AX048, 10AS048	Advance	Preliminary
	10AX057, 10AS057	Advance	Preliminary
	10AX066, 10AS066	Advance	Preliminary
	10AX090, 10AT090	Preliminary	Preliminary
	10AX115, 10AT115	Preliminary	Preliminary

Related Information

[System Design with Advance FPGA Timing Models](#)

IBIS Models

Table 6: IBIS Model Status for the Quartus II Software Release Version 14.0 Arria 10 Edition

Device Family	IBIS Model Status
Arria 10	Preliminary - 14.0

⁽¹⁾ This release contains advance timing models for some Arria 10 devices. These models will change and should not be relied on for production timing. For more information about working with advance timing models, please review the *System Design with Advance FPGA Timing Models* white paper or contact Altera.

EDA Interface Information

Synthesis Tools

Table 7: Synthesis Tools Supporting the Quartus II Software Release Version 14.0 Arria 10 Edition

Synthesis Tools ⁽²⁾	Version ⁽³⁾	NativeLink Support
Mentor Graphics® Precision	2014a	Yes
Synopsys® Synplify, Synplify Pro, and Synplify Premier	E-2014.03-SP1	Yes

Simulation Tools

Table 8: Simulation Tools Supporting the Quartus II Software Release Version 14.0 Arria 10 Edition

Simulation Tools	Version	NativeLink Support
Aldec Active-HDL	9.3 (Windows only)	Yes
Aldec Riviera-PRO	2013.10	Yes
Cadence Incisive Enterprise Simulator (IES)	13.10.012 (Linux only)	Yes
Mentor Graphics ModelSim® PE	10.1e	Yes
Mentor Graphics ModelSim SE	10.2c	Yes
Mentor Graphics ModelSim-Altera	10.1e	Yes
Mentor Graphics Questa®	10.2c	Yes
Synopsys VCS and VCS MX	2013.06-1	Yes

⁽²⁾ EDA Synthesis tools that support Arria 10 devices will be released by vendors shortly after the release of the Quartus II software release version 14.0 Arria 10 edition. Contact your vendor account manager for details.

⁽³⁾ The versions currently listed in this column are for the Quartus II software release version 13.1 Arria 10 edition.

Antivirus Verification

The Quartus II software release version 14.0 Arria 10 edition has been verified virus free using the following software:

McAfee VirusScan Enterprise + AntiSpyware Enterprise Version: 8.8.0 (8.8.0.975)
Scan Engine Version (32 bit): 5600.1067
Scan Engine Version (64 bit): 5600.1067
DAT Version: 7464.0000

Software Issues Resolved

Table 9: Issues Resolved in the Quartus II Software Release Version 14.0 Arria 10 Edition

Customer Service Request Numbers							
10994344	11035316	11043735	11047870	11052822	11057898	11064046	11070937
10999900	11035676	11045624	11048149	11053439	11057943	11064183	11073780
11031388	11035886	11046042	11048212	11053940	11058575	11065389	—
11032502	11039859	11046664	11050559	11054381	11059688	11065630	—
11032699	11041068	11046770	11051111	11055201	11060137	11066735	—
11034403	11041564	11046777	11051255	11056440	11060523	11067502	—
11035052	11042584	11047047	11051925	11056820	11062003	11068478	—
11035187	11042860	11047869	11052098	11056821	11062113	11070369	—

Software Patches Included in this Release

Table 10: Software Patches included in the Quartus II Software Release Version 14.0 Arria 10 Edition

Quartus II Software Version	Patch	Customer Service Request Number
13.1a10.2	2.02a	—

Latest Known Quartus II Software Issues

Table 11: Latest Known Quartus II Software Release Version 14.0 Arria 10 Edition Issues

Description	Workaround
<p>IP Migration to the Quartus II Software Release Version 14.0 Arria 10 Edition Fails</p> <p>When migrating your IP to the Quartus II software release version 14.0 Arria 10 edition, the migration might fail if you have a previous version of the Quartus II software open simultaneously.</p>	<p>Ensure you only have the Quartus II software release version 14.0 Arria 10 edition open during IP migration.</p>
<p>LVDS SERDES IP Core in CDR Mode RTL Simulations Fail in ModelSim</p> <p>In the Quartus II software release version 14.0 Arria 10 edition, ModelSim register transfer level (RTL) simulations for the LVDS SERDES IP Core in clock data recovery (CDR) mode fail. This issue applies to QuestaSim, ModelSim AE and ModelSim SE.</p>	<p>The simulations work if you turn off ModelSim optimizations (no-vopt).</p>
<p>Qsys Device Selection Issues in the Quartus II Software Release Version 14.0 Arria 10 Edition</p> <p>The Qsys system integration tool has two issues with device selection:</p> <ol style="list-style-type: none"> 1. Qsys defaults to a “default” device when no device family is specified in the Arria 10 edition of the Quartus II software release version 14.0. 2. When you select the "auto" device in the Quartus II software and launch Qsys or the IP parameter editor, the Quartus II software device family setting is not passed back to Qsys or the IP parameter editor. 	<p>You must select a specific device in the Quartus II software before you launch Qsys or the IP parameter editor. Do not select the "auto" device setting.</p> <p>Alternatively, you can select the device family from within Qsys or the IP parameter editor.</p>
<p>The Quartus II Software Release Version 14.0 Arria 10 Edition Has Two Identical VCCR Options for Arria 10 Devices in the GUI</p> <p>In the Quartus II software release version 14.0 Arria 10 edition, the GUI has two identical VCCR options for Arria 10 devices under Assignments > Settings > Operating Settings and Conditions > Voltage. The two identical options appear next to each other in the Voltage pane of the Settings window.</p>	<p>You can ignore the Arria 10 VCCR options under Assignments > Settings > Operating Settings and Conditions > Voltage; the VCCR options that appear in the GUI are not the VCCR_GXB supply.</p>

Description	Workaround
<p>PLL dynamic reconfiguration reset does not restore the originally programmed PLL settings in the Arria 10 device</p>	<p>Please refer to the Altera Knowledge Base support solution located at http://www.altera.com/support/kdb/solutions/fb203040.html.</p>
<p>Cannot Generate PowerPlay Early Power Estimator (EPE) File from the PowerPlay Power Analyzer</p> <p>In the Quartus II software release version 14.0 Arria 10 edition, generating the PowerPlay Early Power Estimator (EPE) File from the PowerPlay Power Analyzer is not supported for designs with unregistered digital signal processing (DSP) blocks. An internal error will occur in the PowerPlay Power Analyzer.</p>	<p>Do not use unregistered DSP blocks when generating an EPE File.</p>
<p>Some IP Cores do not Migrate to the Quartus II Software Release Version 14.0 Arria 10 Edition</p> <p>The following IP cores do not support migration to the Quartus II software release version 14.0 Arria 10 edition:</p> <ul style="list-style-type: none"> • altmult_add • lpm_mux • lpm_add_sub • lpm_constant • lpm_compare • Ram initializer (altmem_init) <p>These IP cores are not included in the IP Catalog.</p> <p>If you launch the MegaWizard Plug-In Manager with the <code>qmegwiz</code> command and attempt to open one of the above IP cores generated with a previous version of the Quartus II software, the parameter editor opens but the device selection menu is empty. You cannot generate these IP cores.</p>	<p>You can only edit or regenerate your previous IP core in the corresponding previous version of the Quartus II software. Alternately, you can use the IP Catalog to select and define a suitable replacement IP core supported in the Quartus II software release version 14.0 Arria 10 edition.</p>

Description	Workaround
<p>Automatic Upgrade of the Transceiver Native PHY IP Core from the Quartus II Software Release Version 13.1 Arria 10 Edition to the Quartus II Software Release Version 14.0 Arria 10 Edition Might Fail</p> <p>Automatic upgrade of the Transceiver Native PHY IP Core created in the Quartus II software release version 13.1 Arria 10 edition might fail if the IP configuration uses the PHY interface for PCI Express (PIPE) Gen3 protocol mode. In the Quartus II software release version 13.1 Arria 10 edition, the Transceiver Native PHY incorrectly allowed illegal data rate settings; the correct data rate setting for PIPE Gen3 is 5000 megabits per second (Mbps).</p>	<p>You must manually update your IP; change the data rate with the Transceiver Native PHY IP GUI parameter editor and regenerate your IP.</p>
<p>In the Quartus II Software Release Version 14.0 Arria 10 Edition, You Cannot Merge PCS-Bonded Simplex TX with Simplex RX in the Transceiver Native PHY IP Core</p> <p>You cannot merge the physical coding sublayer (PCS)-bonded simplex transmitter (TX) with the simplex receiver (RX) in the Transceiver Native PHY IP Core. The Quartus II software compilation will fail at the Fitter stage.</p>	<p>Do not merge the simplex TX with the simplex RX.</p>
<p>Qsys IRQ bridge erroneously inserts clock crossers</p> <p>In the <code>hw.tcl</code> for the Interrupt Request (IRQ) Bridge component of the Qsys system integration tool, the following assignment is commented out: <code>#set_interface_property "sender\${s}_irq" associatedClock "clk"</code></p> <p>This error causes the interrupt request (IRQ) bridge to insert clock crossers, but the IRQ receivers and senders are in the same clock domain.</p>	<p>You must uncomment the following assignment in the IRQ bridge <code>.tcl</code> file:</p> <pre>#set_interface_property "sender\${s}_irq" associatedClock "clk"</pre> <p>This file is included with the product and is located in the IRQ bridge component folder.</p>
<p>Quartus II Software Release Version 14.0 Arria 10 Edition Power Model for 3 V I/O Standards</p> <p>The Quartus II software release version 14.0 Arria 10 edition does not include a power model for 3 V I/O standards.</p>	<p>There is no workaround.</p>

Description	Workaround
<p>Critical Warning (332008) and Error (332000): ERROR Issued by the Fitter in LVDS SERDES IP Core Designs</p> <p>In the Quartus II software release version 14.0 Arria 10 edition, the Fitter issues the following warning and error message:</p> <pre>Critical Warning (332008): Read_sdc failed due to errors in the SDC file Error (332000): ERROR: Argument <node_ object> is an empty collection. Specify one that is a non-empty collection. while executing "get_node_info -name [get_clock_info - target \$iclk_name]" invoked from within "set itarget [get_node_info -name [get_ clock_info -target \$iclk_name]]" invoked from within "foreach_in_collection iclk_name [get_ clocks] { set itarget [get_node_info -name [get_clock_info -target \$iclk_name]] lappend target_..." ("foreach" body line 137) ... Error: An error occurred during placement and routing</pre> <p>This issue is reported when your design:</p> <ol style="list-style-type: none"> 1. Includes the LVDS SERDES IP Core, and 2. Includes a create_clock setting without a target (for example, a virtual clock) <p>These warning and error messages occur because the Synopsys Design Constraints (SDC) expect a clock setting to have a target; if there is no target the SDC issues an error causing the Fitter to issue the subsequent warning and error message.</p>	<p>To workaroud this issue:</p> <ol style="list-style-type: none"> 1. Locate the SDC file in the LVDS SERDES IP Core; in your project directory, navigate to <code><lvds_module_name>/altera_lvds_core20_140/synth/*.sdc</code>, or locate the file using the <code><lvds_module_name>.qip</code> file 2. Locate the following line in the SDC file: <code>set itarget [get_node_info -name [get_clock_info -target \$iclk_name]]</code> 3. Edit the line to: <code>if { [catch { [get_node_info -name [get_clock_info -target \$iclk_name]] } itarget] } { continue }</code> <p>Rerun the Fitter</p>

Information about known software issues is available on the Quartus II Software Support webpage at the following URL: <http://www.altera.com/support/software/sof-quartus.html>

You can find known issue information for previous versions of the Quartus II software on the Altera Knowledge Database webpage at the following URL: <http://www.altera.com/support/kdb/kdb-index.jsp>

Information about issues affecting the Altera IP Library is available in the *Altera IP Release Notes* at the following URL: http://www.altera.com/literature/rn/rn_ip.pdf

Document Revision History

Table 12: Quartus II Software Release Version 14.0 Arria 10 Edition Document Revision History

Date	Version	Changes
September 2014	Arria 10 Edition 14.0.1	Updated the Simulation Tools table to indicate the Cadence Incisive Enterprise Simulator (IES) is only supported on the Linux platform.
August 2014	Arria 10 Edition 14.0.0	Initial release.