STRATIX V FPGA FEATURES

PRODUCT LINE		STRATIX V GS FPGAs[1]					STRATIX V GX FPGAs[1]										STRATIX V E FPGAs[1]	
		5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6	5SGXB9	5SGXBB	5SEE9	5SEEB
Resources	LEs (K)	236	360	457	583	695	340	420	490	622	840	952	490	597	840	952	840	952
	ALMs	89,000	135,840	172,600	220,000	262,400	128,300	158,500	185,000	234,720	317,000	359,200	185,000	225,400	317,000	359,200	317,000	359,200
	Registers	356,000	543,360	690,400	880,000	1,049,600	513,200	634,000	740,000	938,880	1,268,000	1,436,800	740,000	901,600	1,268,000	1,436,800	1,268,000	1,436,800
	M20K memory blocks	688	957	2,014	2,320	2,567	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660	2,640	2,640	2,640	2,640
	M20K memory (Mb)	13	19	39	45	50	19	37	45	50	52	52	41	52	52	52	52	52
	MLAB memory (Mb)	2.72	4.15	5.27	6.71	8.01	3.92	4.84	5.65	7.16	9.67	10.96	5.65	6.88	9.67	10.96	9.67	10.96
	Variable-precision DSP blocks	600	1,044	1,590	1,775	1,963	256	256	256	256	352	352	399	399	352	352	352	352
	18 x 18 multipliers	1,200	2,088	3,180	3,550	3,926	512	512	512	512	704	704	798	798	704	704	704	704
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
	Regional clocks	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92	92
	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]																
	I/O standards supported	LVTTL, LVCMOS, PCI*, PCI-X, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12																
	LVDS channels, 1.4 Gbps (receive/transmit)	108	174	174	210	210	174	174	210	210	210	210	150	150	150	150	210	210
	Transceiver count (14.1 Gbps)	24	36	36	48	48	36	36	48	48	48	48	66	66	66	66	–	–
	Transceiver count (28.05 Gbps)	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	PCI Express hardened IP blocks (Gen3 x8)	1	1	1	4	4	2	2	4	4	4	4	4	4	4	4	–	–
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3																
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count																		
F780 pin (29 mm, 1.0 mm pitch)		360, 90, 12[3]	360, 90, 12[3]	–	–	–	360, 90, 12[3]	–	–	–	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		432, 108, 24	432, 108, 24	552, 138, 24	–	–	432, 108, 24	552, 138, 24	552, 138, 24	552, 138, 24	–	–	–	–	–	–	–	–
F1152 pin (35 mm, 1.0 mm pitch)		–	–	–	–	–	432, 108, 36	432, 108, 36	432, 108, 36	432, 108, 36	–	–	–	–	–	–	–	–
F1517 pin (40 mm, 1.0 mm pitch)		–	696, 174, 36	696, 174, 36	696, 174 ,36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36[4]	696, 174, 36[4]	432, 108, 66	432, 108, 66	–	–	696, 174, 0[4]	696, 174, 0[4]
F1517 pin (40 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	600,150,48	600,150,48	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	–	–	–	600, 150, 66	600, 150, 66	600, 150, 66[4]	600, 150, 66[4]	–	–
F1932 pin (45 mm, 1.0 mm pitch)		–	–	–	840,210,48	840,210,48	–	–	840, 210, 48	840, 210, 48	840, 210, 48	840, 210, 48	–	–	–	–	840, 210, 0	840, 210, 0

Notes:

1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.
2. 3.3 V compliant, requires a 3.0 V power supply.
3. Hybrid package (flip chip) FBGA: 33 x 33 (mm) 1.0-mm pitch.
4. Hybrid package (flip chip) FBGA: 45 x 45 (mm) 1.0-mm pitch.
5. 360, 90, 12 Numbers indicate GPIO count, LVDS count, and transceiver count.
6. Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.
7. Stratix series devices are offered for commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered for industrial temperatures (0 ˚C to 100 ˚C).