



OIF Serial Framer Level 5 (SFI-5) IP Core

40G systems are being introduced into the marketplace, as carriers begin to deploy higher bandwidth. To this end, the Optical Internetworking Forum (OIF) has specified a 17 lane interface for 40G that is data agnostic for a variety of applications. The goal of this interface is to support converged data at 40G with FEC overhead, and robust functionality as required in this high speed environment.

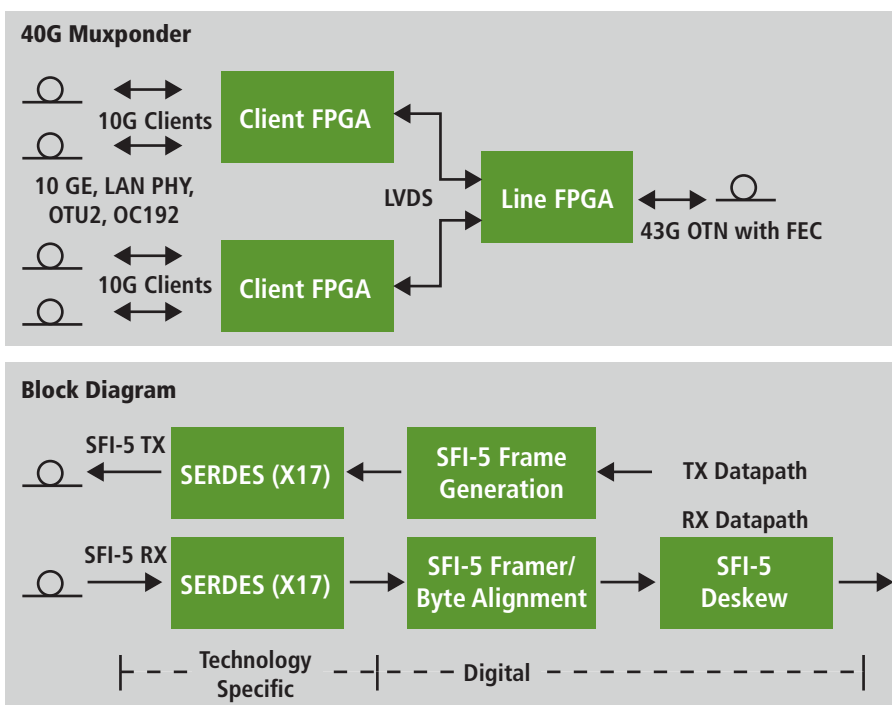
General Features

- OIF SFI-5 compliance
- Verilog HDL RTL
- Exceeds OIF skew standards: up to 16 bits of deskew
- Supports up to 56 Gbps data rates
- Each lane reports its current skew position
- Individual Lane Out of Alignment (OOA) alarms
- Per lane PRBS for integrity checking
- Support for Altera Stratix II GX devices
- Easy to interface, only datapath and clock must connect system
- High Speed (256 bit - up to 200 MHz)

Key Features

- Hardware tested with leading industry 40 Gbps optical transceivers
- Can be used with Altera's Enhanced FEC or G.709 FEC
- Patent Pending design to beat FPGA Skew Injection

40G Muxponder Application



Standard Data Rates Supported

- OTN OTU-3
- SONET OC-768
- SDH STM-256

Product Overview

This document details the Altera SFI-5 IP core. The SFI-5 IP core is a 17 lane interface with 16 data lanes and 1 parity lane, with each lane running at 2.5G – 3.125G.

The clock and data is recovered from the individual data and parity lanes from the SERDES interface. The data is subsequently retimed to the system clock for framing and deskew.

The datapath runs at 155-200 MHz, at a data width of 256 bits. This width can be changed to accommodate other system interface speeds.

By using the Altera SFI-5 IP core, you can leverage system expertise to ensure competitive differentiation without the burden of designing a standard interface.

The SFI-5 core supports a line rate of 43.018 Gbps and can be over-clocked to support higher data rates. A dual-SFI-5 core for example can be used for 100G style applications.

Customization and Support

Leveraging Altera's extensive IP library, you can build a complete Field Programmable Standard Product (FPSP) – a complete FPGA-based solution developed to a custom functional specification. By making use of hardware validated IP cores, Altera can deliver a custom, validated, IP solution at lightning speed.

In addition to product customization, Altera can provide any necessary software drivers to support our products.

Related Products

For additional information regarding Altera FPGA products and NTC OTN IP Products visit www.altera.com.

Want to Dig Deeper?

For more information about Altera's OIF Serial Framer Level 5 (SFI-5) IP Core, please contact your Altera sales representative or FAE, or visit www.altera.com.

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