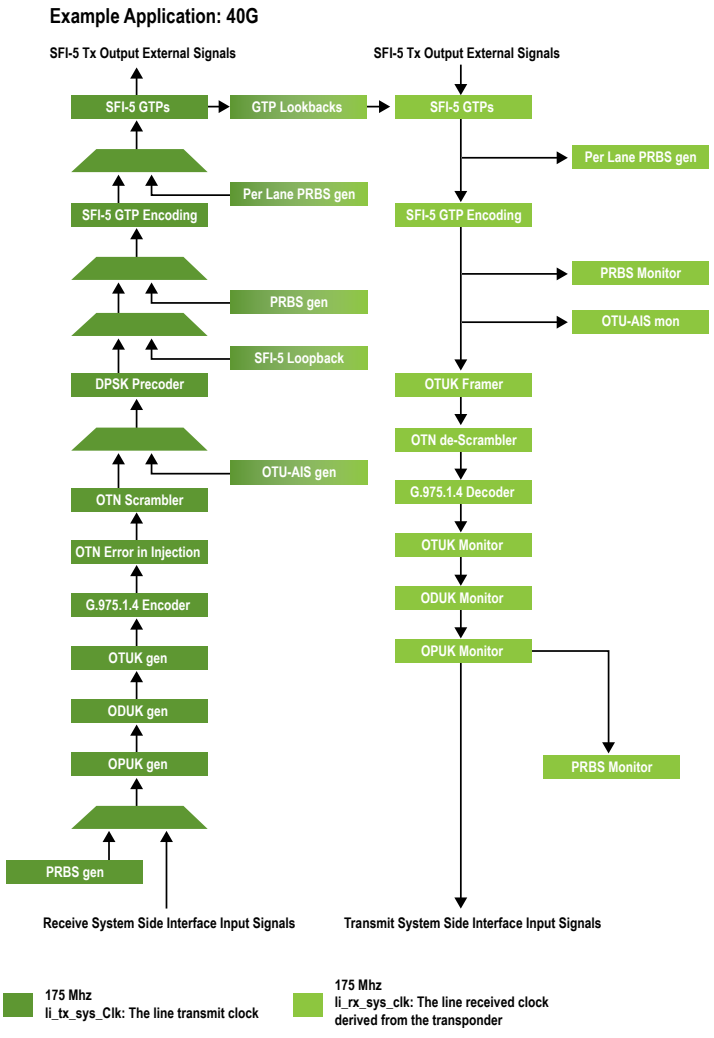
# BCH/RS FEC IP Core

## General Features

- Compliant with G.975.1 Annex 4
- 8.56dB net coding gain at 10-15 output BER
- 10G or 40G rates and variable rates in between
- Generic CPU interface for control and monitoring

## Application Diagrams




## Key Features

- Enables replacement of 1.4 ASSPs
- Support for ASIC and FPGA implementation

## Statistics:

- corrected bits
- corrected ones
- corrected zeros
- corrected codes
- corrected blocks
- uncorrectable codes

## Related Products

For additional information regarding Altera OTN IP products visit **www.altera.com**.

## Want to Dig Deeper?

For more information about this IP core, please contact your Altera® sales representative or FAE, or visit **www.altera.com**.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