15. Avalon-ST Multi-Channel Shared Memory FIFO Core

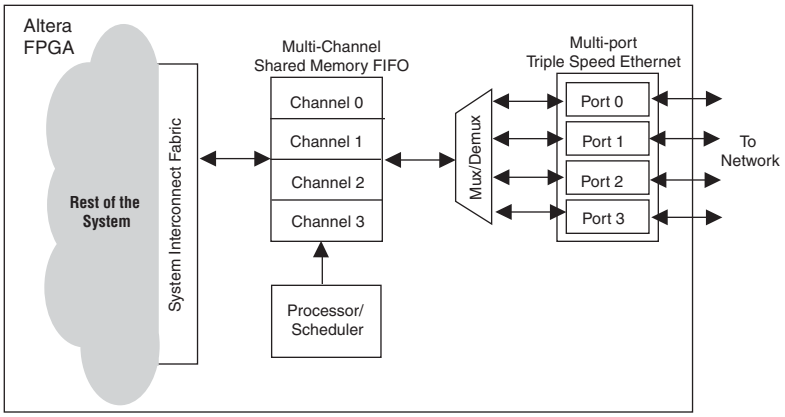
QII55015-9.1.0

Core Overview

The Avalon® Streaming (Avalon-ST) Multi-Channel Shared Memory FIFO core is a FIFO buffer with Avalon-ST data interfaces. The core, which supports up to 16 channels, is a contiguous memory space with dedicated segments of memory allocated for each channel. Data is delivered to the output interface in the same order it was received on the input interface for a given channel.

Figure 15–1 shows an example of how the core is used in a system. In this example, the core is used to buffer data going into and coming from a four-port Triple Speed Ethernet MegaCore function. A processor, if used, can request data for a particular channel to be delivered to the Triple Speed Ethernet MegaCore function.

Figure 15–1. Multi-Channel Shared Memory FIFO in a System—An Example



The Avalon-ST Multi-Channel Shared FIFO core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated systems.

This chapter contains the following sections:

Performance and Resource Utilization

This section lists the resource utilization and performance data for various Altera device families. The estimates are obtained by compiling the core using the Quartus® II software.

Table 15–1 shows the resource utilization and performance data for a Stratix II GX device (EP2SGX130GF1508I4).

Table 15–1. Memory Utilization and Performance Data for Stratix II GX Devices

Channels	ALUTs	Logic Registers	Memory Blocks			f_{MAX} (MHz)
			M512	M4K	M-RAM	
4	559	382	0	0	1	> 125
12	1617	1028	0	0	6	> 125

Table 15–2 shows the resource utilization and performance data for a Stratix III device (EP3SL340F1760C3). The performance of the MegaCore function in Stratix IV devices is similar to Stratix III devices.

Table 15–2. Memory Utilization and Performance Data for Stratix III Devices

Channels	ALUTs	Logic Registers	Memory Blocks			f_{MAX} (MHz)
			M9K	M144K	MLAB	
4	557	345	37	0	0	> 125
12	1741	1028	0	24	0	> 125

Table 15–3 shows the resource utilization and performance data for a Cyclone III device (EP3C120F780I7).

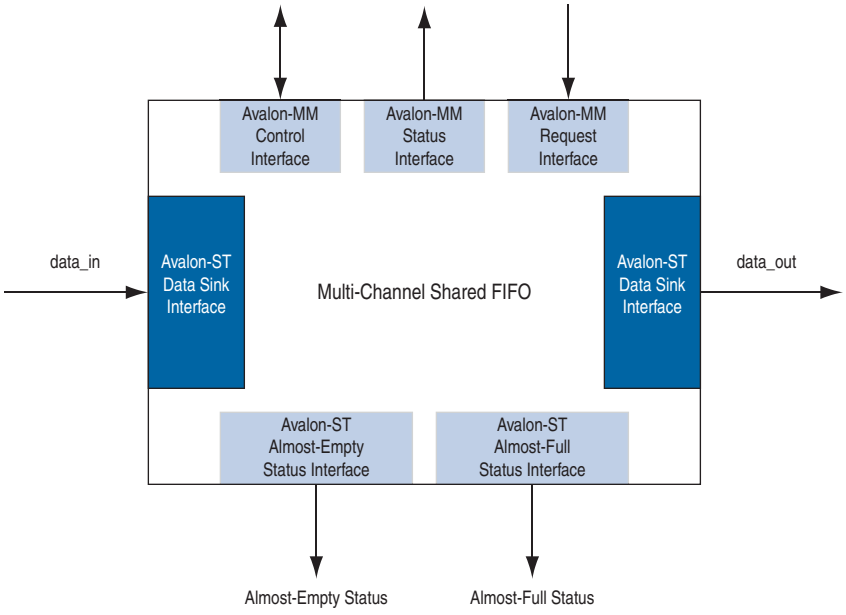
Table 15–3. Memory Utilization and Performance Data for Cyclone III Devices

Channels	Total Logic Elements	Total Registers	Memory M9K	f_{MAX} (MHz)
4	711	346	37	> 125
12	2284	1029	412	> 125

Functional Description

Figure 15–2 shows a block diagram of the Avalon-ST Multi-Channel Shared FIFO core.

Figure 15–2. Avalon-ST Multi-Channel Shared Memory FIFO Core



Interfaces

This section describes the core's interfaces.

Avalon-ST Interfaces

The core includes Avalon-ST interfaces for transferring data and almost-full status.

Table 15–4 shows the properties of the Avalon-ST data interfaces.

Table 15–4. Properties of Avalon-ST Interfaces

Feature	Property	
	Data Interfaces	**Status Interfaces**
Backpressure	Ready latency = 0.	Not supported.
Data Width	Configurable.	Data width = 2 bits. Symbols per beat = 1.
Channel	Supported, up to 16 channels.	Supported, up to 16 channels.
Error	Configurable.	Not used.
Packet	Supported.	Not supported.

Avalon-MM Interfaces

The core can have up to three Avalon-MM interfaces:

- **Avalon-MM control interface**—Allows master peripherals to set and access almost-full and almost-empty thresholds. The same set of thresholds is used by all channels.
- **Avalon-MM status interface**—Provides the FIFO fill level for a given channel. The FIFO fill level represents the amount of data in the FIFO at any given time. The fill level is available on the `readdata` bus one clock cycle after the read request is received.
- **Avalon-MM request interface**—Allows master peripherals to request data for a given channel. This interface is implemented only when the parameter **Use Request** is set to 1. The `request_address` signal contains the channel number. Only one FIFO entry is returned for each request.

For more information about Avalon interfaces, refer to the *Avalon Interface Specifications*.

Operation

The Avalon-ST Multi-Channel Shared FIFO core allocates dedicated memory segments within the FIFO for each channel, and is implemented such that the memory segments occupy a single memory block. The depth of each memory segment is determined by the parameter **FIFO depth**. If the core is configured to support more than one channel, the Avalon-MM request interface must be implemented to allow master peripherals to request data for a specific channel. Otherwise, only channel 0 is accessible.

When a request is received on the core's Avalon-MM request interface, the requested data is available on the Avalon-ST data source interface after three clock cycles. Only one word of data can be requested at a time. The core delivers the data to the Avalon-ST data source interface after a full packet is received.

The core does not implement any mechanism to accept incoming requests while processing. Once the core starts processing a request, incoming requests are dropped until the current one completes and data is transferred to the requesting component. Packets received on the Avalon-ST sink interface are dropped if the error signal is asserted.

You can configure almost-full thresholds to manage FIFO overflow. The current threshold status for each channel is available from the core's Avalon-ST status interfaces in a round-robin fashion. For example, if the threshold status for channel 0 is available on the interface in clock cycle *n*, the threshold status for channel 1 is available in clock cycle *n+1* and so forth.

Instantiating the Core in SOPC Builder

Use the MegaWizard™ interface for the Avalon-ST Multi-Channel Shared FIFO core in SOPC Builder to add the core to a system.

Table 15–5 lists and describes the parameters you can configure.

Table 15–5. Configurable Parameters

Parameter	Legal Values	Description
Number of channels	1, 2, 4, 8, and 16	The total number of channels supported on the Avalon-ST data interfaces.
Symbols per beat	1–32	The number of symbols transferred in a beat on the Avalon-ST data interfaces
Bits per symbol	1–32	The symbol width in bits on the Avalon-ST data interfaces.
Error width	0–32	The width of the `error` signal on the Avalon-ST data interfaces.
FIFO depth	2–2^{32}	The depth of each memory segment allocated for a channel. The value must be a multiple of 2.
Use request	0 or 1	Setting this parameter to 1 implements the Avalon-MM request interface. If the request interface is disabled, only channel 0 can be used.
Address width	1–32	The width of the FIFO address. This parameter is determined by the parameter **FIFO depth**; **FIFO depth** = $2^{\text{Address Width}}$.

Device Support

The Avalon-ST Multi-Channel Shared FIFO core supports all Altera device families.

Software Programming Model

The following sections describe the software programming model for the Avalon-ST Multi-Channel Shared FIFO core.

HAL System Library Support

The Altera-provided driver implements a HAL device driver that integrates into the HAL system library for Nios II systems. HAL users should access the Avalon-ST Multi-Channel Shared FIFO core via the familiar HAL API and the ANSI C standard library.

Register Map

You can update and access the FIFO thresholds via the Avalon-MM control interface. Table 15–6 shows the register map for the control interface.

Table 15–6. Control Interface Register Map

Offset	Name	Access	Description
Base + 0	`Almost_Full_Threshold`	RW	The value of the primary almost-full threshold. The bit `Almost_full_data[0]` on the Avalon-ST almost-full status interface is set to 1 when the FIFO level is greater than or equal to this threshold.
Base + 8	`Almost_Full2_Threshold`	RW	The value of the secondary almost-full threshold. The bit `Almost_full_data[1]` on the Avalon-ST almost-full status interface is set to 1 when the FIFO level is greater than or equal to this threshold.

Referenced Documents

This chapter references *Avalon Interface Specifications*.

Document Revision History

Table 15–7 shows the revision history for this chapter.

Table 15–7. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009 v9.1.0	No change from previous release.	—
March 2009 v9.0.0	No change from previous release.	—
November 2008 v8.1.0	Changed to 8-1/2 x 11 page size. No change to content.	—
May 2008 v8.0.0	Initial release.	—