FIR Compiler

This document addresses known errata and documentation issues for the Altera® FIR Compiler, v7.1. Errata are functional defects or errors, which may cause an Altera FIR Compiler MegaCore® function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the FIR Compiler v7.1.

Table 1. FIR Compiler v7.1 Issues

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For existing up-to-date errata, refer to the *FIR Compiler, v7.1 Errata Sheet* on the Errata Sheets page of the Altera literature website.

FIR Compiler v7.1 Issues

Altera has identified the following issues that affect the FIR Compiler, v7.1.

coef_in Bit Width Incorrect When Using Manual Scaling

For a reloadable coefficient FIR filter when the Coefficients Scaling type is set to `Manual`, the coefficient bit width calculations are incorrect.

Affected Configurations

This issue affects all reloadable coefficient filters with manual coefficient scaling.

Design Impact

The simulation model generation and Quartus II compilation fails. The incorrect bit width can be observed from the output bit width displayed in the GUI.

Workaround

Avoid selecting manual coefficient scaling for reloadable coefficient filters. If you need to use manual scaling, then you can do the following:

- **If you want to load your own set of coefficients**: Scale them before you load them into the FIR Compiler. Then set the Coefficients Scaling to None in the main Parameterization window. You will notice that the output bit width displayed in the GUI has changed. The simulation model will also generate successfully.
- **If you want to generate the filter coefficients using the coefficient generator**: First design a filter with fixed coefficients. Set the manual scaling factor as you require, then generate this filter. The coefficient set is written to a file *<your_fir_filter>*_**coef_int.txt**. Restart the FIR compiler to edit your filter parameters but this time, go to the Edit Coefficient Set page, and instead of generating the coefficients, choose to import the *<your_fir_filter>*_**coef_int.txt** file. Load this file and change the Coefficients Scaling type to None in the main Parameterization window. You will notice that the output bit width displayed in the GUI has changed. The simulation model will also generate successfully.

Solution Status

This issue will be fixed a future release of the FIR Compiler.

Reloadable Coefficient Filters Fail for Some Single Rate Interpolation and Decimation MCV Filters

Reloadable coefficient filters fail for some single rate, interpolation and decimation multicycle variable filters.

Affected Configurations

This error is observed in some of the reloadable coefficient MCV filters when the coefficients are stored in logic cells.

Design Impact

The produced output does not match the expected output.

Workaround

Change the coefficient storage to block memories such as M512, M4K, MLAB, or M9K.

Solution Status

This issue will be fixed a future release of the FIR Compiler.

Error When Preloading Coefficients for HardCopy Devices

Some FIR architectures cannot preload coefficient memories in HardCopy devices.

Affected Configurations

This issue affects configurations targeting HardCopy devices.

Design Impact

Some FIR architectures fail during synthesis when targeting Hardcopy devices.

Workaround

Avoid using pre-initialized memory by selecting data storage and coefficient storage to LEs.

Solution Status

This issue will be fixed a future release of the FIR Compiler.

Signed Binary Fraction Results in Output Bit Width Mismatch

For signed binary fraction data types, some FIR filter variations fail Quartus® II compile and simulation model generation.

Affected Configurations

This issue affects all configurations with signed binary fraction data types.

Design Impact

Compilation fails in the Quartus II software.

Workaround

This problem is related to a user interface problem. In some cases, when you reopen the variation file using IP Toolbench and re-generate the filter the problem is resolved. If it still fails compilation, use one of the other data types (Signed Binary or Unsigned Binary).

Solution Status

This issue will be fixed a future release of the FIR Compiler.

Half-Band Decimator & Symmetric Interpolator Filters Do Not Support Unsigned Data Types

The half-band decimator and symmetric interpolator filters do not support unsigned input data type.

Affected Configurations

This issue affects half-band decimator and symmetric interpolator filter architectures.

Design Impact

The FIR filter produces incorrect results.

Workaround

The half-band decimator and symmetric interpolator filter architectures require signed input data types. To ensure it works with unsigned data, design the filter with input ports 1-bit larger than the original value and connect the MSB bit of the `ast_sink_data` input port to `0`.

Solution Status

This issue will be fixed a future release of the FIR Compiler.

Quartus II Simulation Vector File Not Generated

FIR Compiler v7.1 does not create a vector file for simulation in the Quartus II software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design can be compiled, but there is no automatically generated vector file testbench available to simulate the design in the Quartus II software.

Workaround

Use NativeLink to simulate the VHDL testbench instead.

Solution Status

This issue will be fixed a future release of the FIR Compiler.

Graphical User Interface Freezes

When you choose a **Coefficient Width** of 2 bits and at the same time set the coefficient scaling to **Auto Power of 2**, the graphical user interface (GUI) cannot produce the function and the GUI can freeze.

Affected Configurations

This issue affects FIR Compiler configurations that use the previously mentioned GUI settings.

Design Impact

This issue causes the GUI to freeze.

Workaround

To use a **Coefficient Width** of 2, manually scale the coefficients to the desired range using the manual coefficient scaling option instead of the **Auto Power of 2** option. Alternatively, you can perform the scaling externally and import the coefficients as text file. When importing coefficients, set the coefficient scaling option to **None**.

Solution Status

This issue will be fixed in a future release of the FIR Compiler.

GUI Freezes or Generates Incorrect Multicycle Variable Architectures

The FIR Compiler GUI can freeze or generate incorrect code if you use all of the following GUI settings:

■ The multicycle variable (MCV) architecture
■ A high number of coefficients
■ A low number of bits per coefficient
■ A high number of cycles
■ Turn on coefficient reloading

Affected Configurations

This issue affects FIR Compiler configurations that use the previously mentioned settings.

Design Impact

This issue causes the FIR Compiler GUI to freeze or generate incorrect code.

Workaround

To avoid this problem, you should instantiate separate filters such that each filter uses only a part of the coefficients. Then, combine the results of these filters.

Solution Status

This issue will be fixed in a future release of the FIR Compiler.

Contact Information

For more information, contact Altera's mySupport website at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *FIR Compiler Compiler v7.1 Errata Sheet*.

Table 2. FIR Compiler Compiler v7.1 Errata Sheet Revision History

Version	Date	Errata Summary
1.1	May 2007	Added errata.
1.0	May 2007	New errata sheet for the 7.1 release.

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