Description

Single Event Upset (SEU) is a change of node state in semiconductor devices caused by ions or electro-magnetic radiation striking a substrate. Altera provides a set of tools to detect, classify and minimize the impact of SEU on the system.

SEU reference design demonstrates a methodology and tools available for a designer to improve system immunity and guarantee successful recovery from SEU.

Altera tools include a Fault Injection mechanism that emulates the SEU event striking specific node of the chip. This tool can be used by the designer to test their system for "what-if" scenarios. In this design the error would be injected to a certain logical block, which would correlate the event using SignalTap® II Logic Analyzer.

Once the error is recognized using integrated error detection cyclic redundancy check (EDCRC) verification block, it is then classified as critical/non-critical and indicates the specific design block where the error occurred using a CRC syndrome obtained from the chip.

For additional information, please contact us at *mil@altera.com* or *contact your local Altera sales representative*.

Features

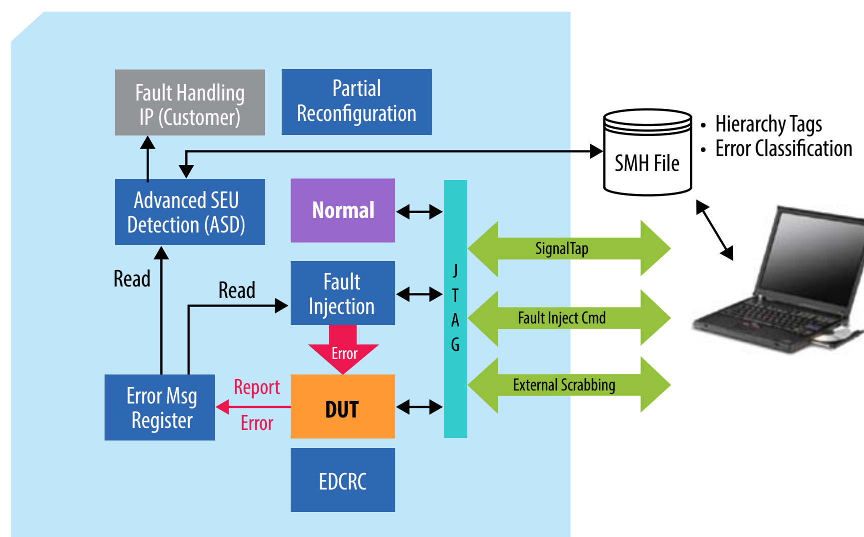
- Advanced SEU Detection IP
- Fault Injection IP
- SEU error classification demonstration
- Error region tagging
- Correction of error – external scrubbing

Applications

- Avionics and Satellites
- Data Center
- Networking Equipment

This information allows the system to react in the most appropriate way to the SEU event that is identified. One of the options is to perform the error correction to the FPGA, in order to recover the FPGA to normal functional state. This is referred as external scrubbing and is demonstrated in this design as well.

Figure 1: SEU Verification and Mitigation Reference Design Block Diagram



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