DSP Development Board

Stratix II Edition

Rev 02

Revision History

Date	Change Description	Rev
10/21/03	Started design	01
2/5/04	Sent out schematic for first design review	01
7/30/04	Started Rev02 changed per document Maine_board_bringup.doc	02

<Core Design>

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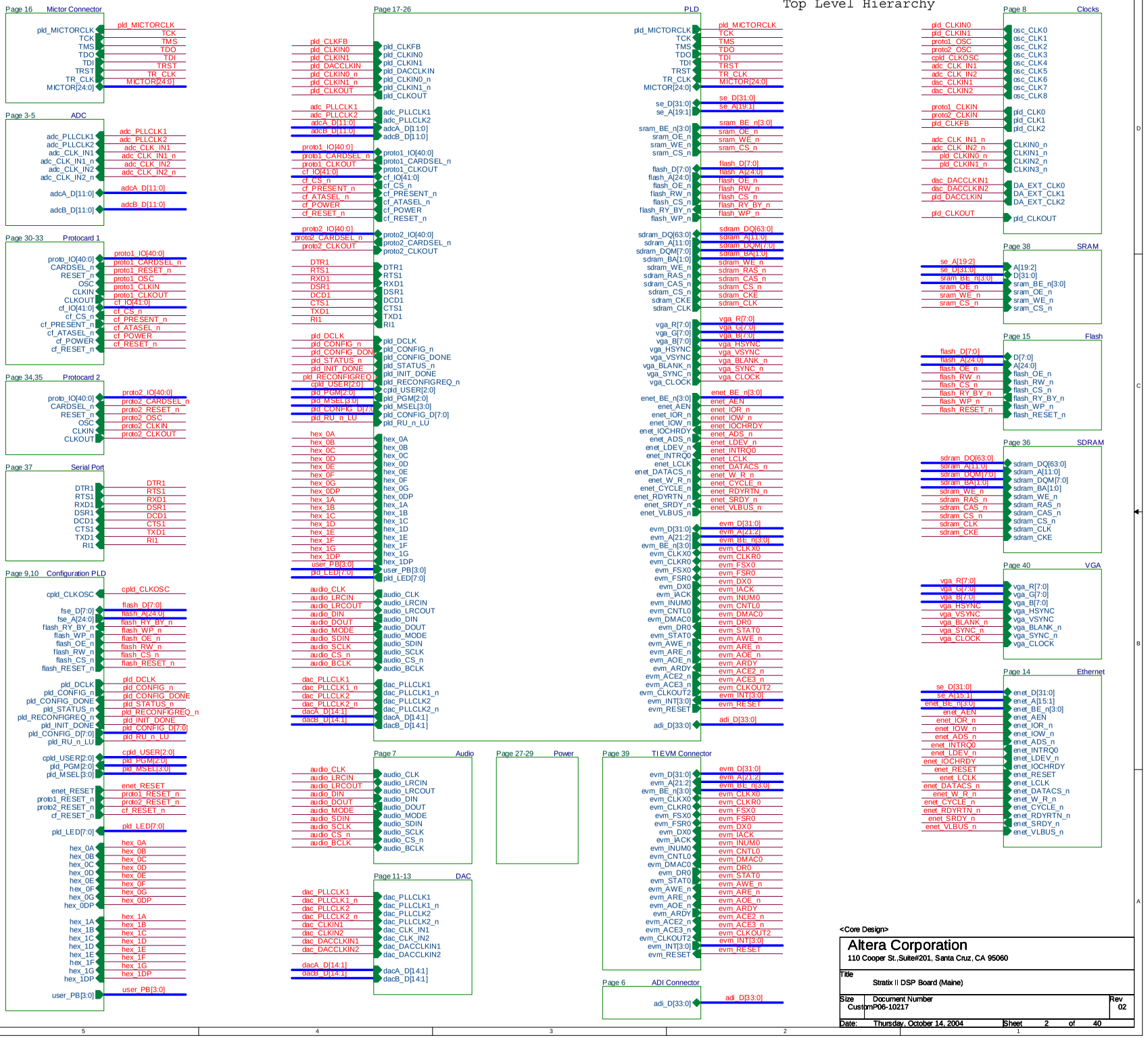
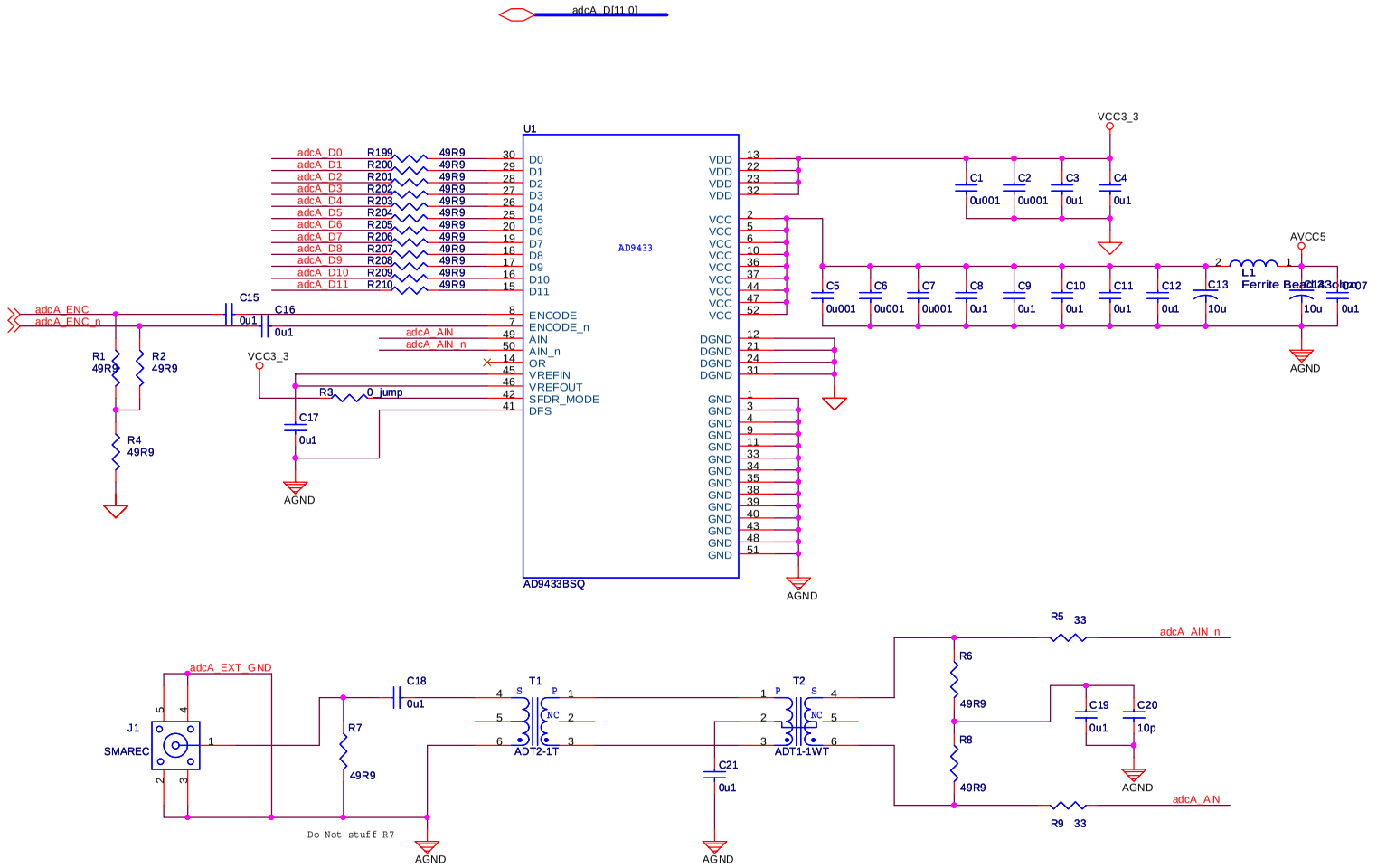
Top Level Hierarchy



ADC A



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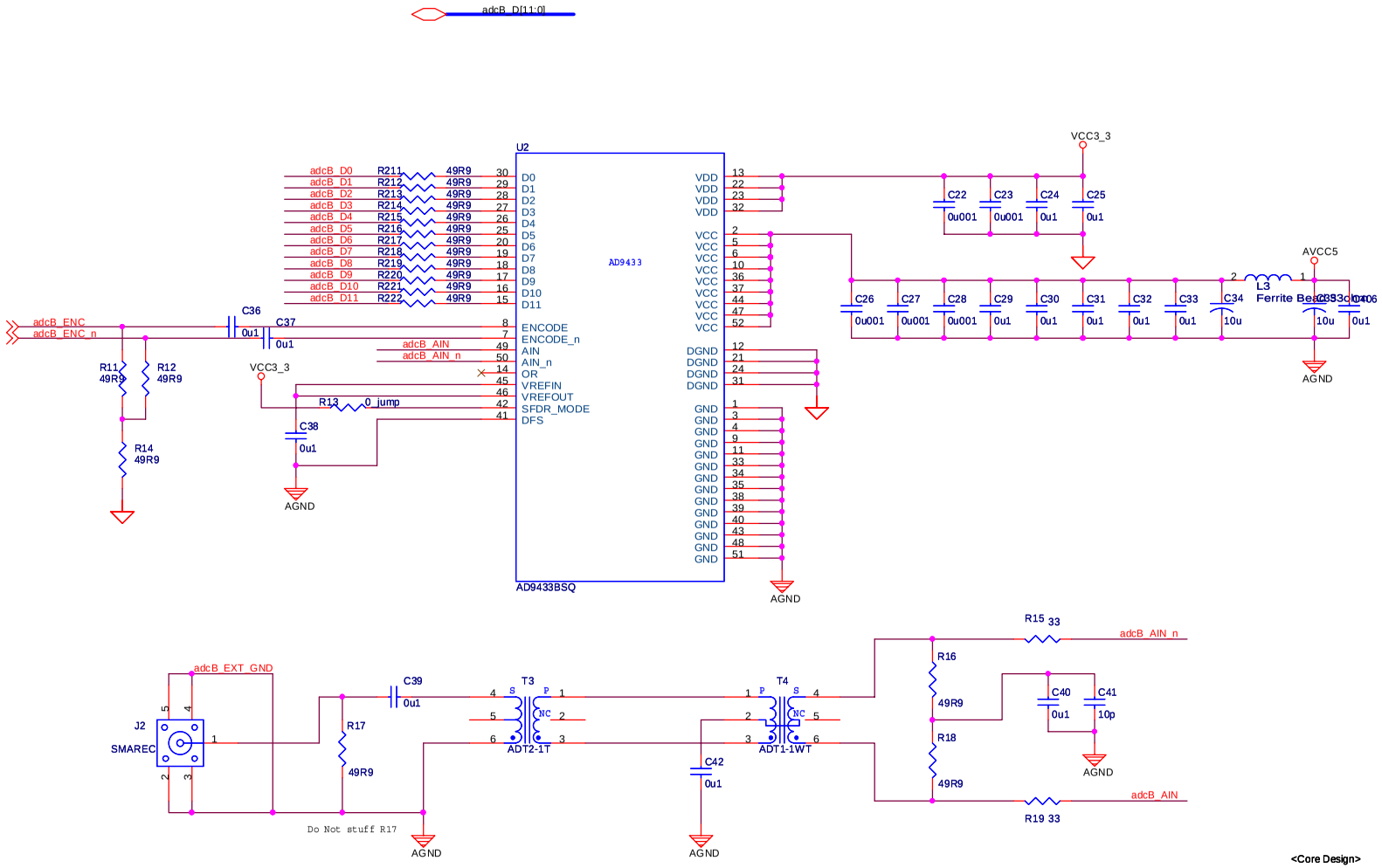
ADC B



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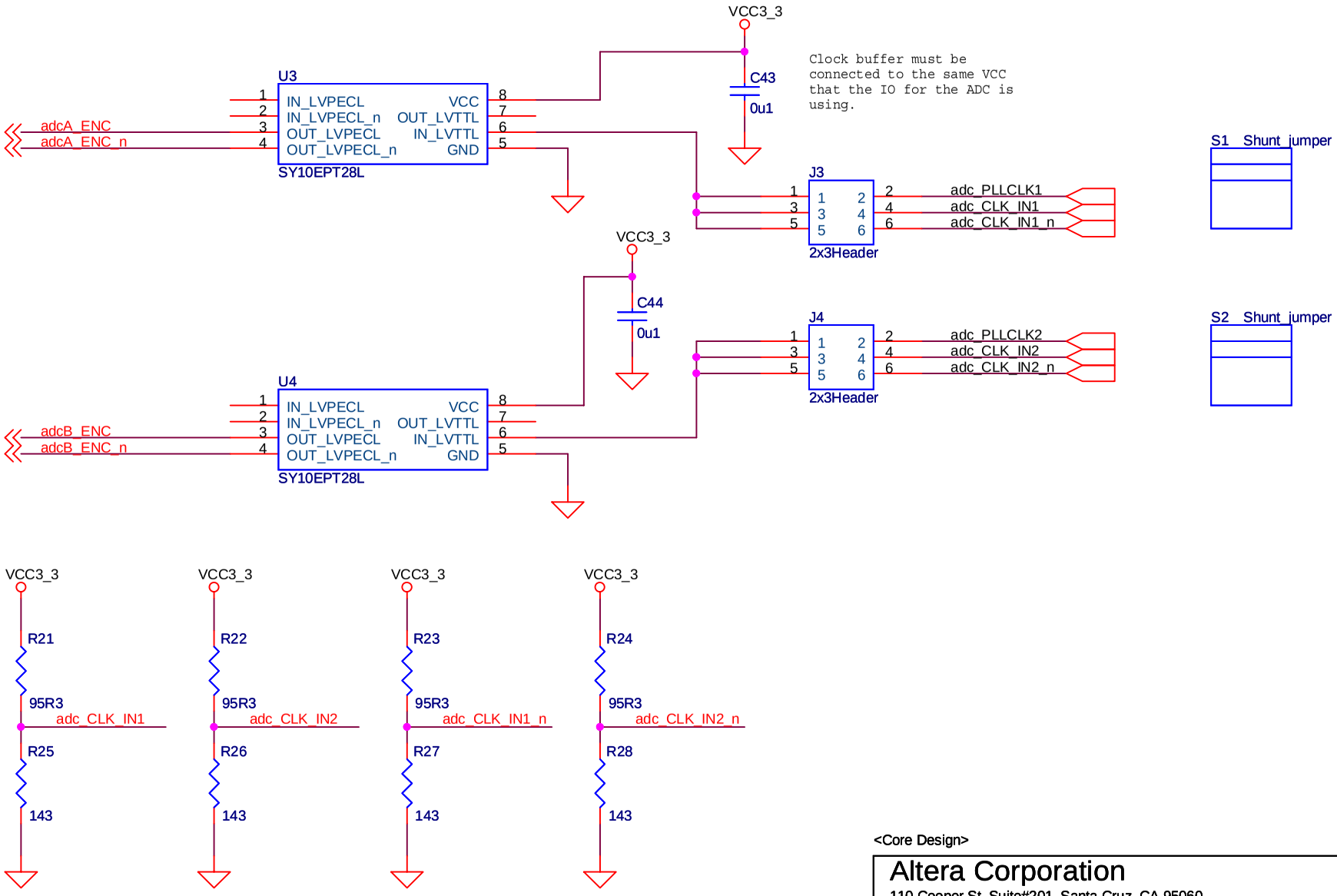
ADC Clock Selection



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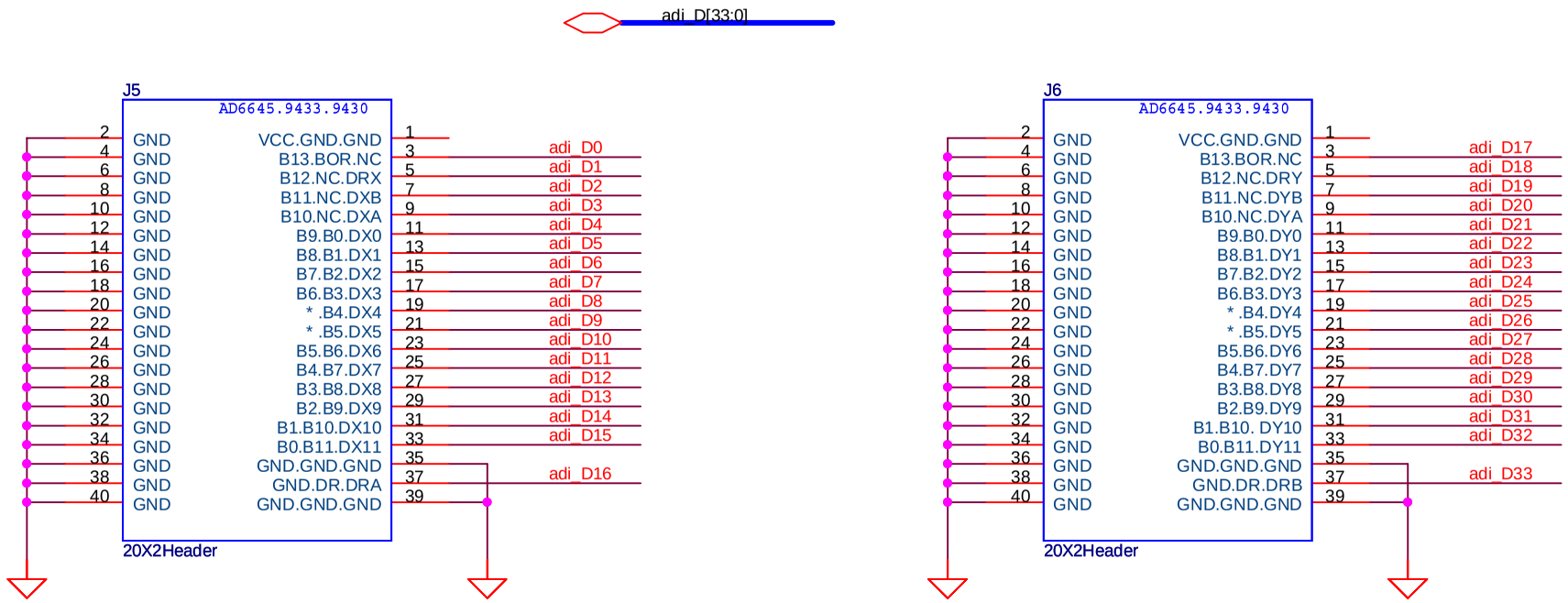
ADI Connector



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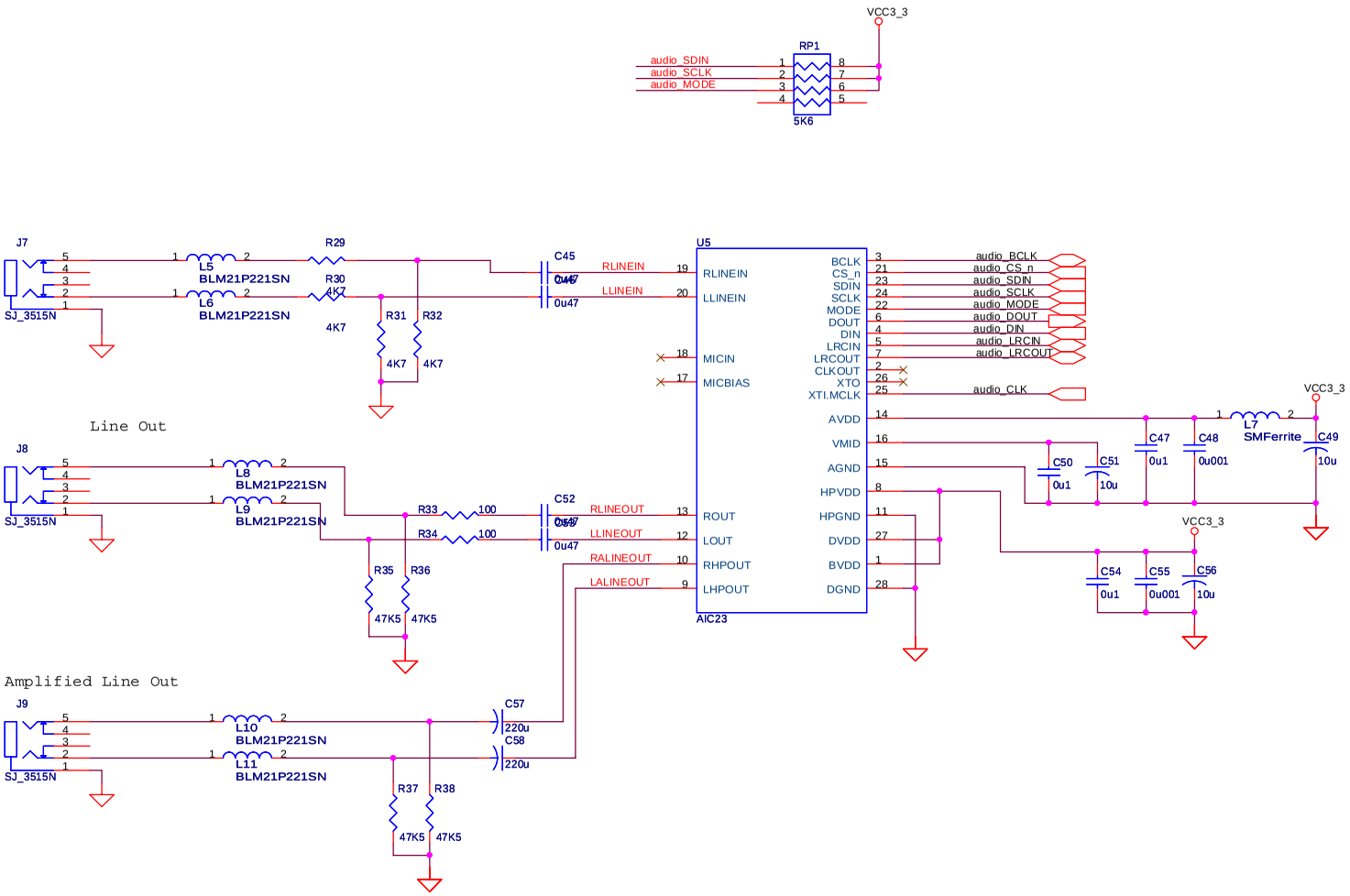
Audio



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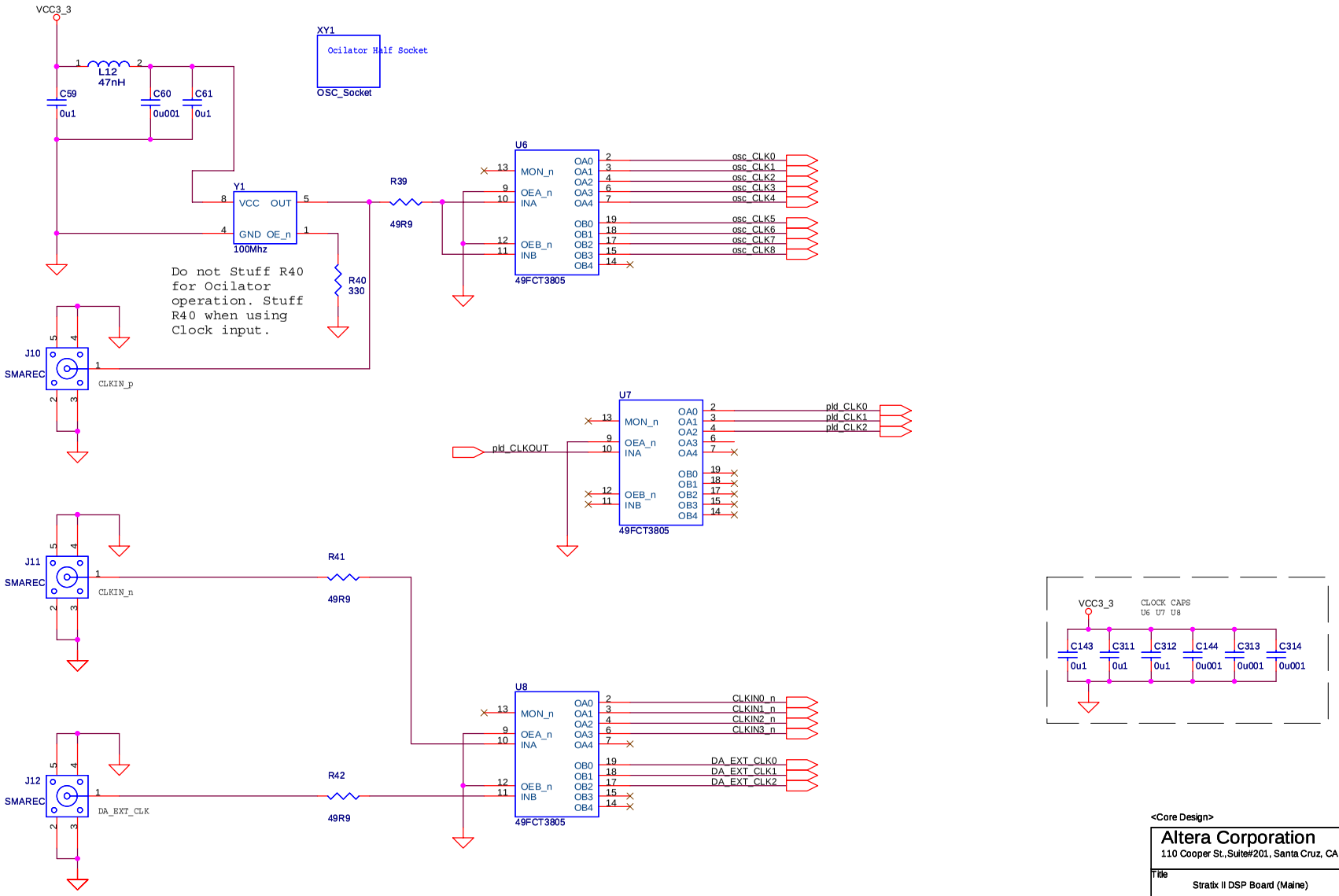
Clocks



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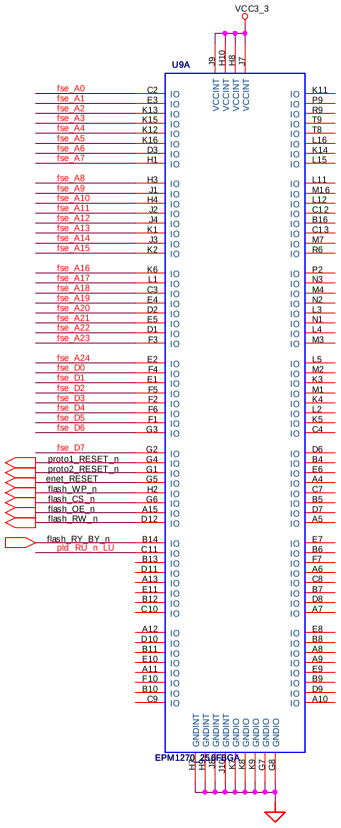
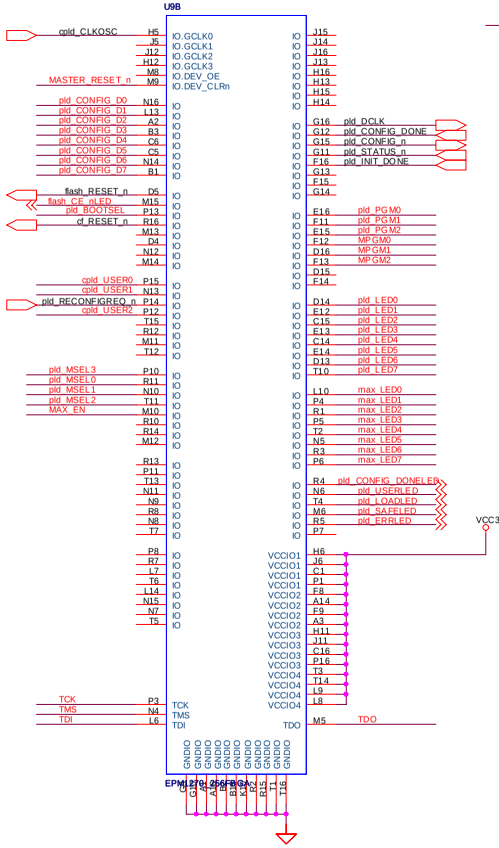
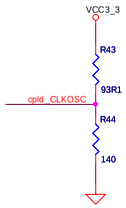
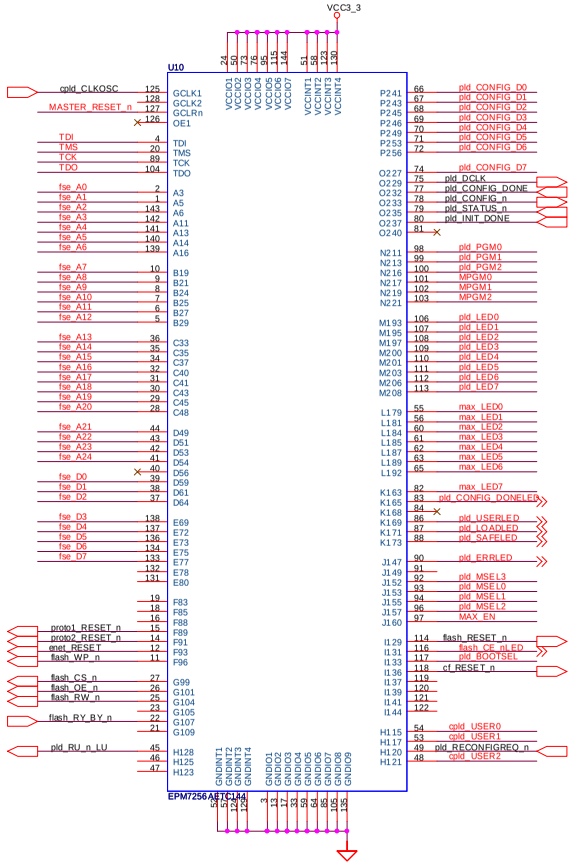
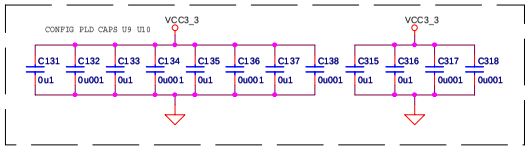
Configuration PLD



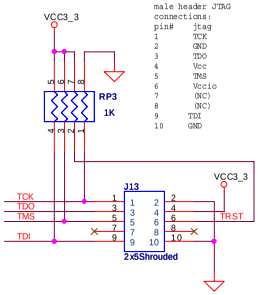


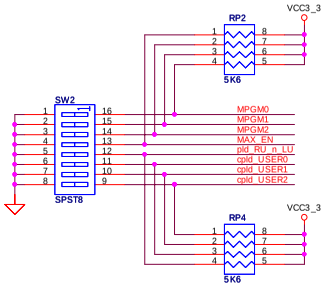




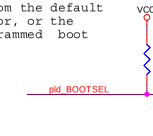


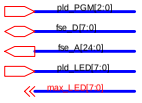
Configuration PLD

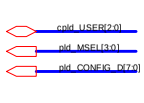




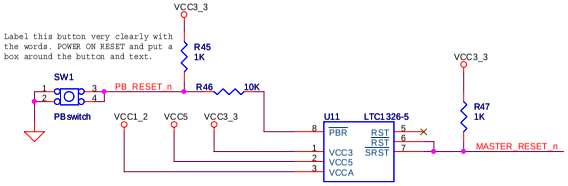
pld_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.







Label this button very clearly with the words. POWER ON RESET and put a box around the button and text.



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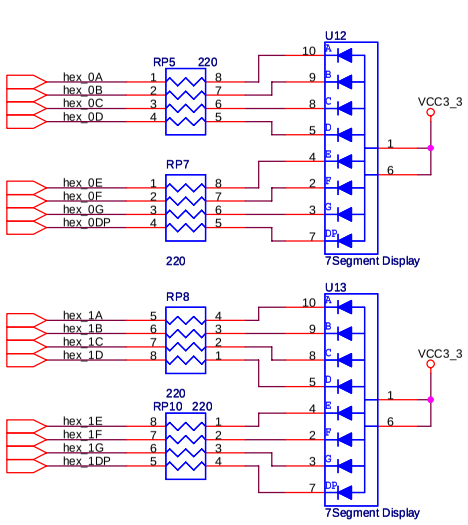
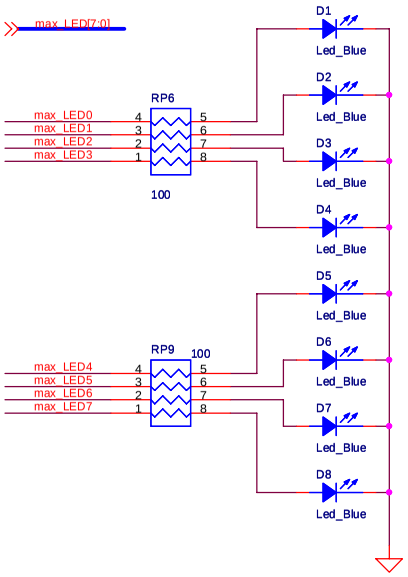
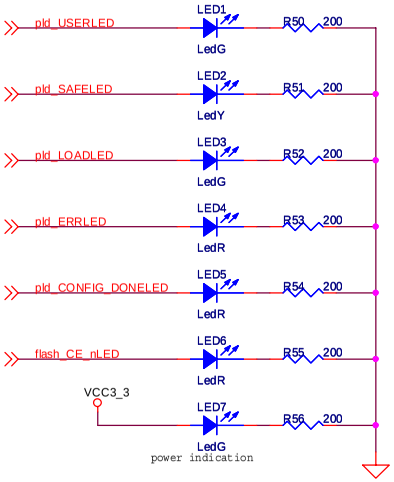
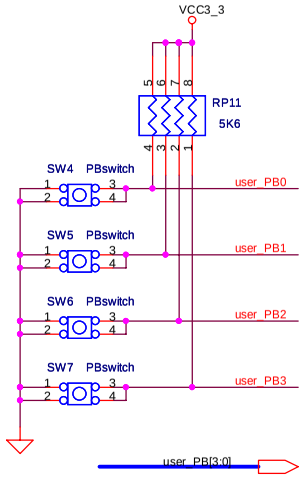
LEDs and Buttons









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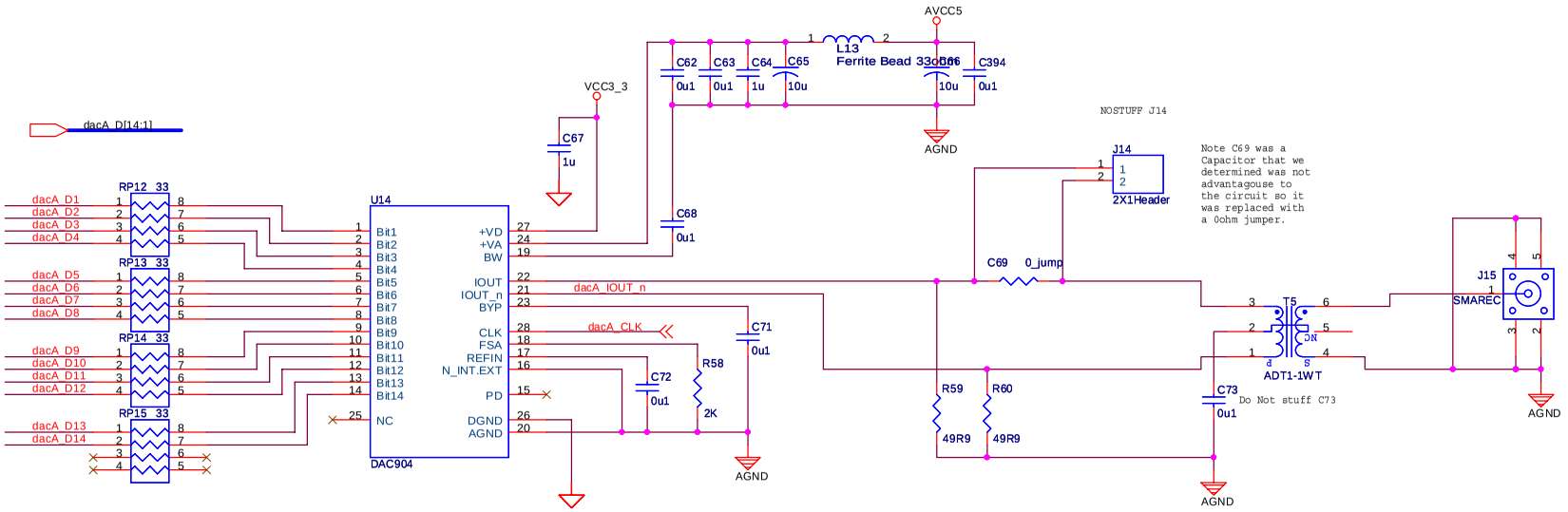
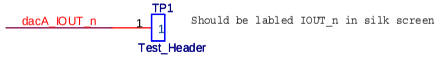
DAC A





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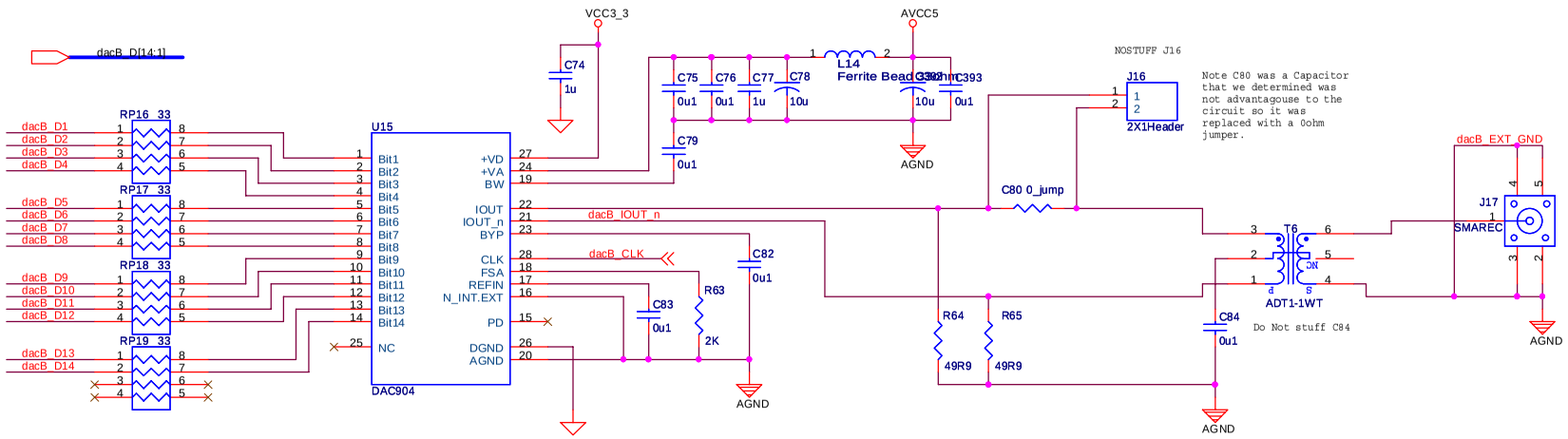
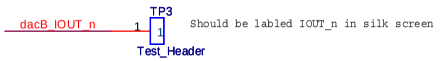
DAC B





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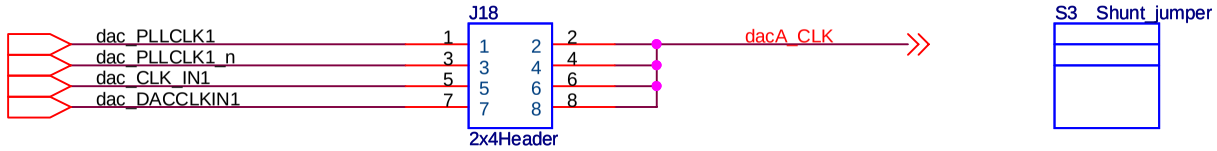
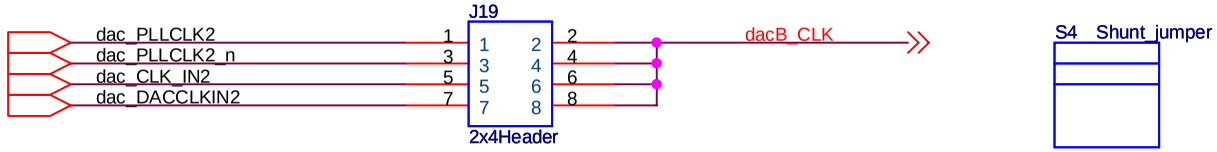
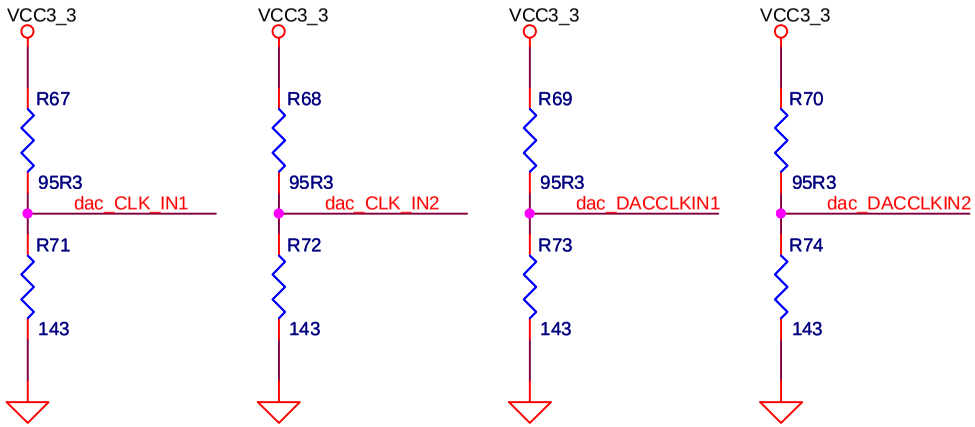
DAC Clock Jumper







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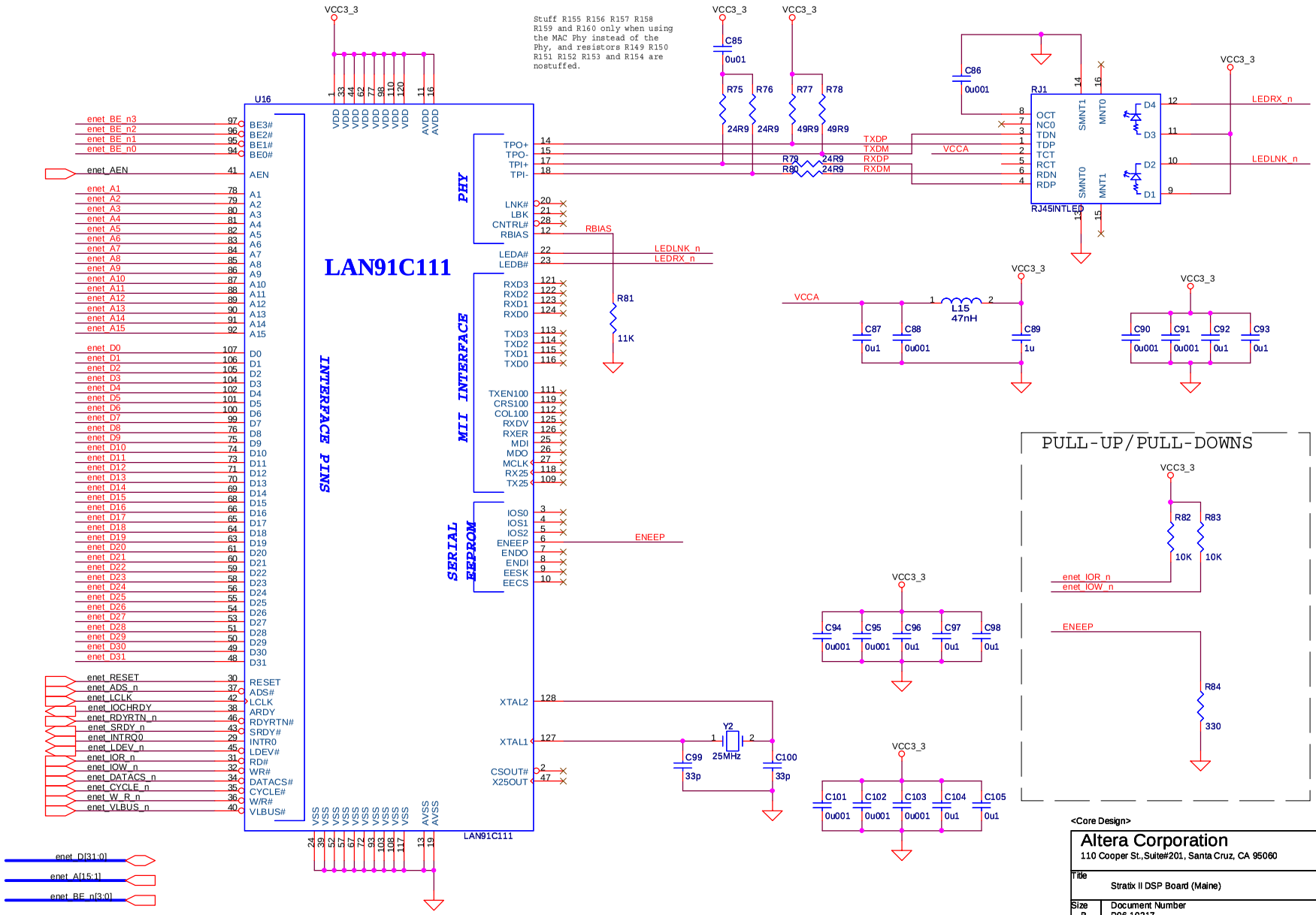
Ethernet
Stuff R155 R156 R157 R158 R159 and R160 only when using the MAC Phy instead of the Phy, and resistors R149 R150 R151 R152 R153 and R154 are nostuffed.
LAN91C111
U16
PHY
MII INTERFACE
SERIAL EEPROM
INTERFACE PINS
RJ45INTLED
PULL-UP/PULL-DOWNS
Y2
25MHz
L15
47nH
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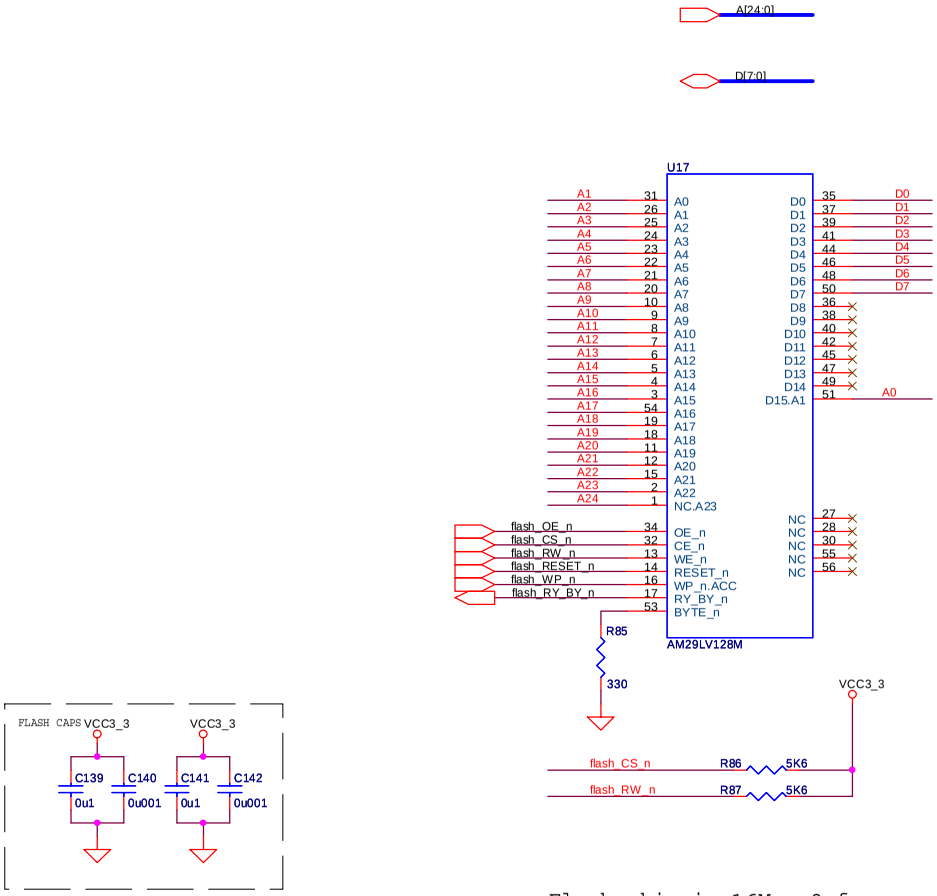

Flash chip is 16M x 8 for
16Mbytes of flash

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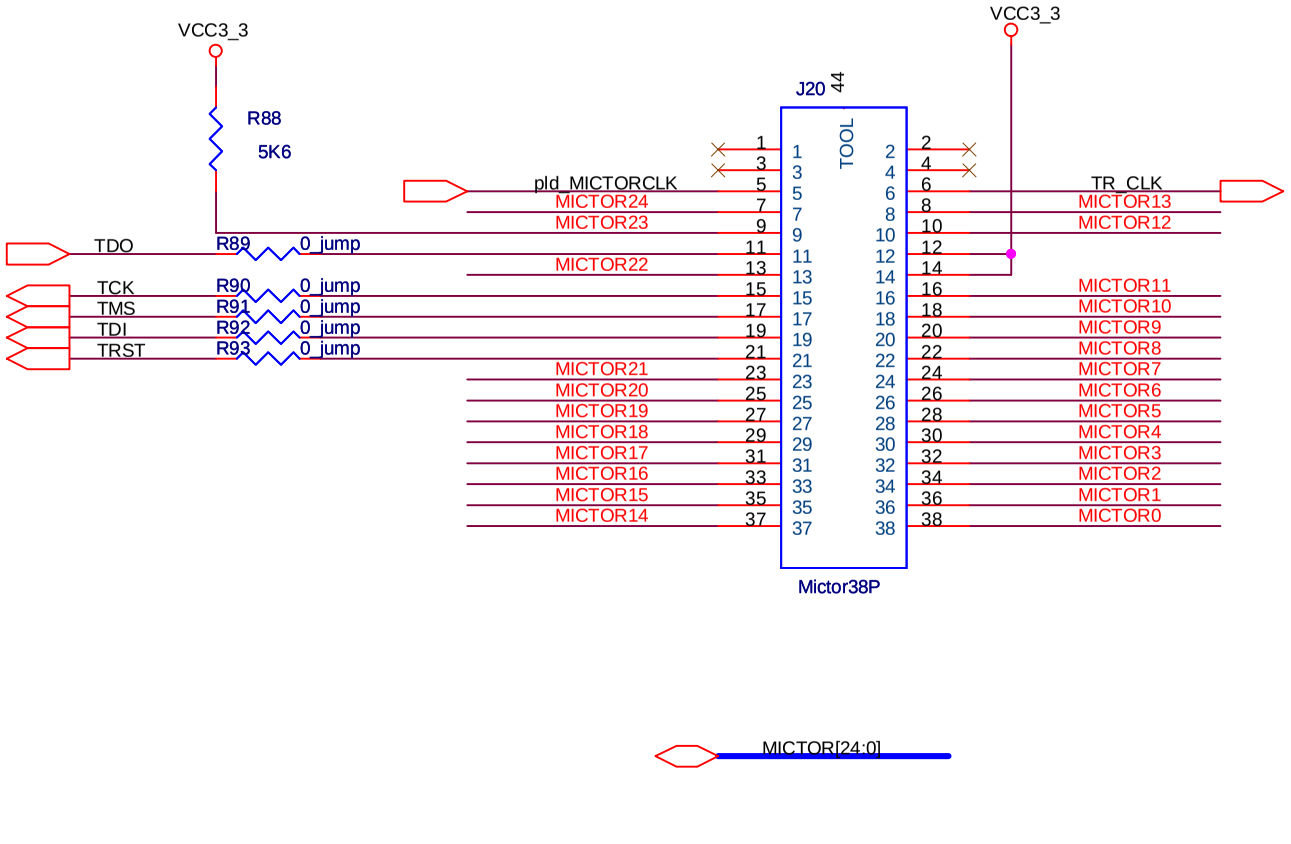
Mictor Connector



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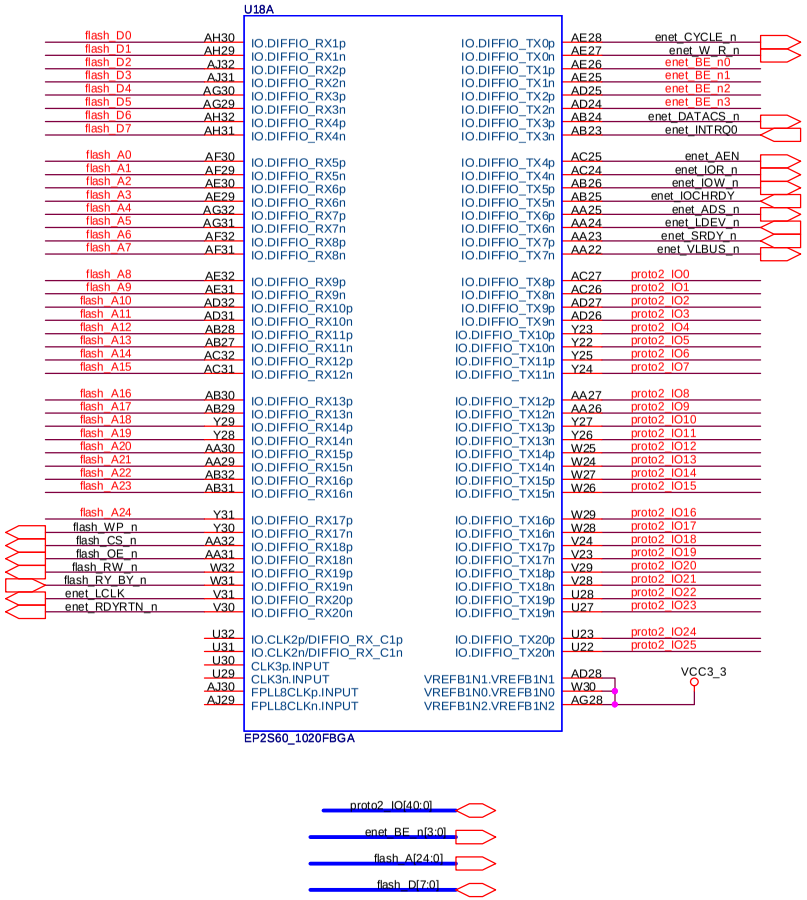

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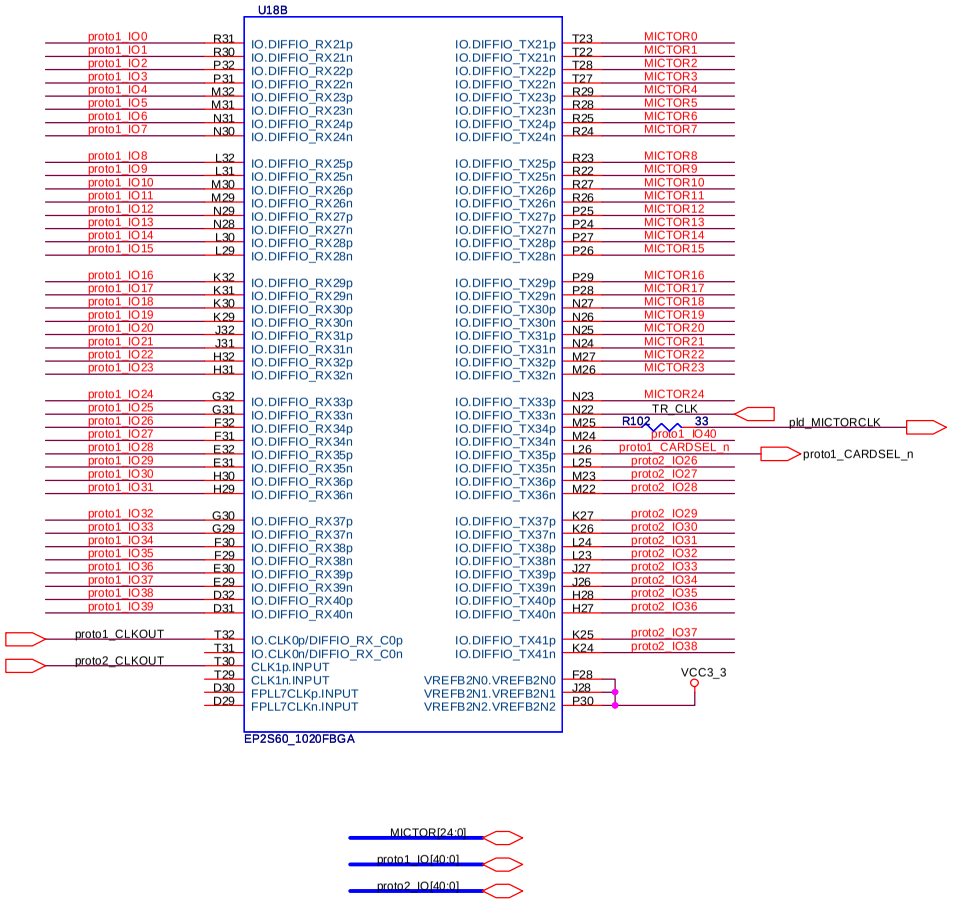
PLD Bank 2



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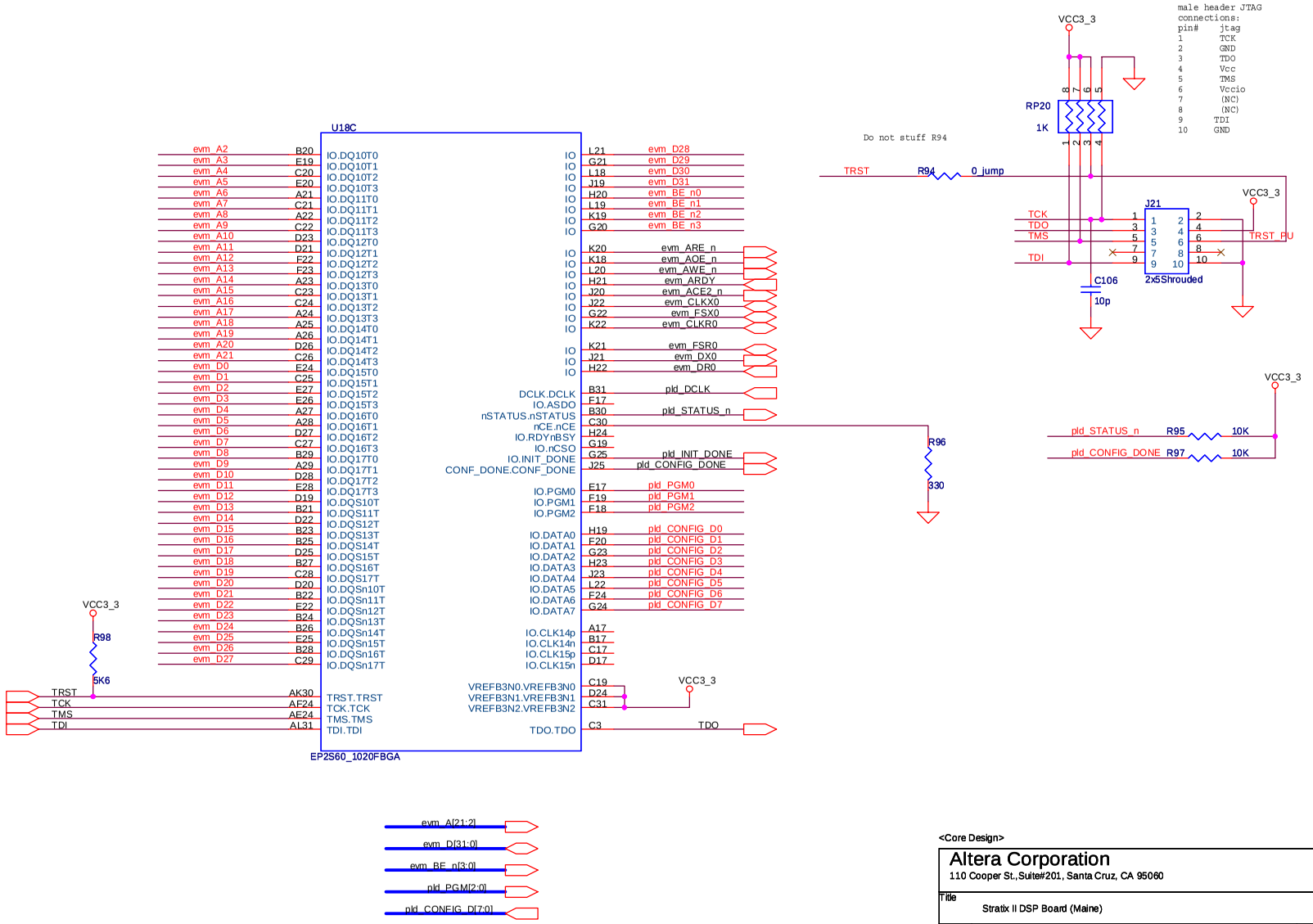
PLD Bank 3



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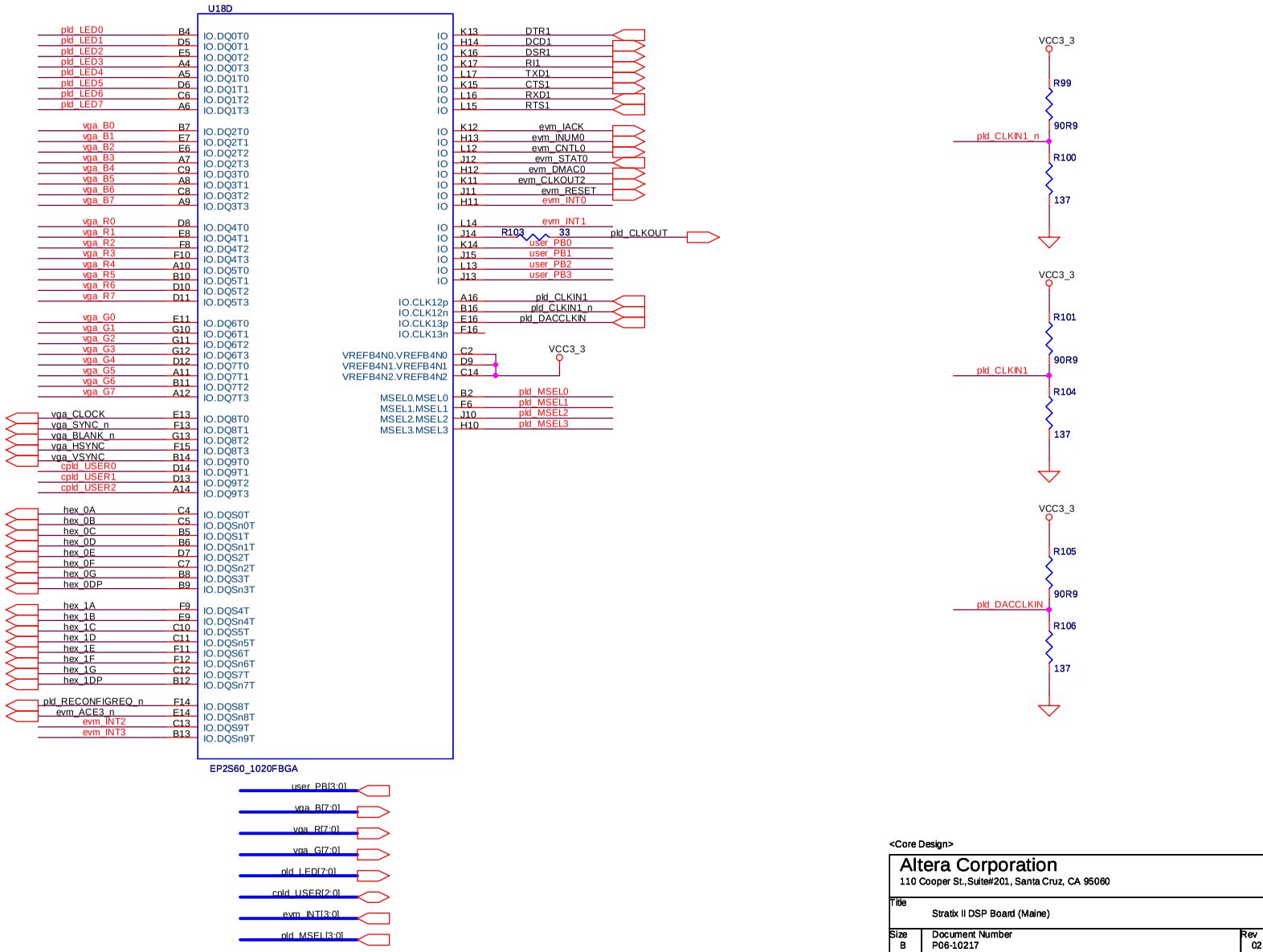
PLD Bank 4



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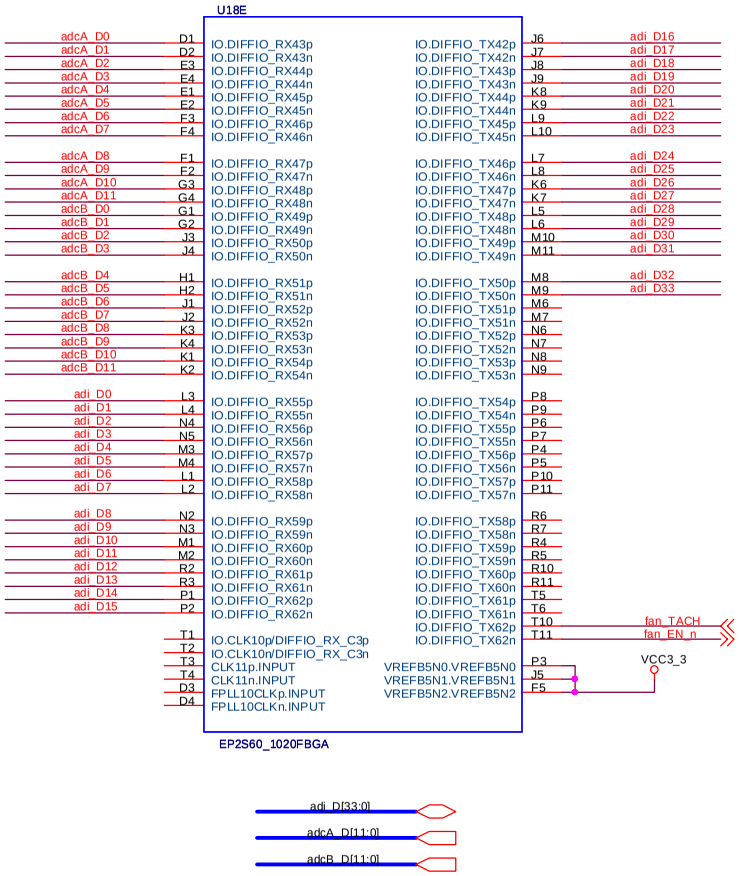
PLD Bank 5



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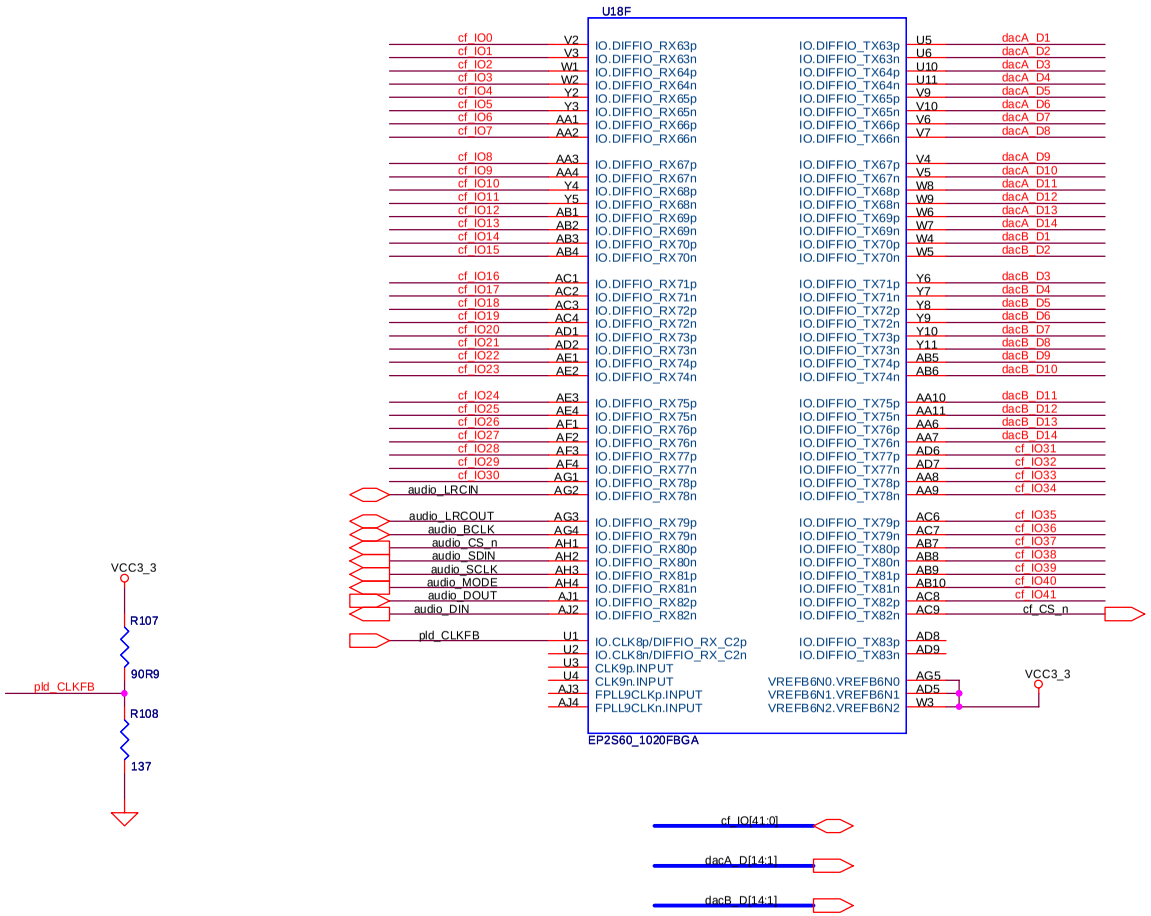
PLD Bank 6



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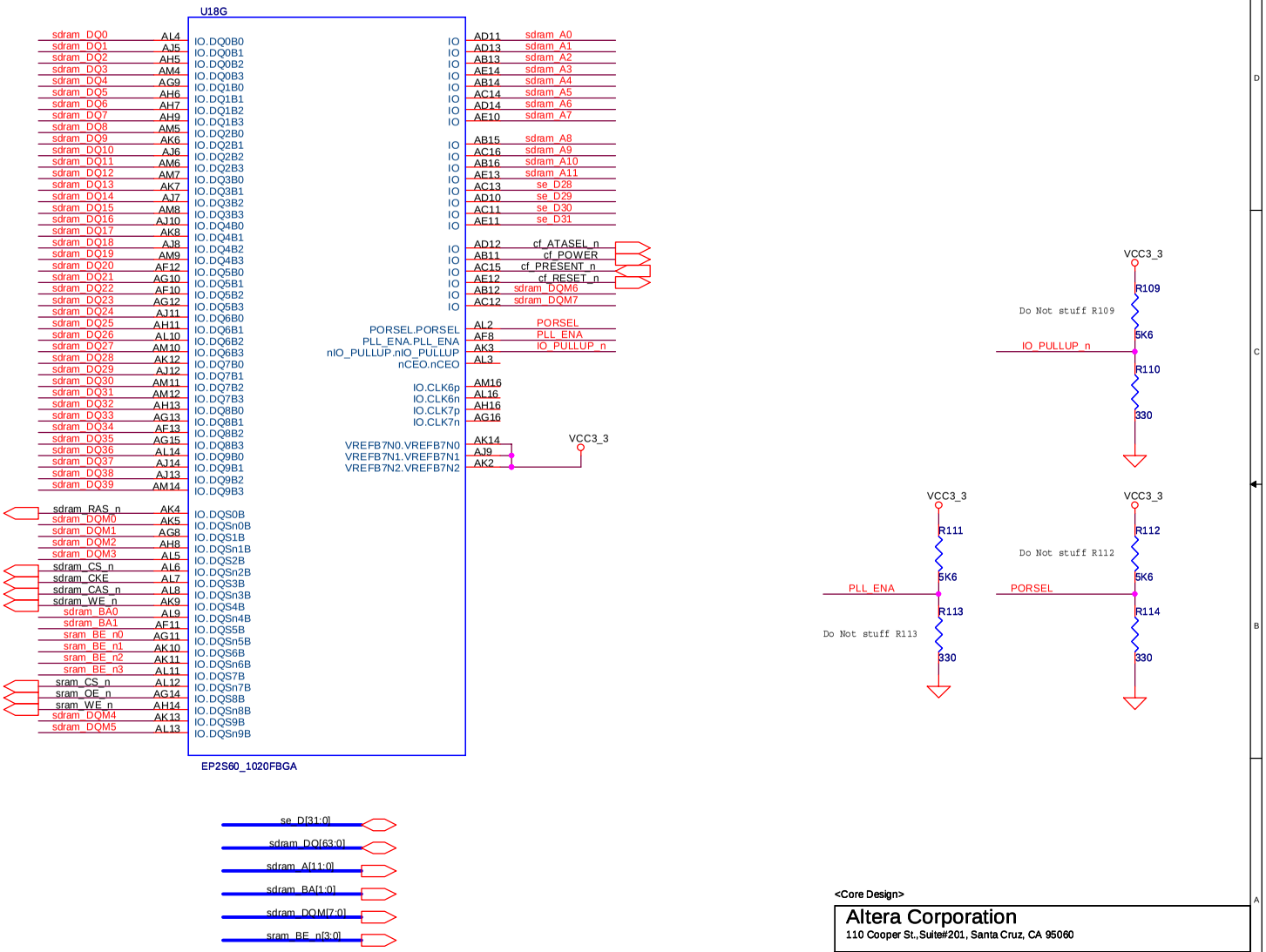
PLD Bank 7



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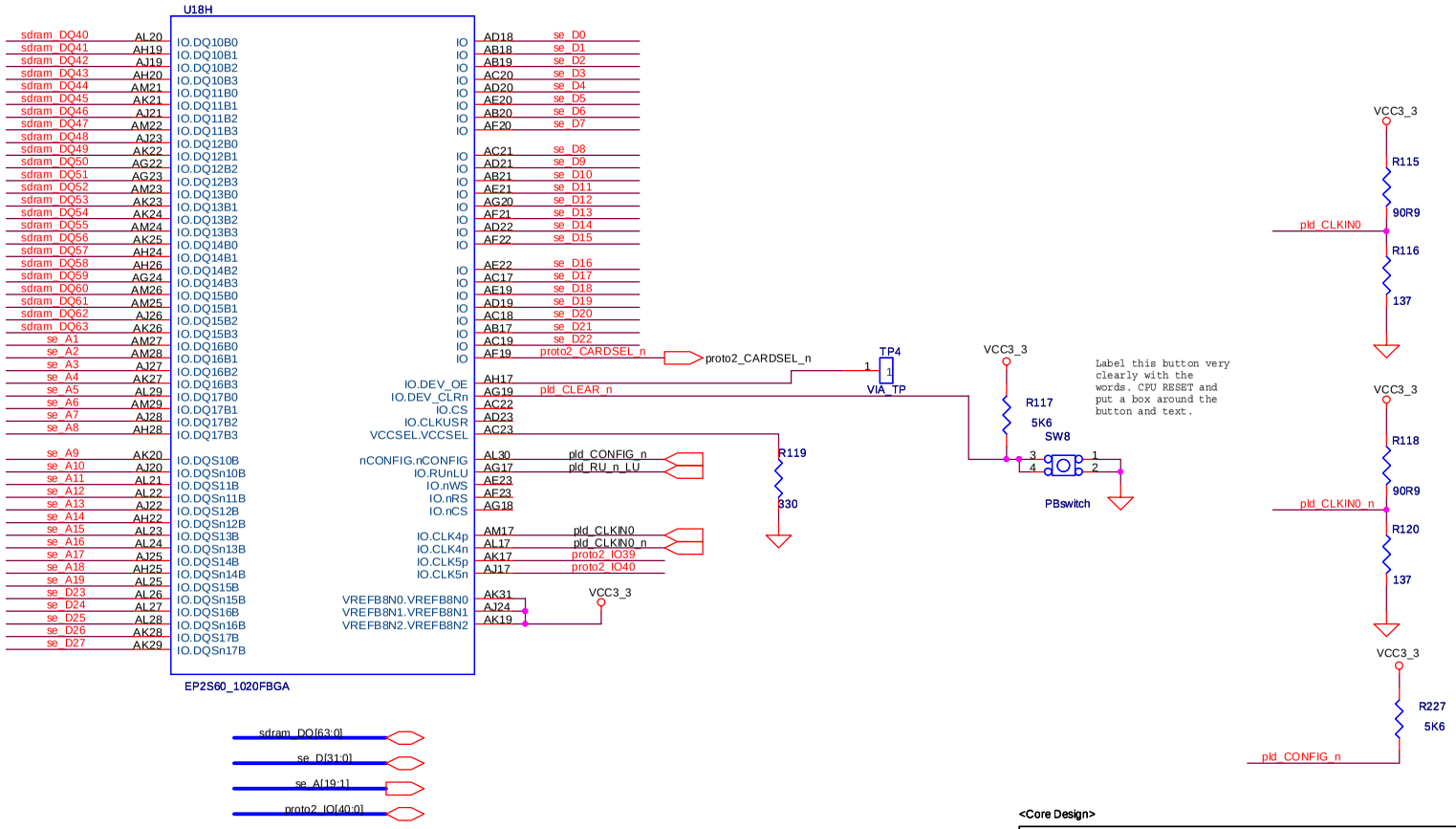
PLD Bank 8



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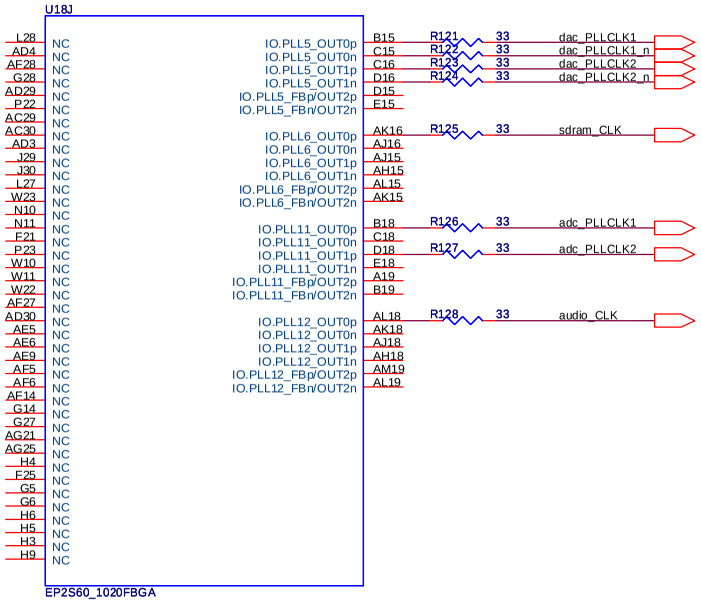
PLD Control Signals



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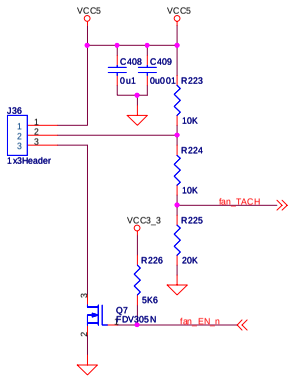

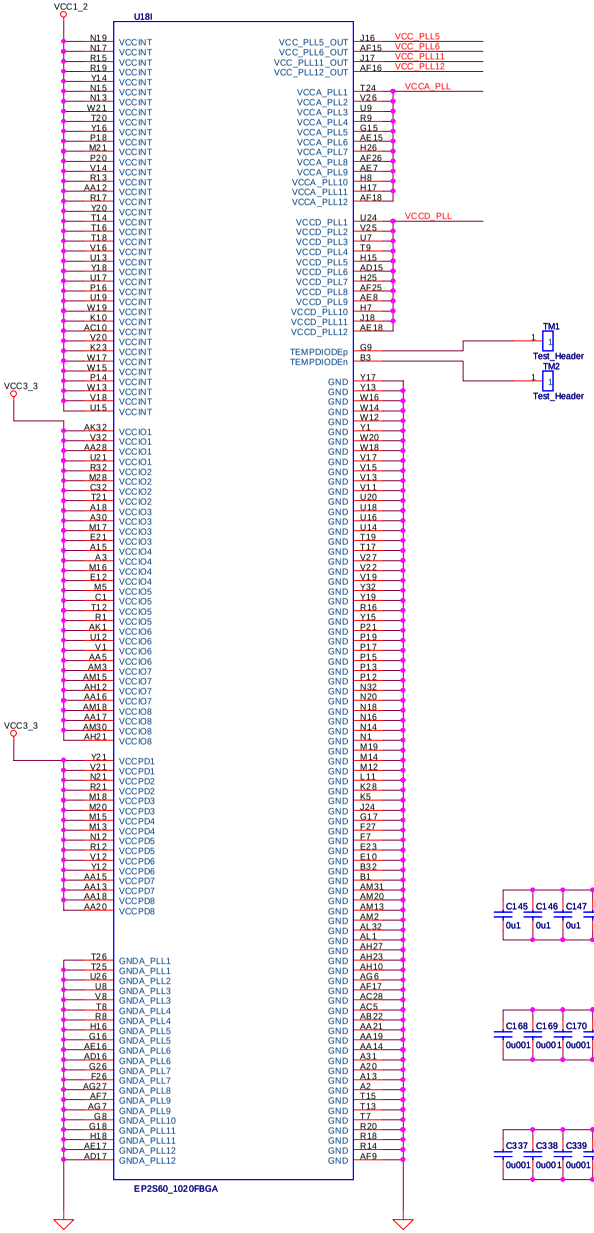

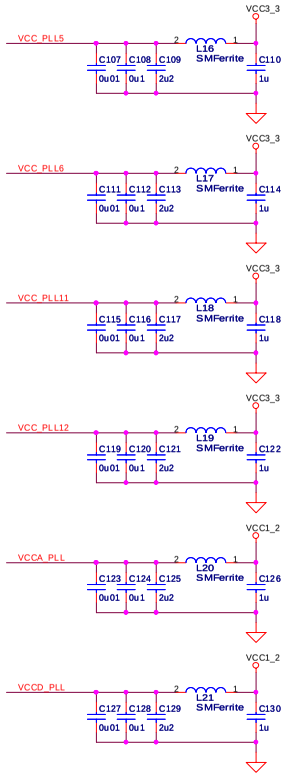

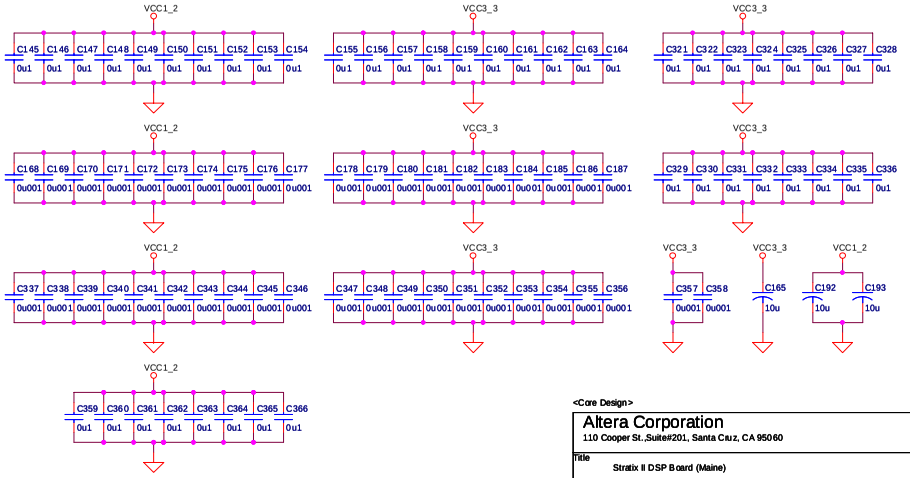

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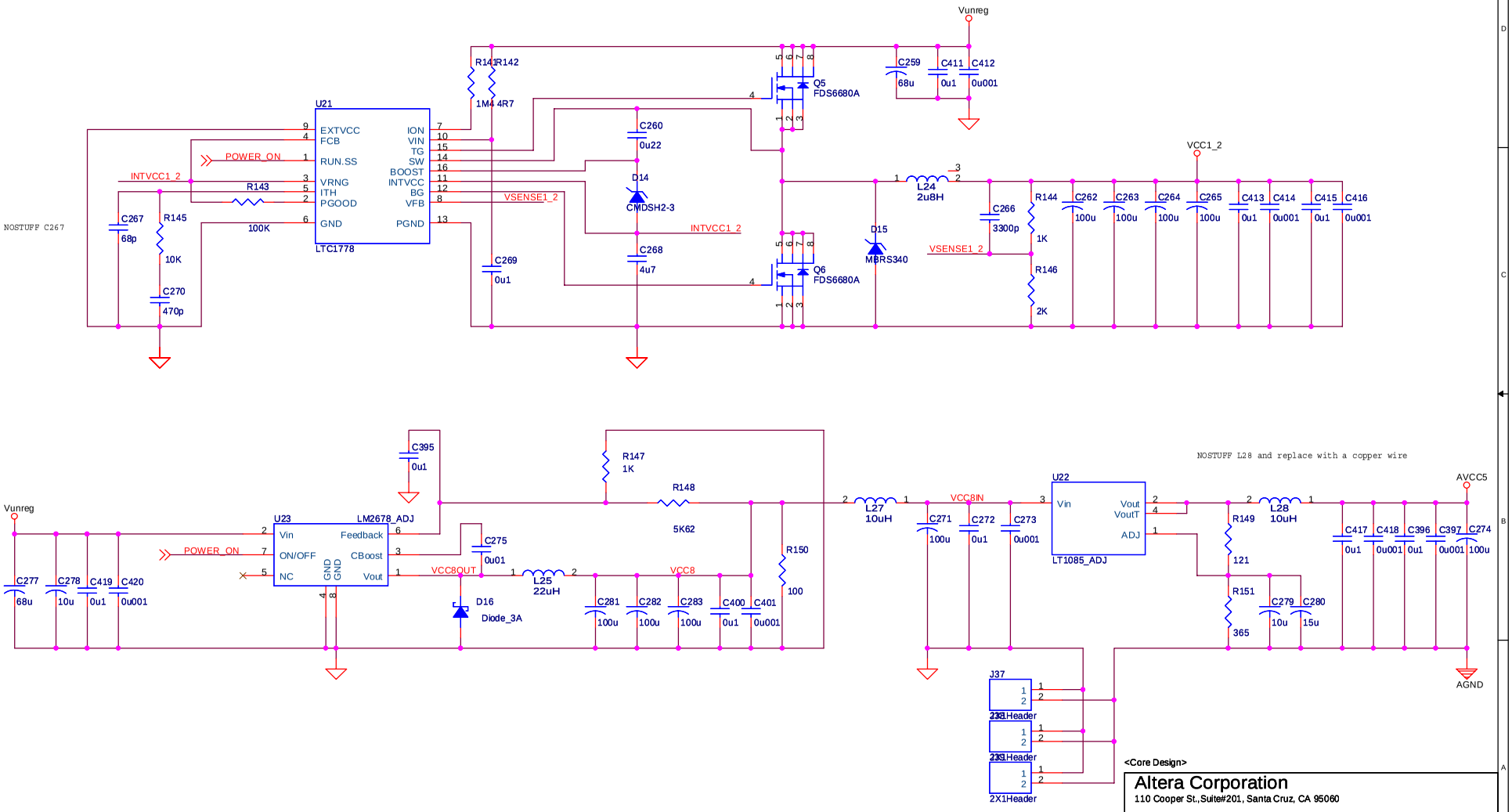
Power Connector



Note jumpers should always be installed to connect AGND to DGND uless and external GND sourse is being used.

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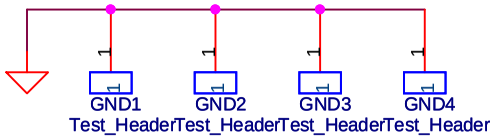
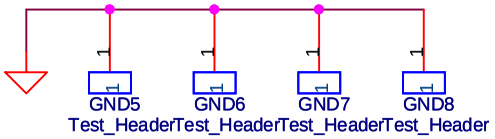
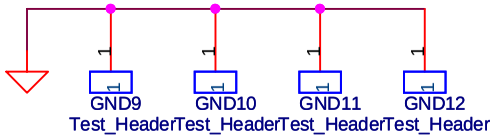
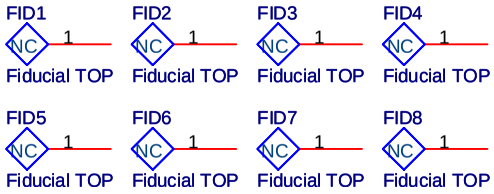
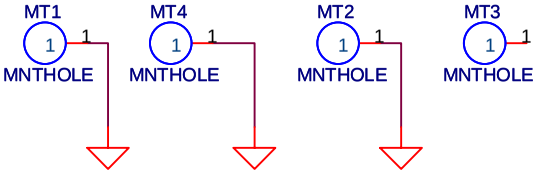
Reset and Test headers

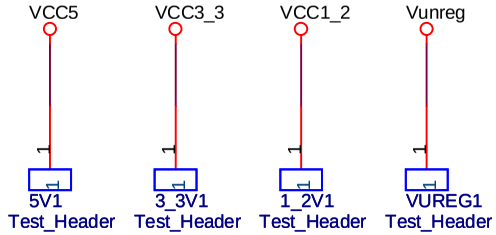


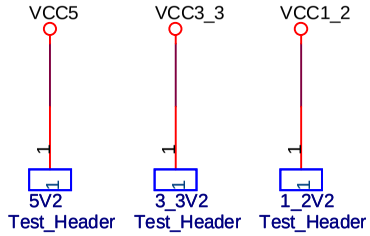


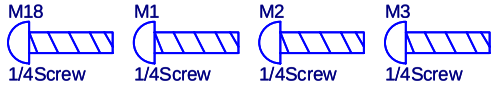


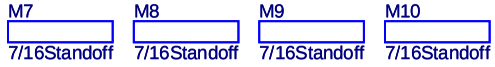


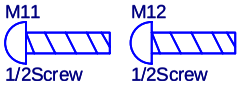


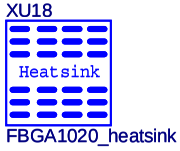












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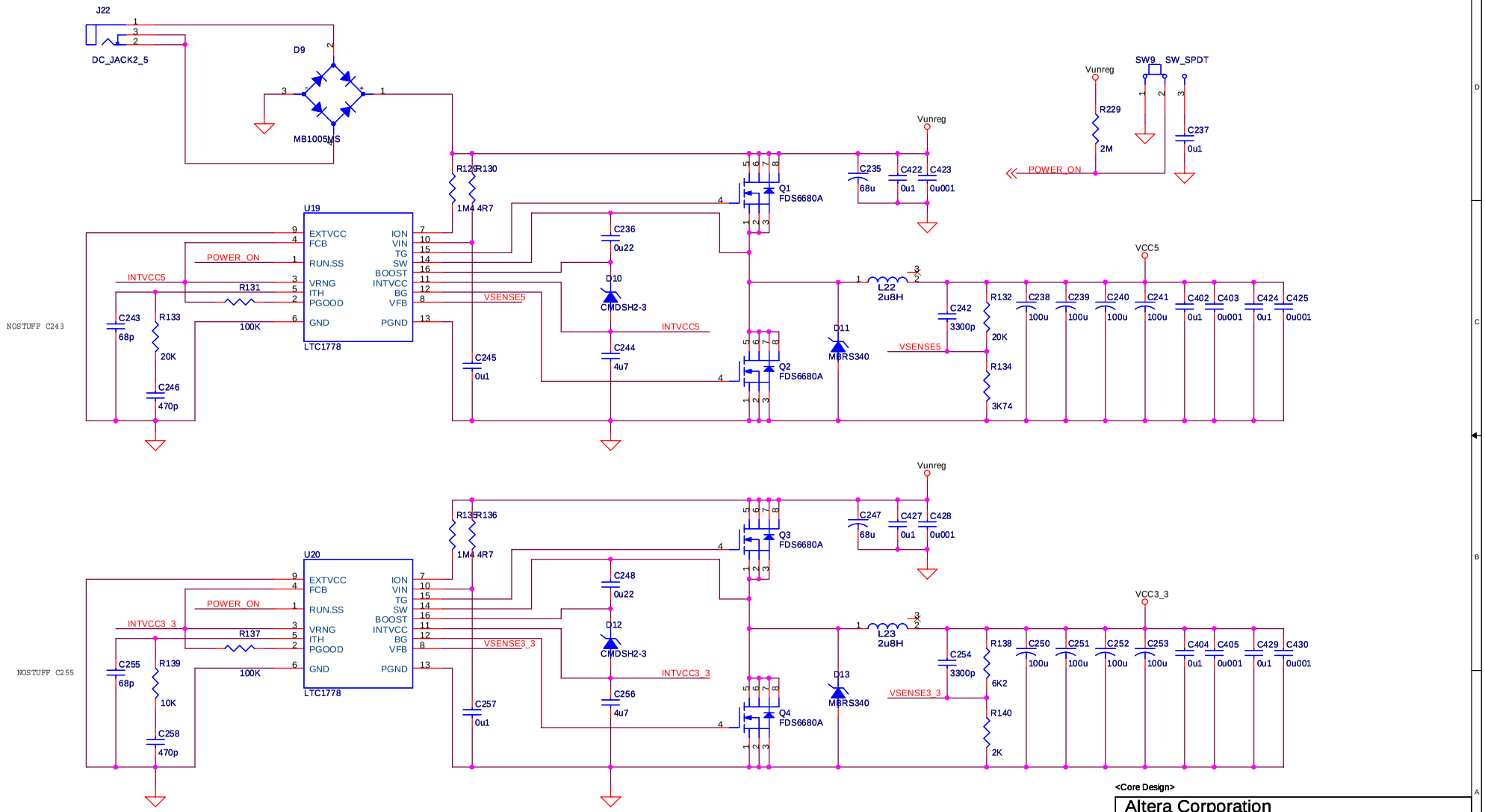
Power 5V and 3.3V



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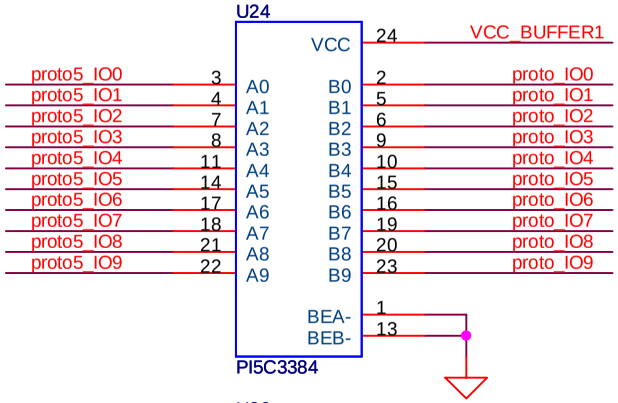
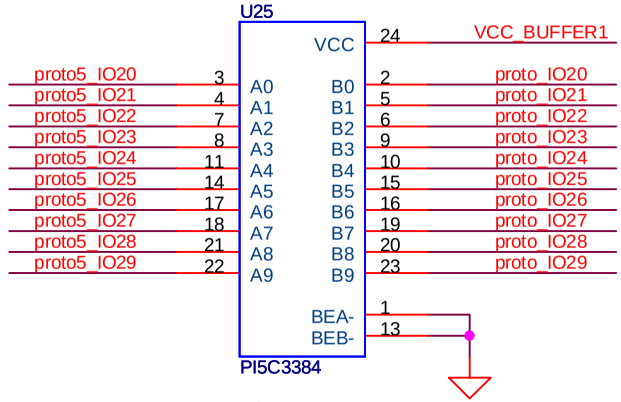
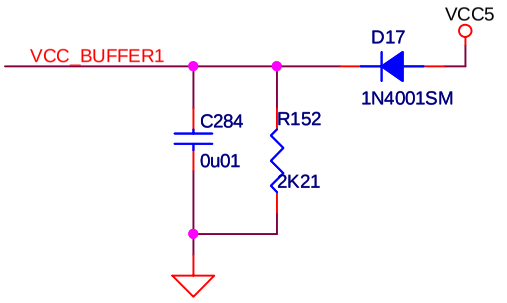
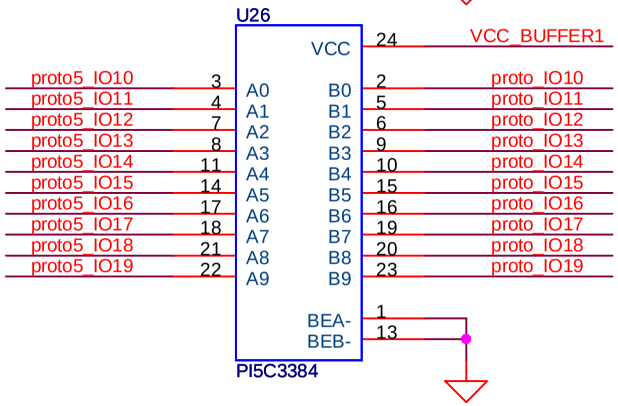
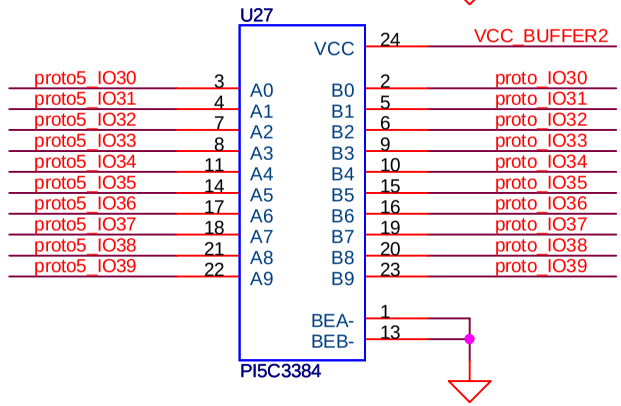
Proto1 Buffers

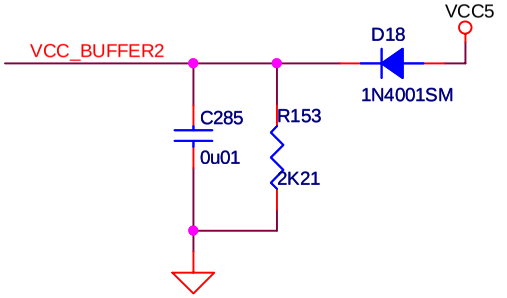


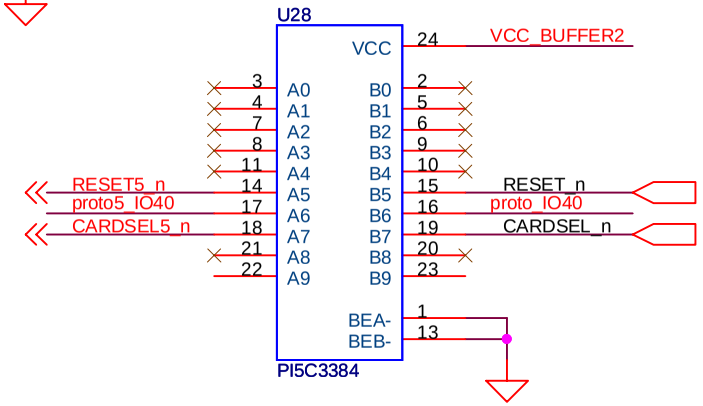




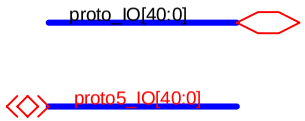


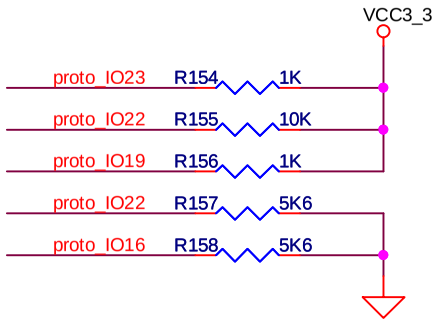






R155 and R157 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R155 should be a nostuff for production.





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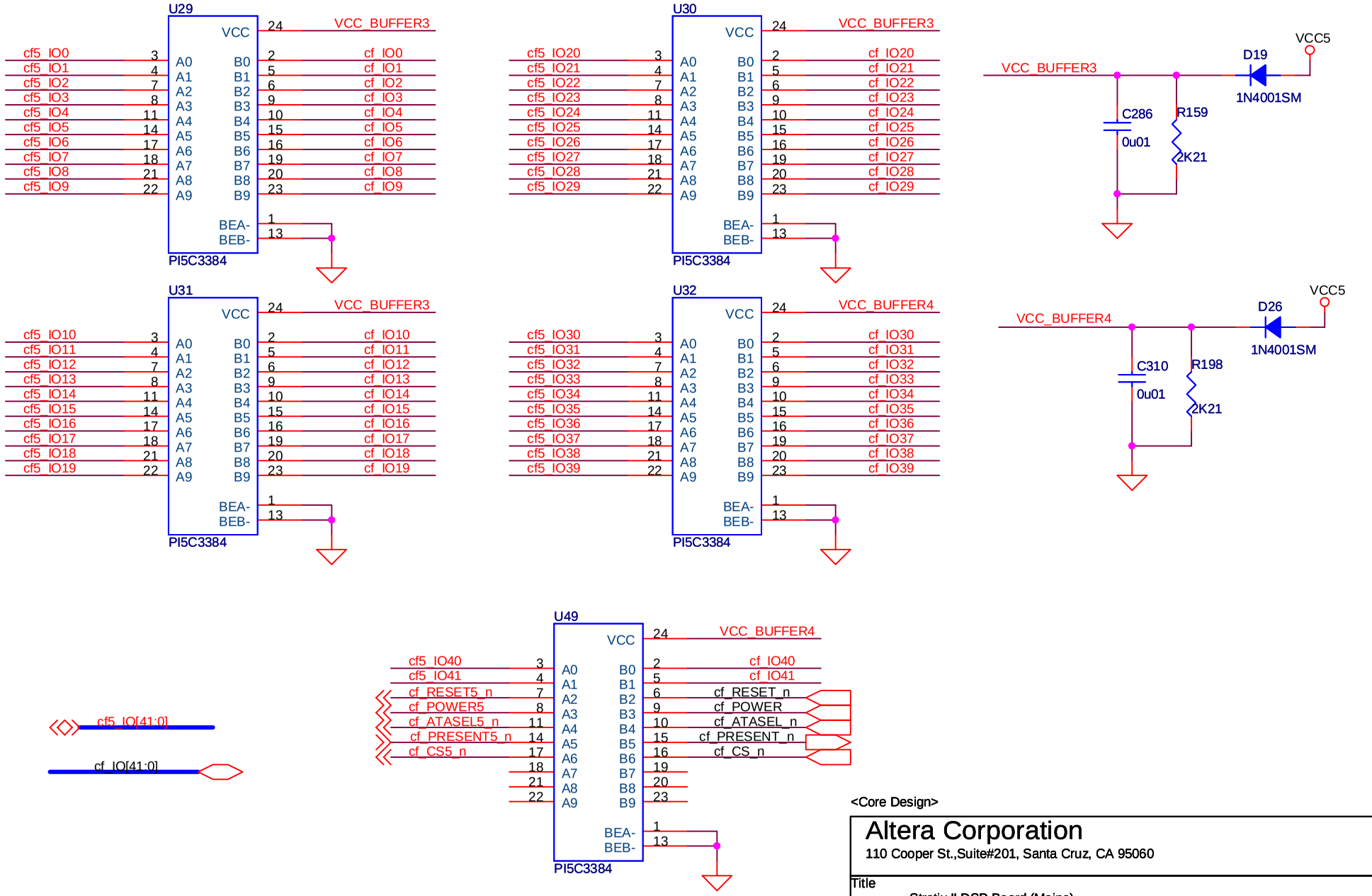

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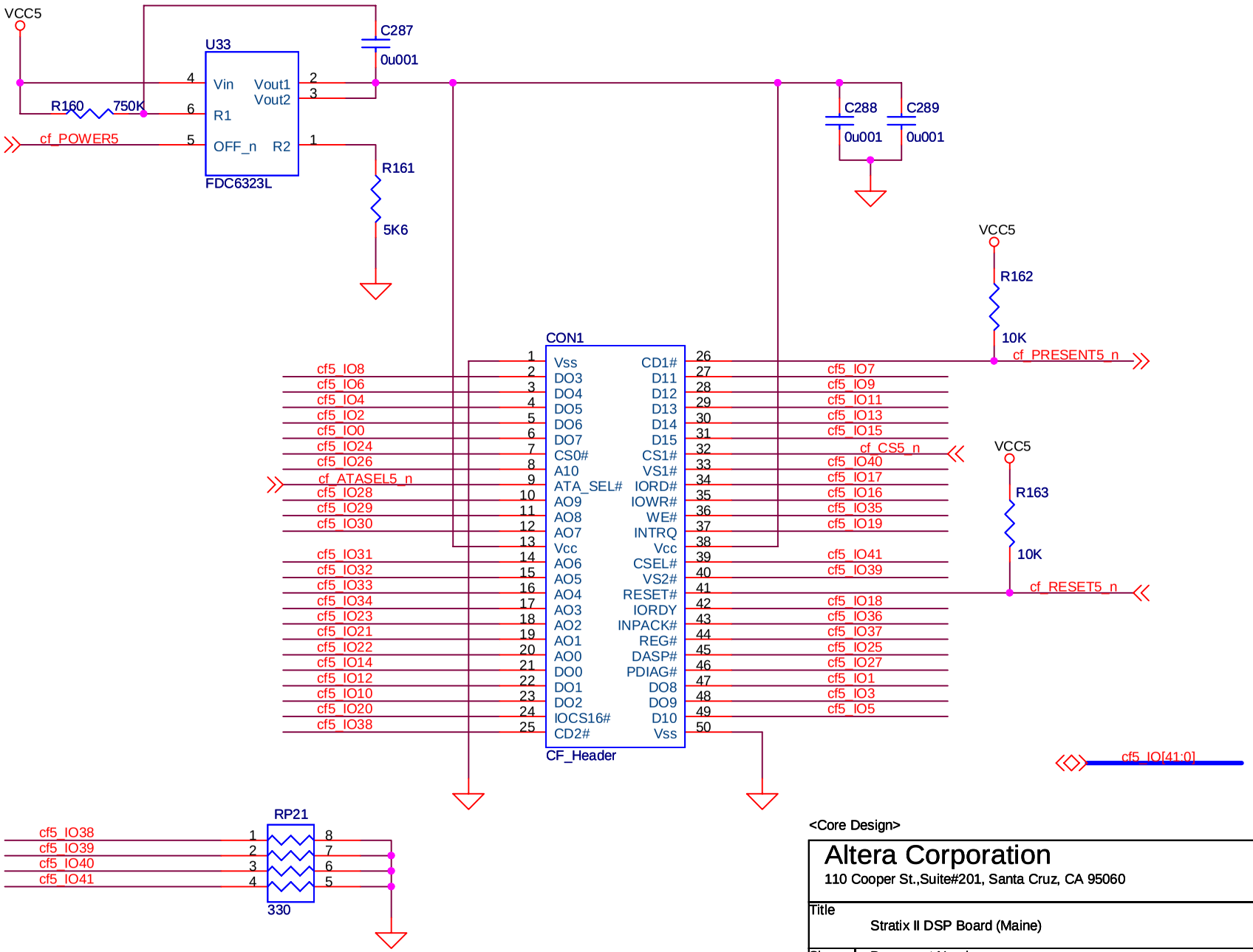
Compact Flash Socket



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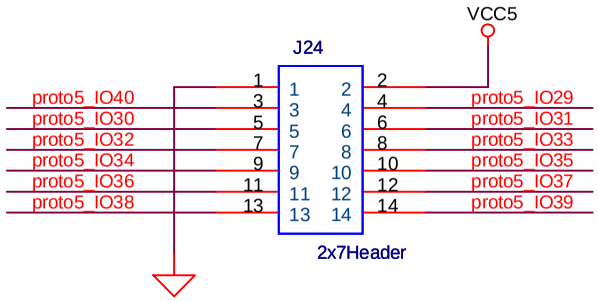
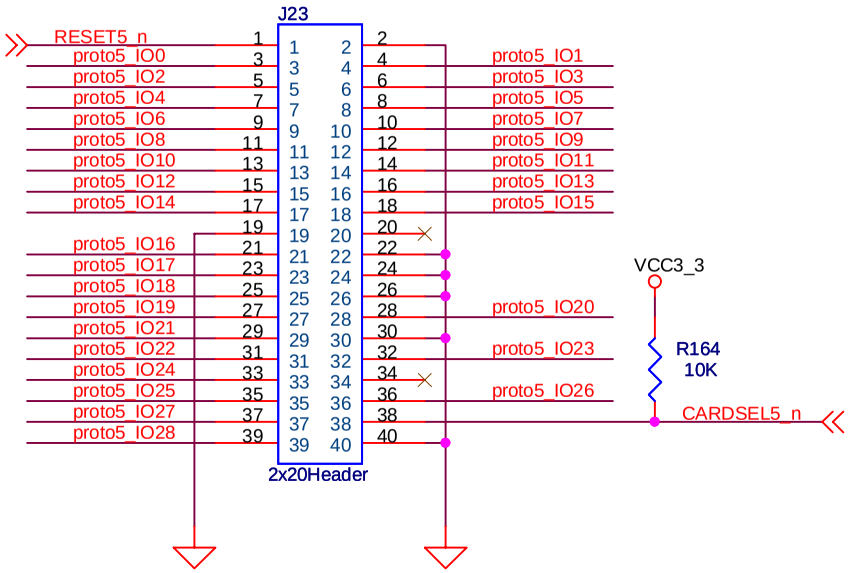
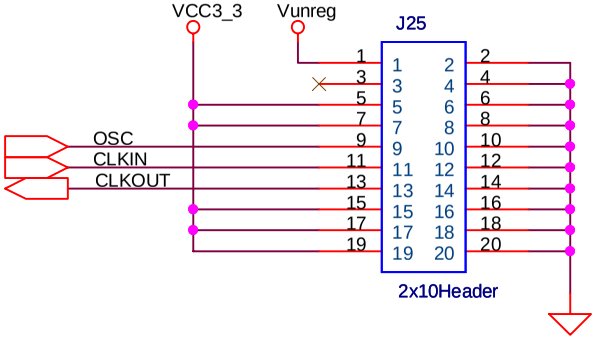
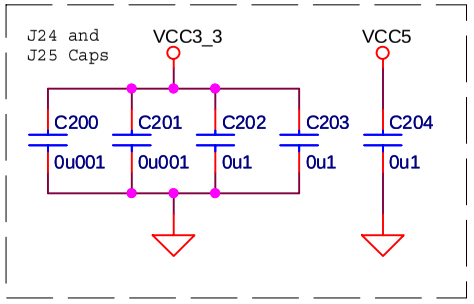
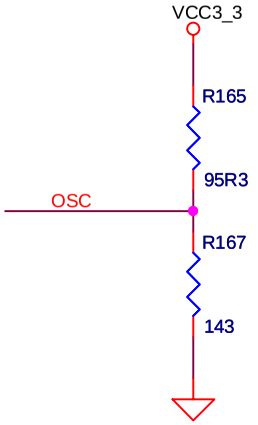
Protocard 1

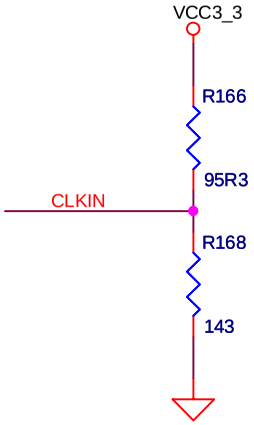


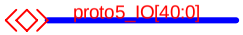












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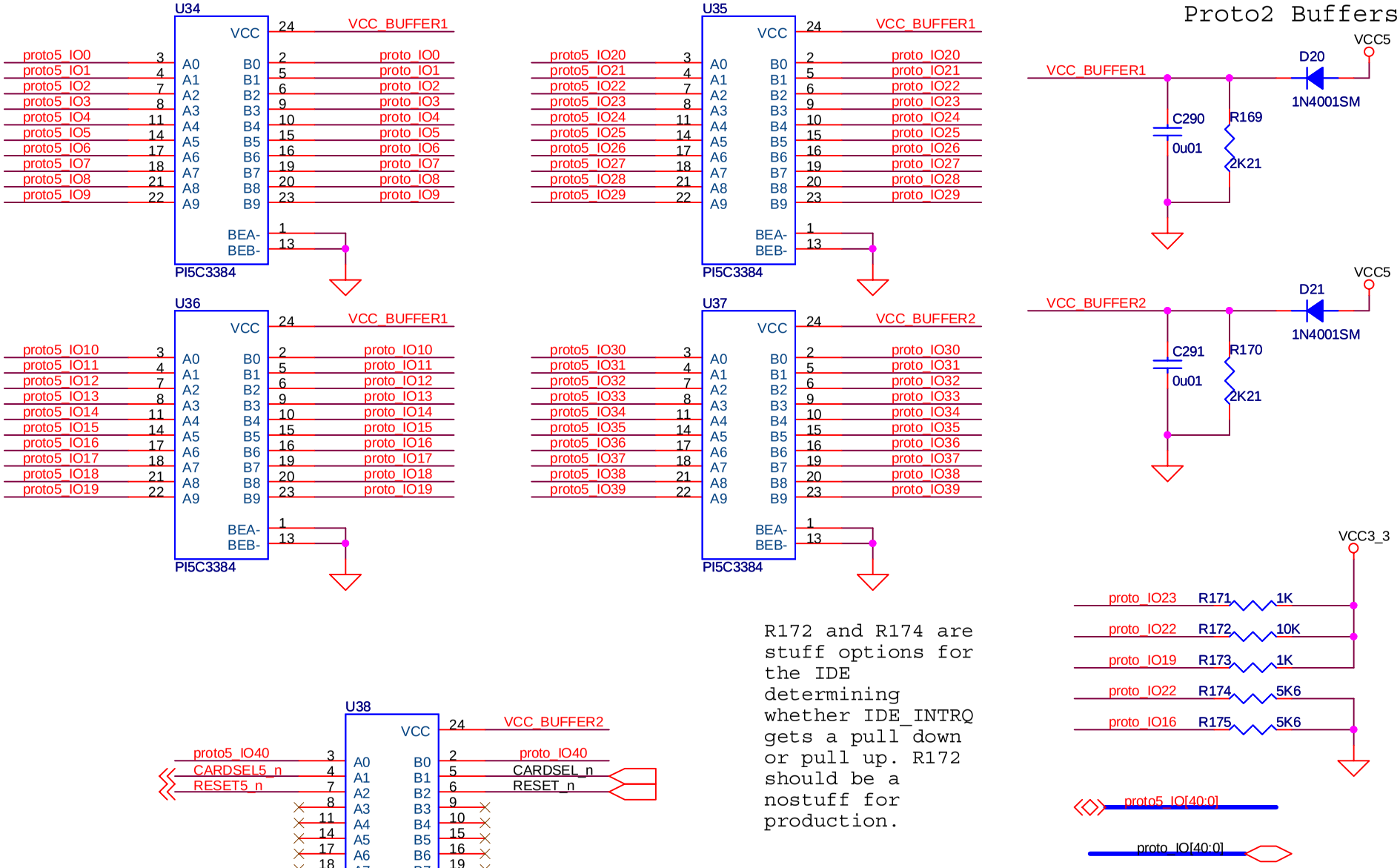
Proto2 Buffers



R172 and R174 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R172 should be a nostuff for production.

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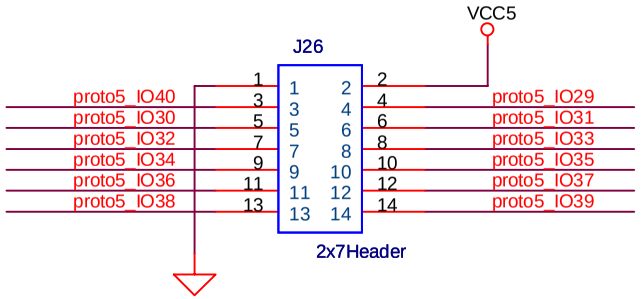
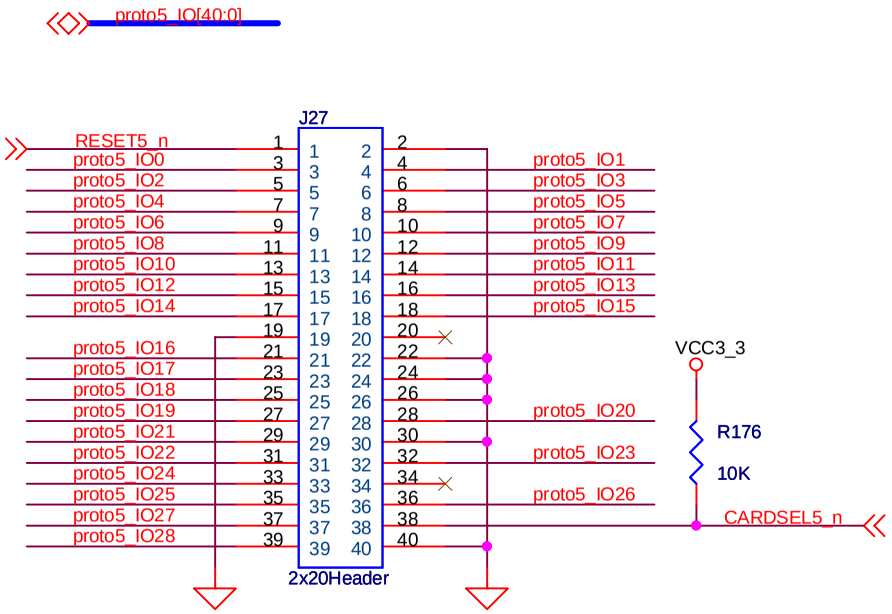
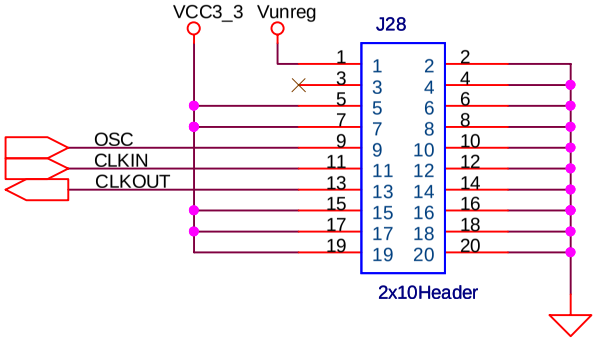
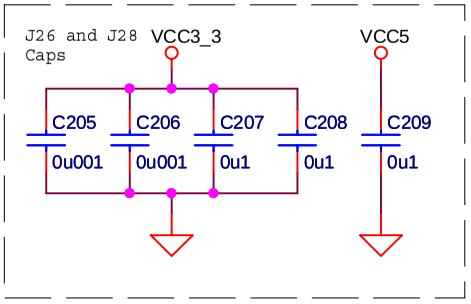
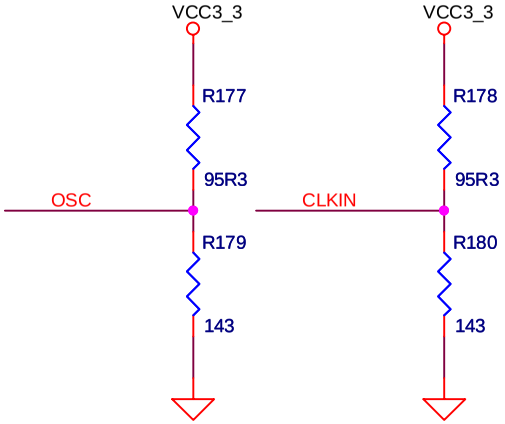
Proto2 Headers











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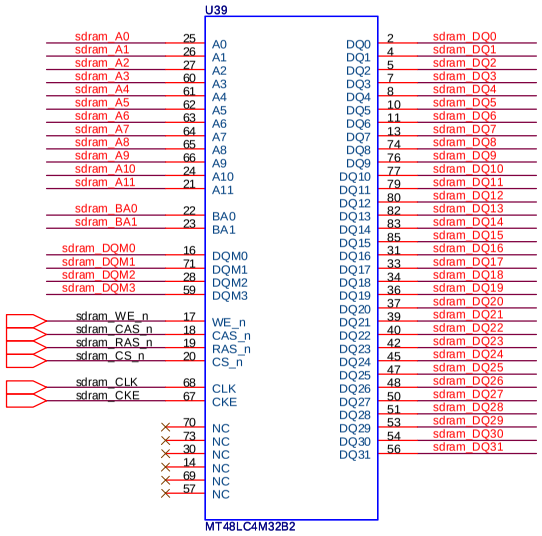

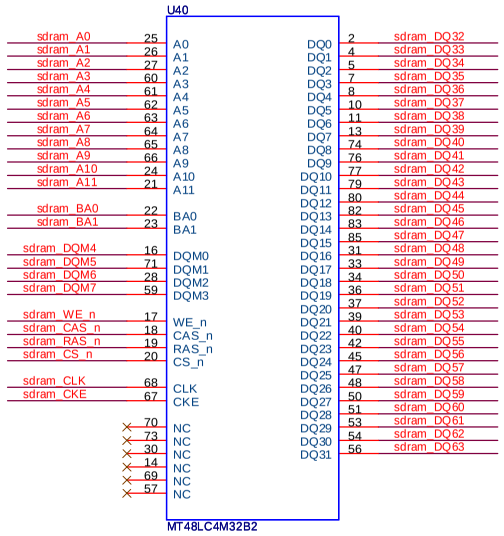

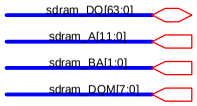

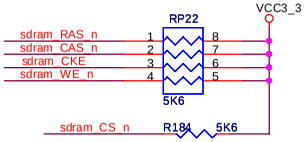

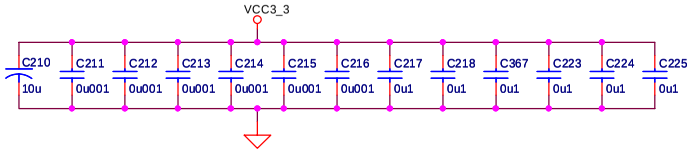

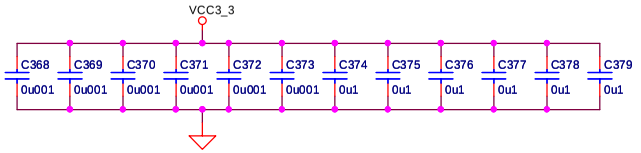

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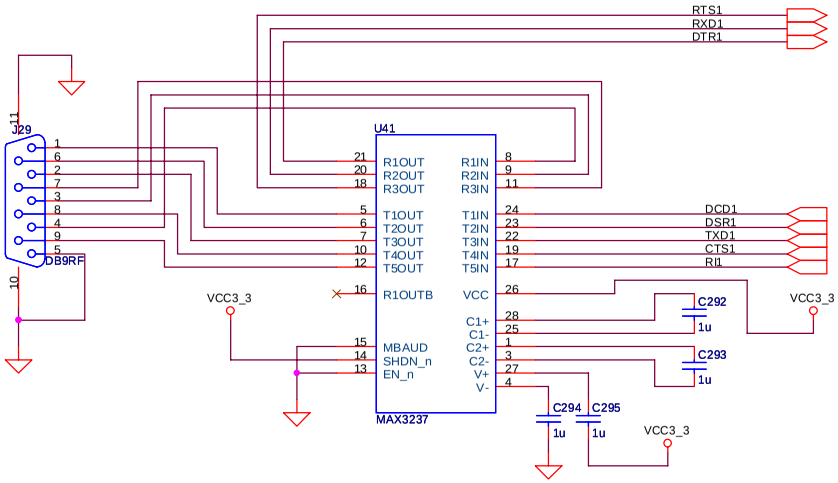
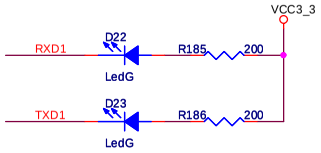
Serial Ports





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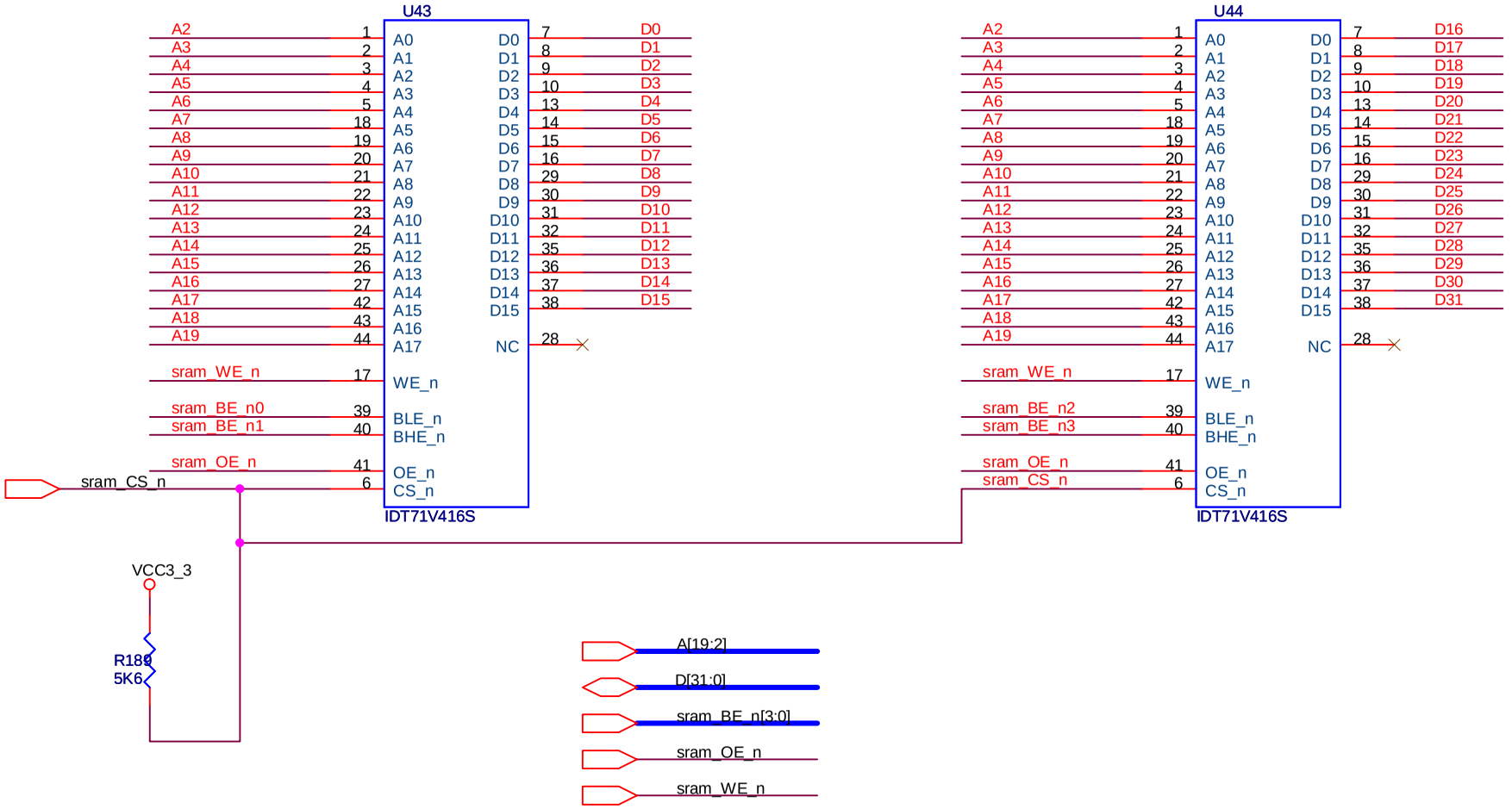
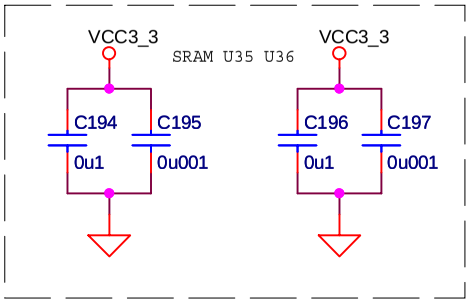
SRAM





One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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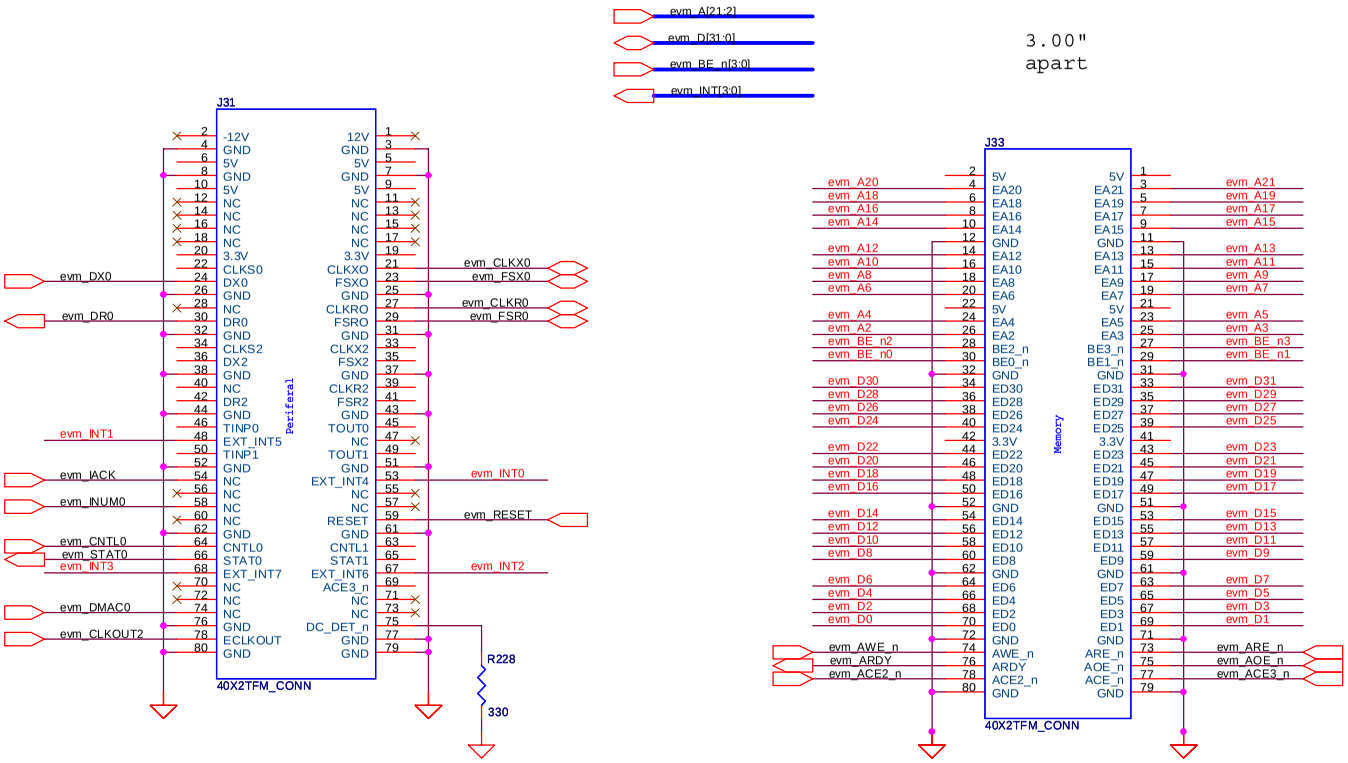
TI EVM Connector



These connectors reference the TI 6416 board

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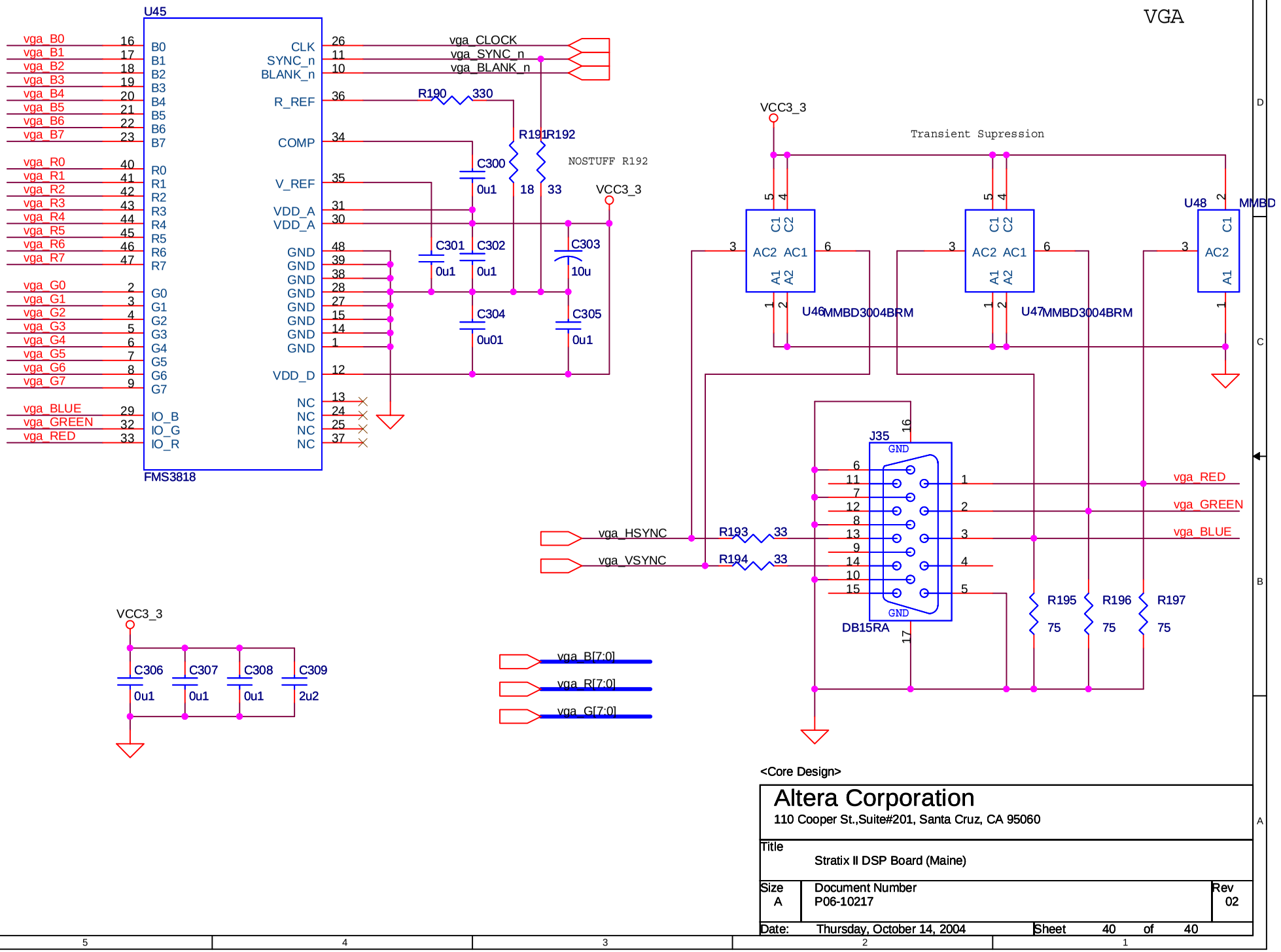
VGA
U45
vga_B0
vga_B1
vga_B2
vga_B3
vga_B4
vga_B5
vga_B6
vga_B7
vga_R0
vga_R1
vga_R2
vga_R3
vga_R4
vga_R5
vga_R6
vga_R7
vga_G0
vga_G1
vga_G2
vga_G3
vga_G4
vga_G5
vga_G6
vga_G7
vga_BLUE
vga_GREEN
vga_RED
B0
B1
B2
B3
B4
B5
B6
B7
R0
R1
R2
R3
R4
R5
R6
R7
G0
G1
G2
G3
G4
G5
G6
G7
IO_B
IO_G
IO_R
CLK
SYNC_n
BLANK_n
R_REF
COMP
V_REF
VDD_A
VDD_A
GND
VDD_D
NC
FMS3818
vga_CLOCK
vga_SYNC_n
vga_BLANK_n
R190 330
R191 18
R192 33
NOSTUFF R192
C300 0u1
C301 0u1
C302 0u1
C303 10u
C304 0u01
C305 0u1
VCC3_3
Transient Supression
U46 MMBD3004BRM
U47 MMBD3004BRM
U48 MMBD
AC1 AC2 A1 A2 C1 C2
J35
DB15RA
vga_HSYNC
vga_VSYNC
R193 33
R194 33
R195 75
R196 75
R197 75
vga_RED
vga_GREEN
vga_BLUE
C306 0u1
C307 0u1
C308 0u1
C309 2u2
vga_B[7:0]
vga_R[7:0]
vga_G[7:0]
<Core Design>
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