

# DSP Development Board Stratix II Edition

## Rev 02

Revision History		Rev
Date	Change Description	
10/21/03	Started design	01
2/5/04	Sent out schematic for first design review	01
7/30/04	Started Rev02 changed per document Maine_board_bringup.doc	02

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**Altera Corp.**

110 Cooper Street, Suite 201, Santa Cruz, CA 95060

Title

Stratix II DSP Board (Maine)

Size

A

Document Number

P06-10217

Rev

02

Date:

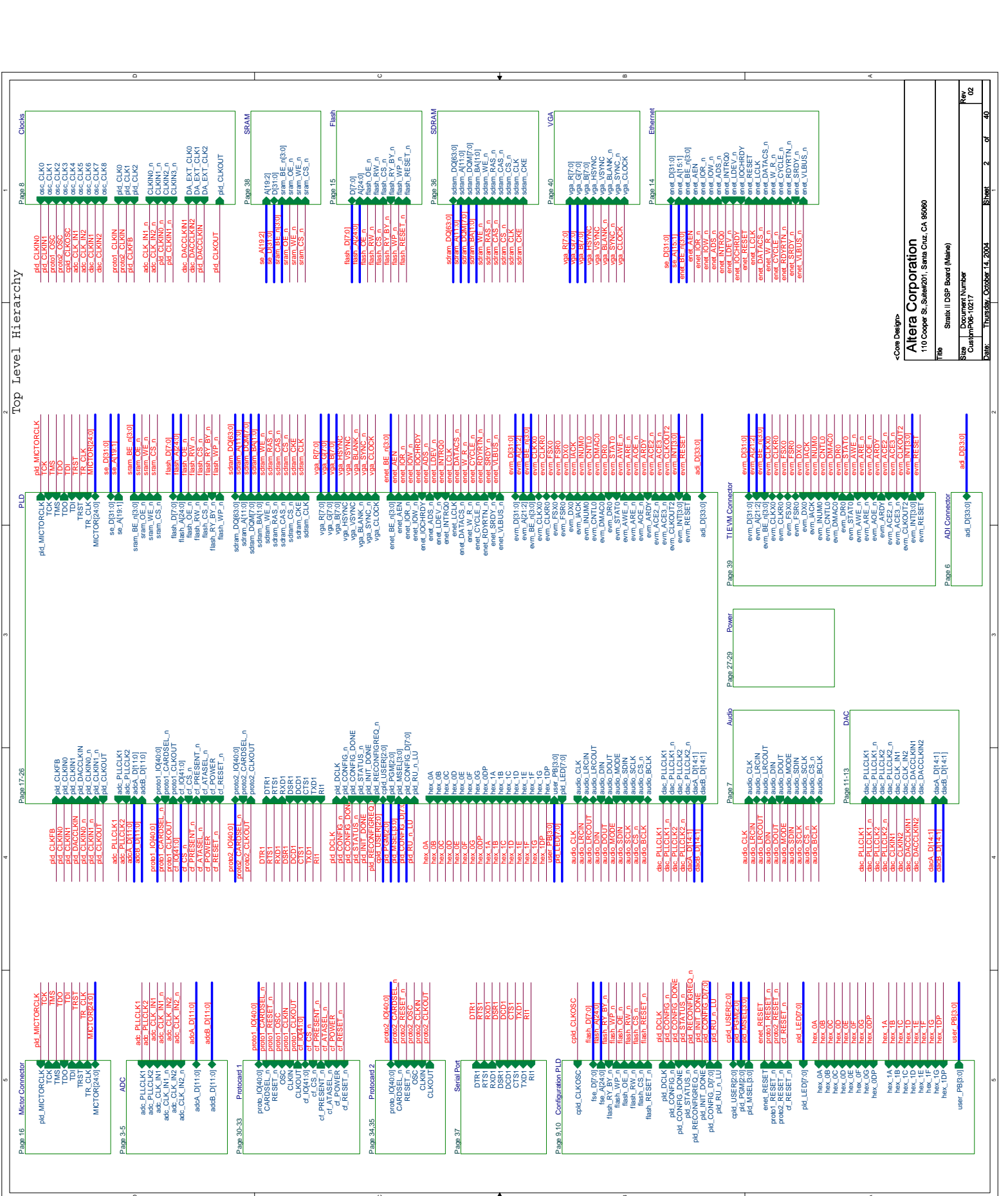
Thursday, October 14, 2004

Sheet

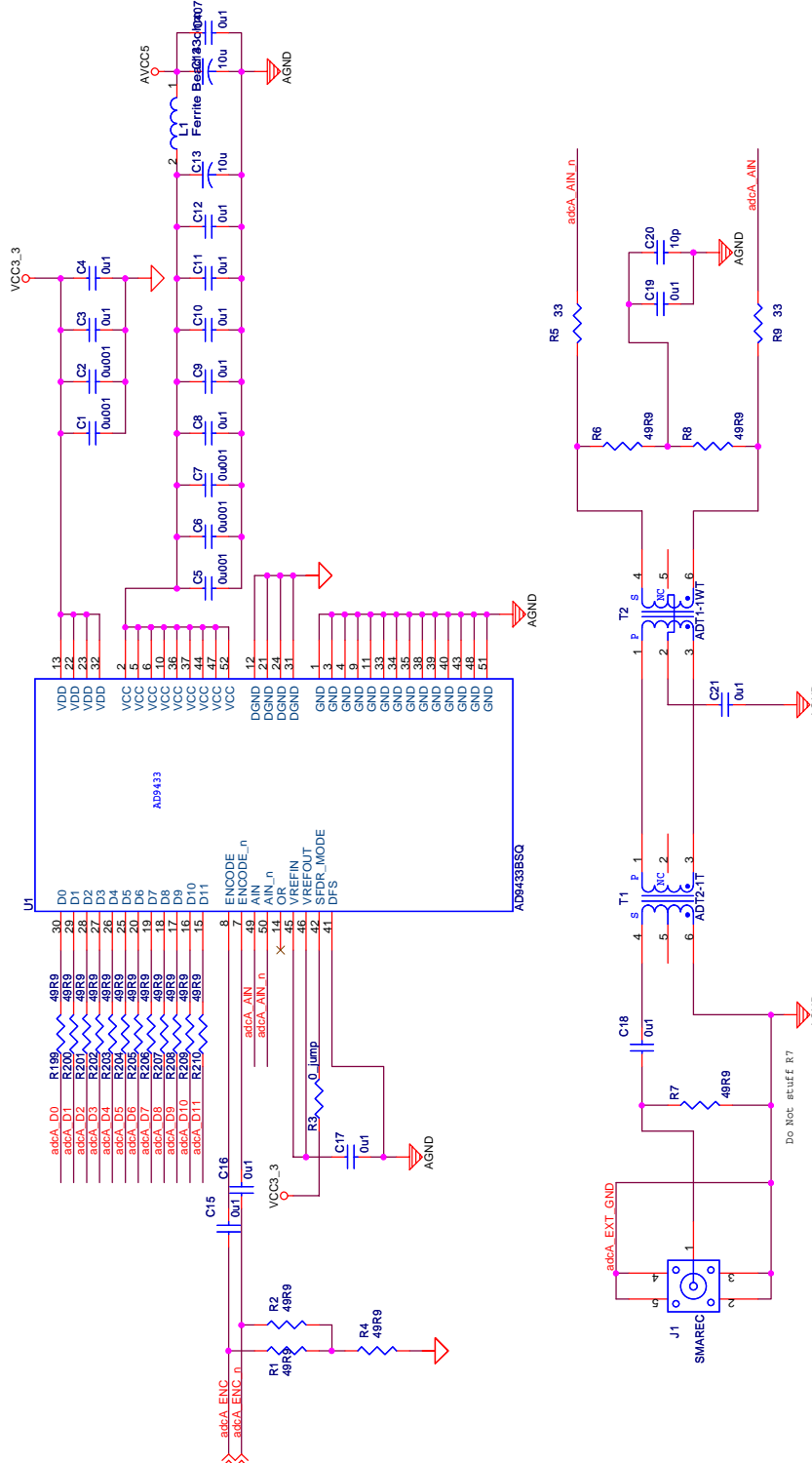
1 of

40

# Top Level Hierarchy



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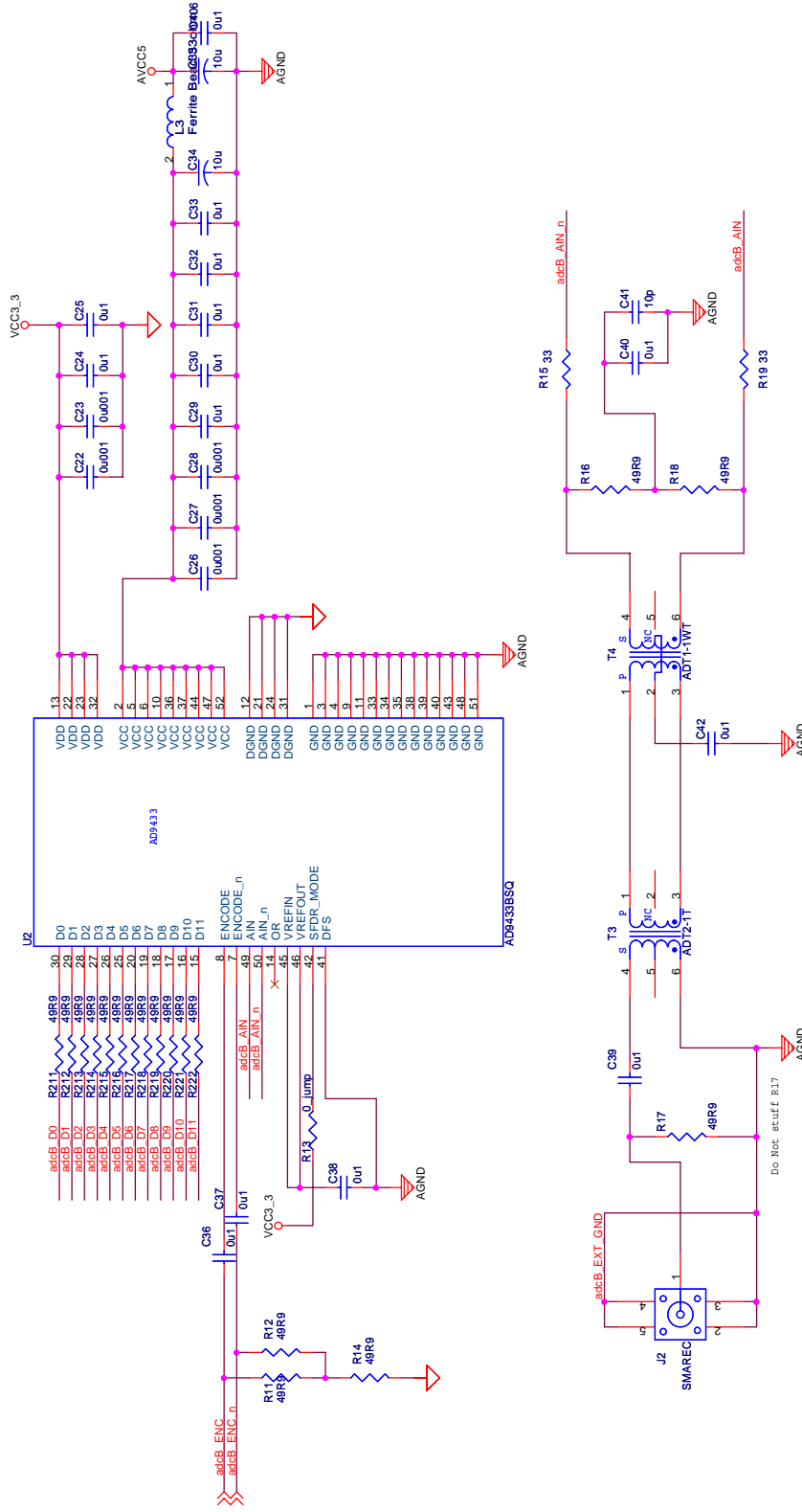


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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	
B	P06-10217	02	
Date	Thursday, October 14, 2004	Sheet	3 of 40

adcB\_D11(0)

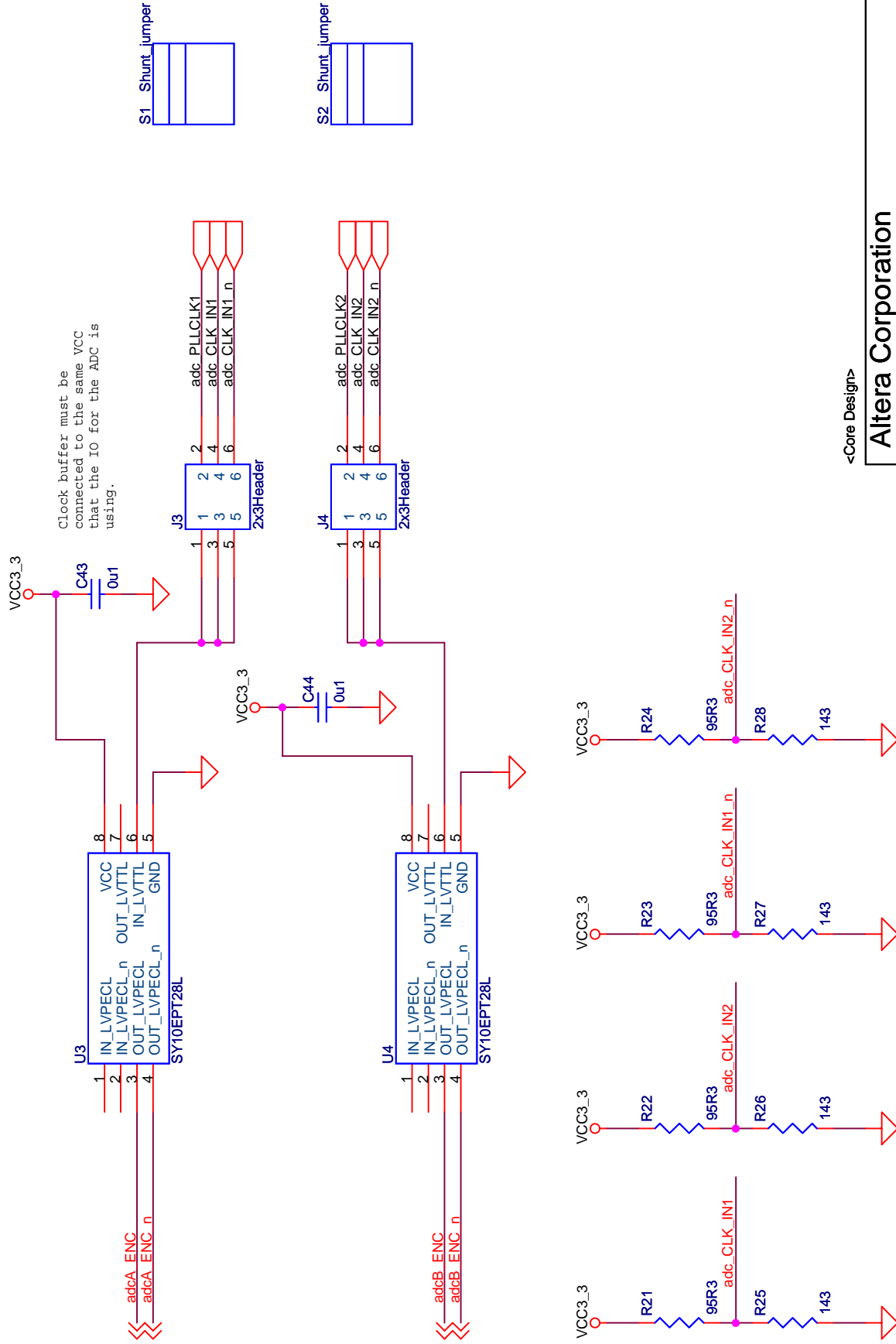


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Title	Stratix II DSP Board (Maine)
Size	Document Number
B	P06-10217
Rev	02
Date	Thursday, October 14, 2004
Sheet	4 of 40

# ADC Clock Selection



Clock buffer must be connected to the same VCC that the IO for the ADC is using.

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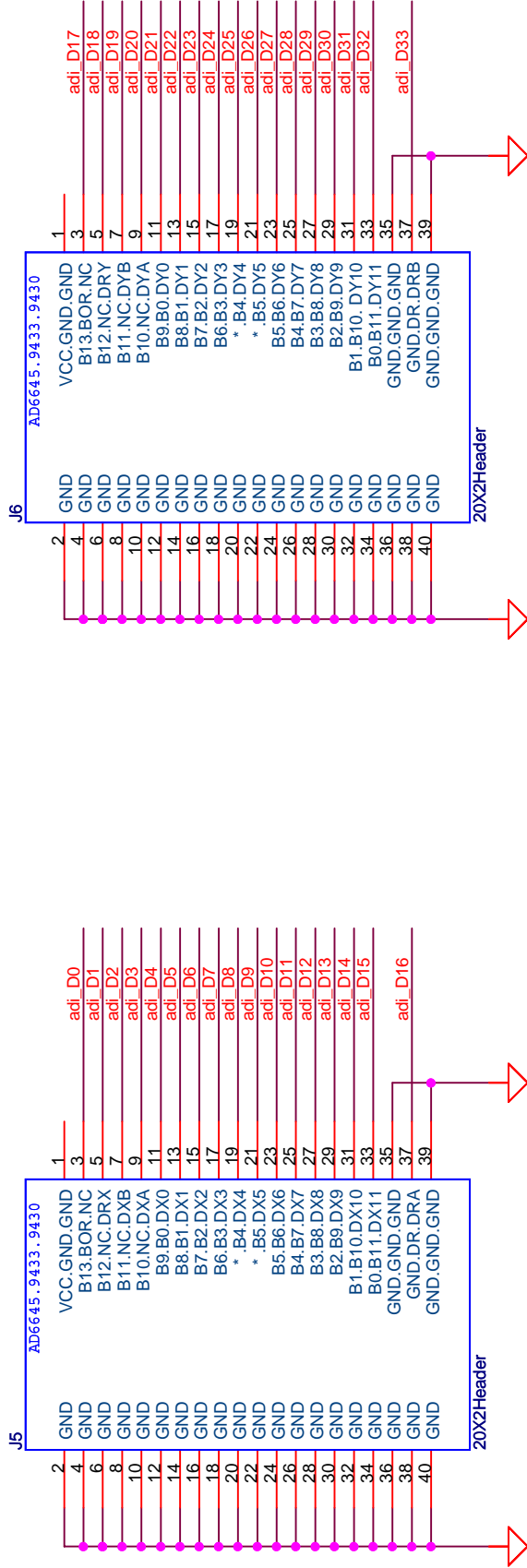
Thursday, October 14, 2004

Sheet

5 of 40

# ADI Connector

adi\_D[33:0]



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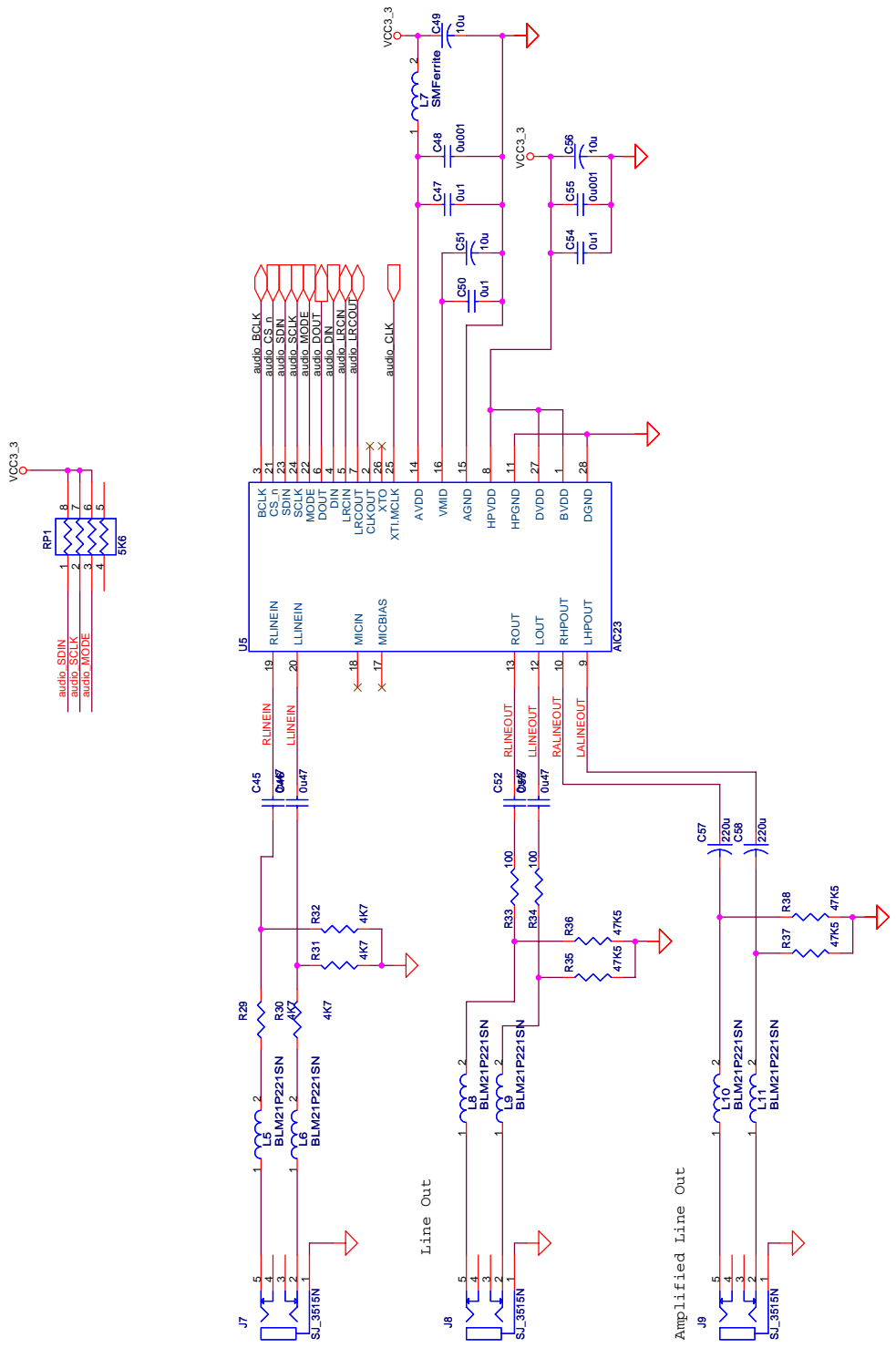
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Date:

Thursday, October 14, 2004

Sheet

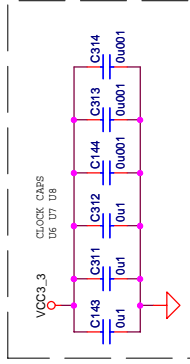
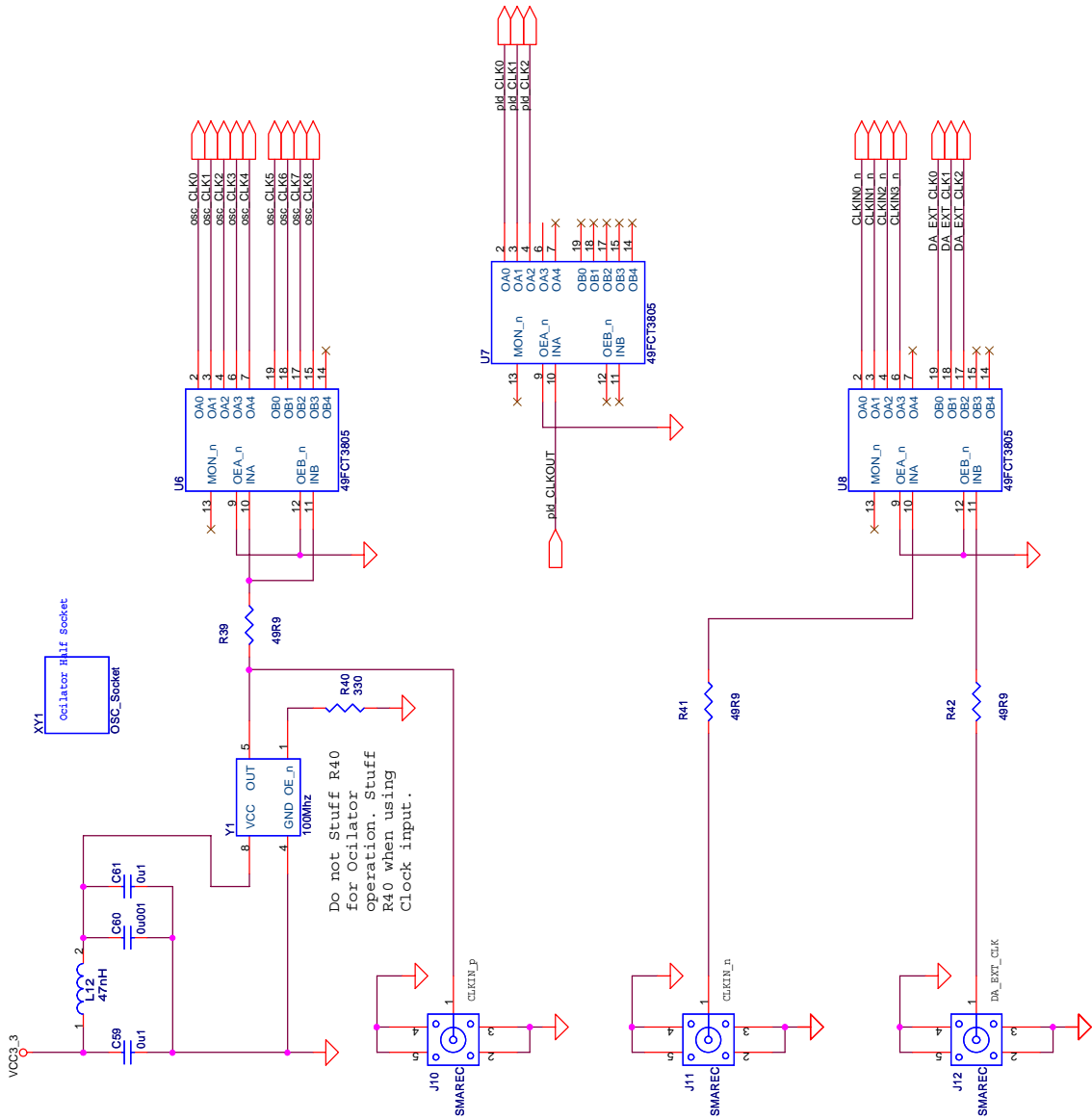
6 of 40



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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	02
B	P06-10217	Date	Thursday, October 14, 2004
		Sheet	7 of 40



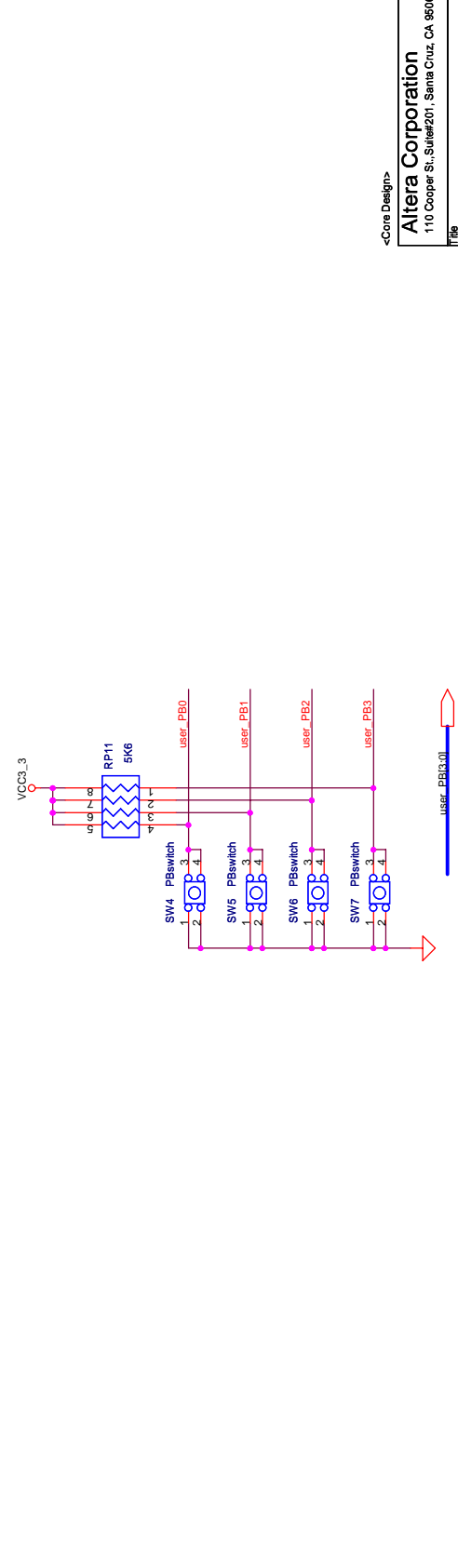
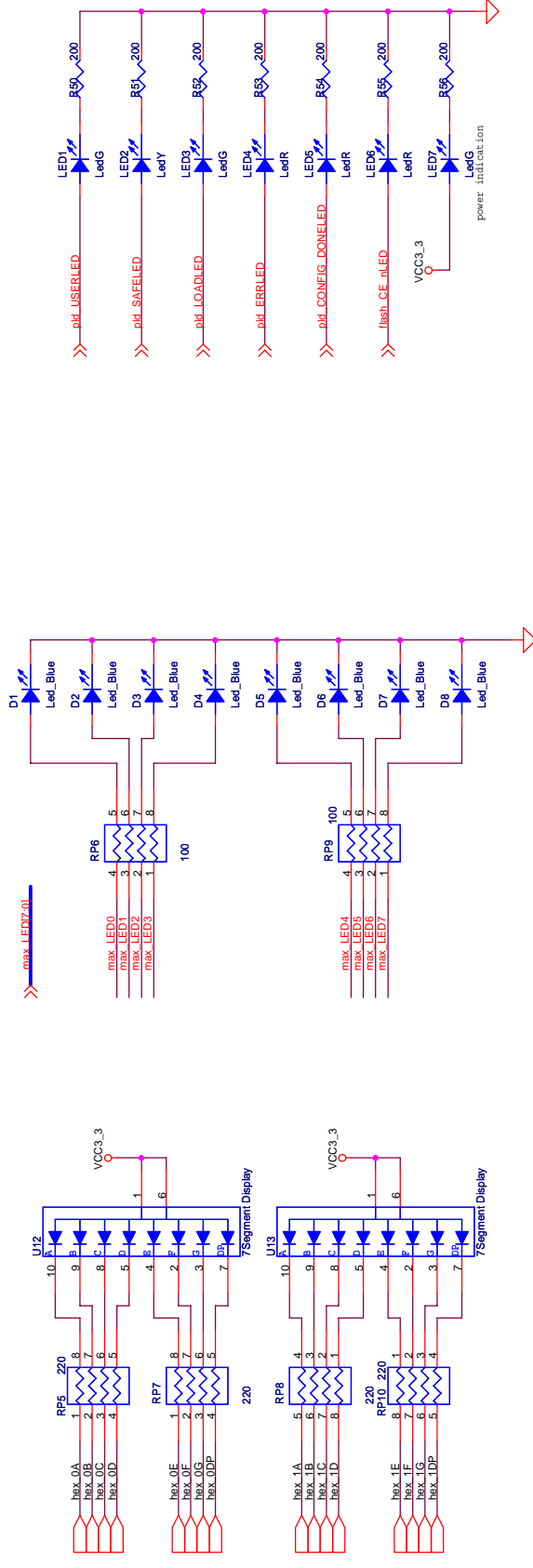
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Size	B	Document Number	P06-10217
Date	Thursday, October 14, 2004	Sheet	8 of 40
Rev		02	

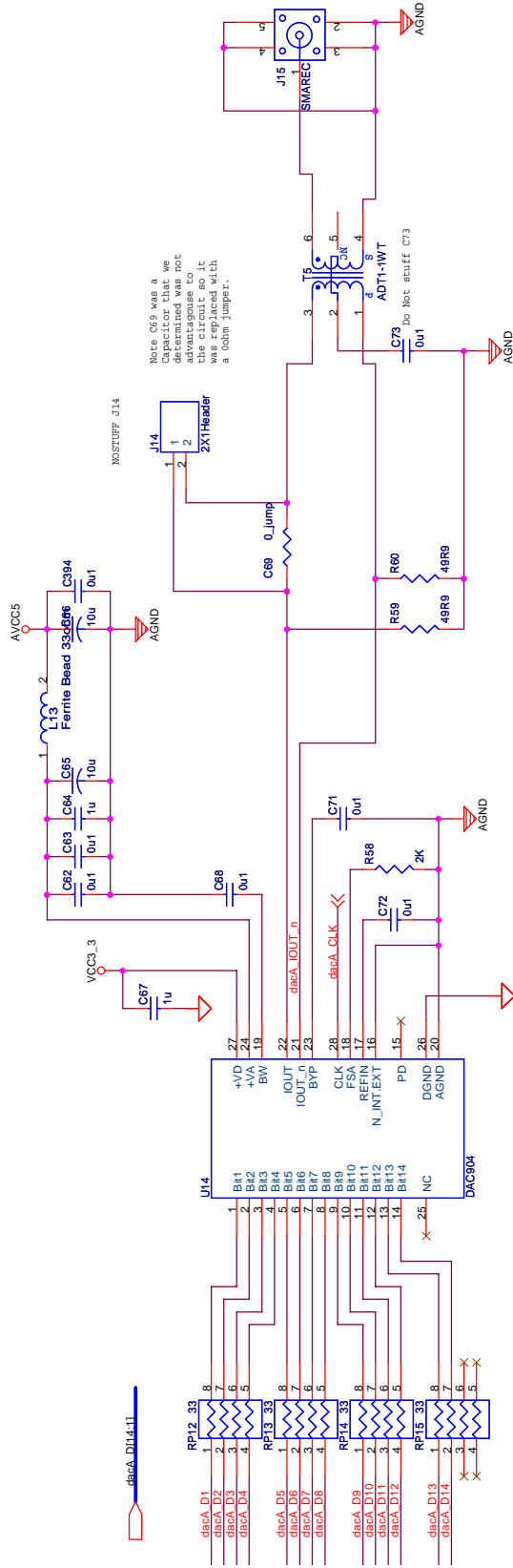






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Title	Stratix II DSP Board (Maine)
Size	Document Number
B	P06-10217
Date:	Thursday, October 14, 2004
Sheet	10 of 40
Rev	02

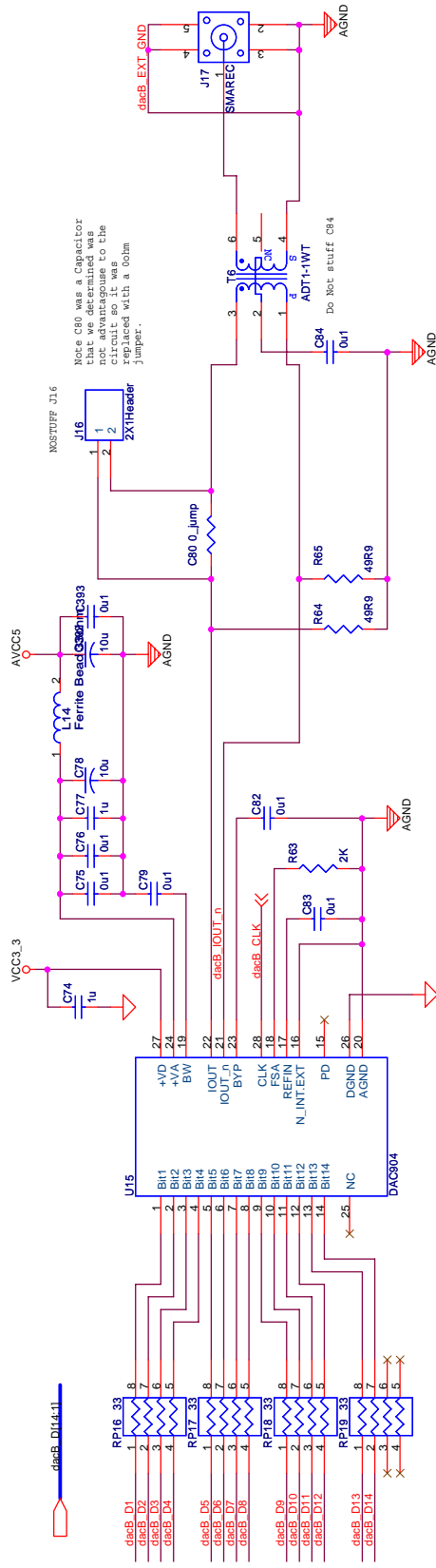


TP1 should be labeled IOUT\_n in silk screen  
 Test Header

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Title		Stratix II DSP Board (Maine)	
Size	B	Document Number	P06-10217
Date	Thursday, October 14, 2004	Sheet	11 of 40
Rev	02		



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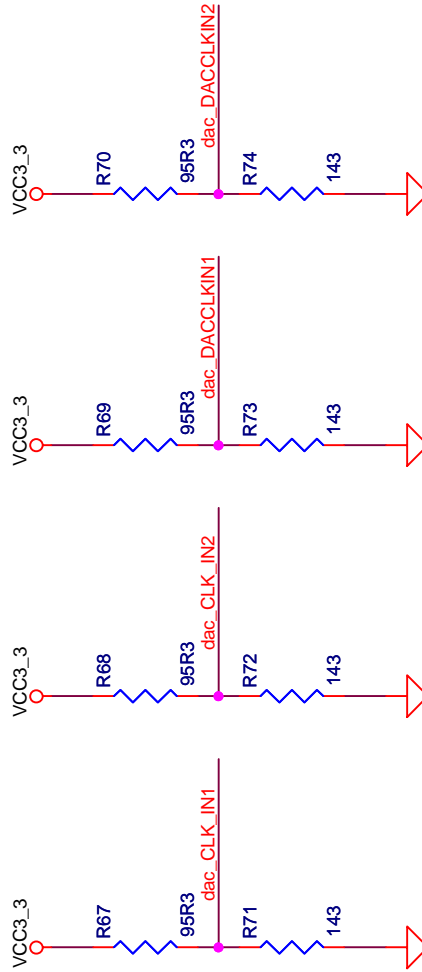
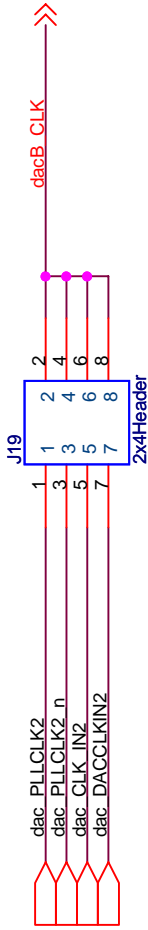
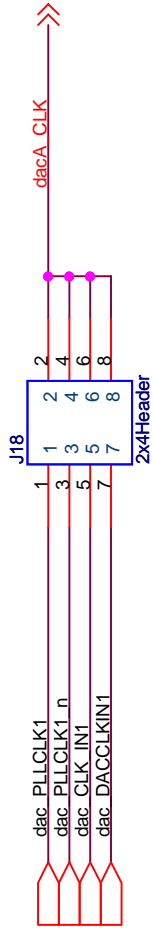
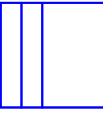
Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	
B	P06-10217	02	
Date	Thursday, October 14, 2004	Sheet	12 of 40

# DAC Clock Jumper

S3 Shunt Jumper



S4 Shunt Jumper



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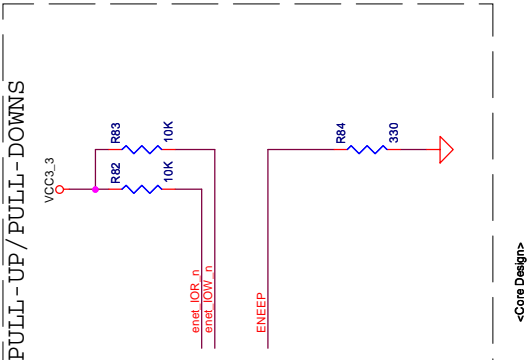
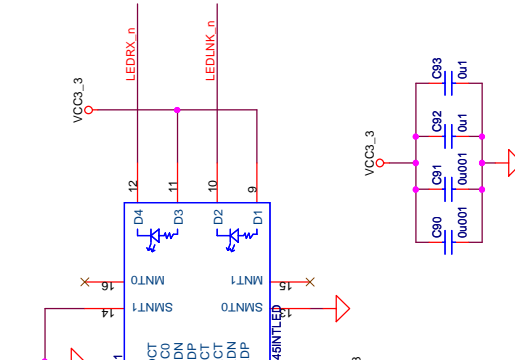
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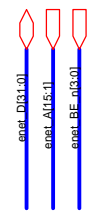
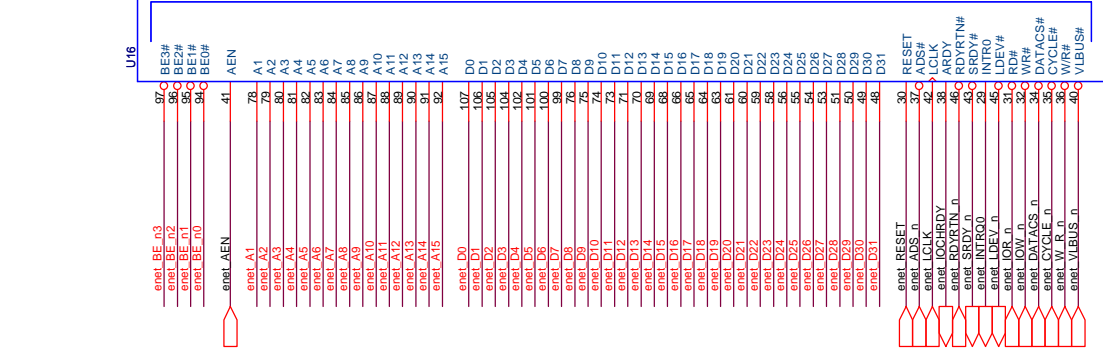
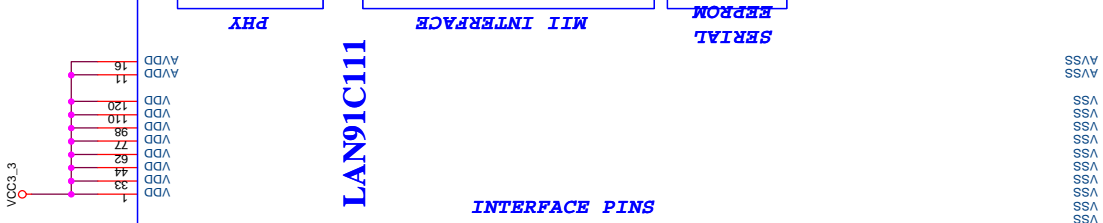
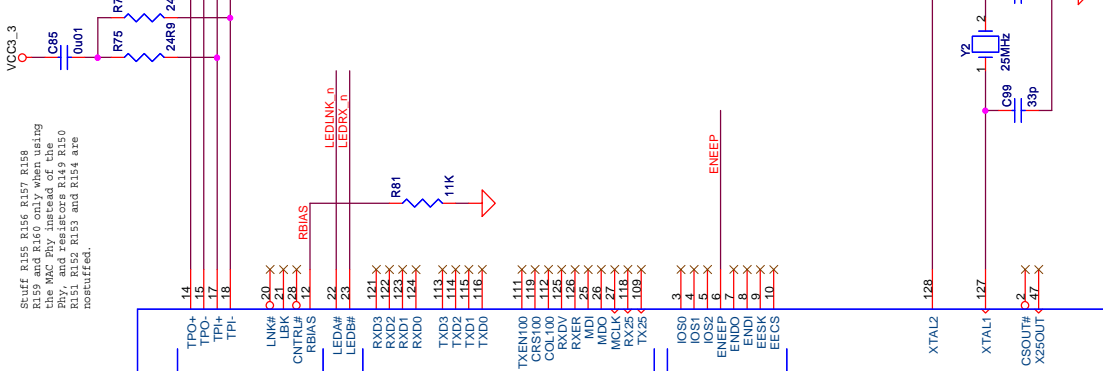
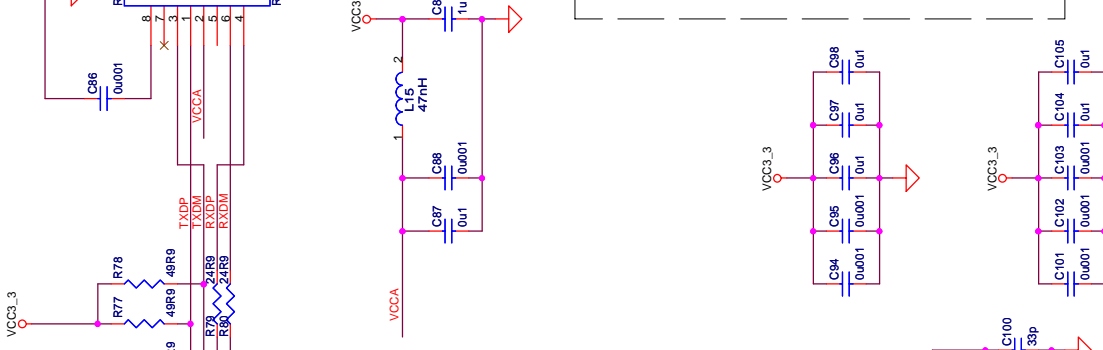
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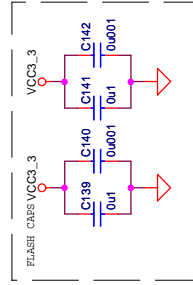
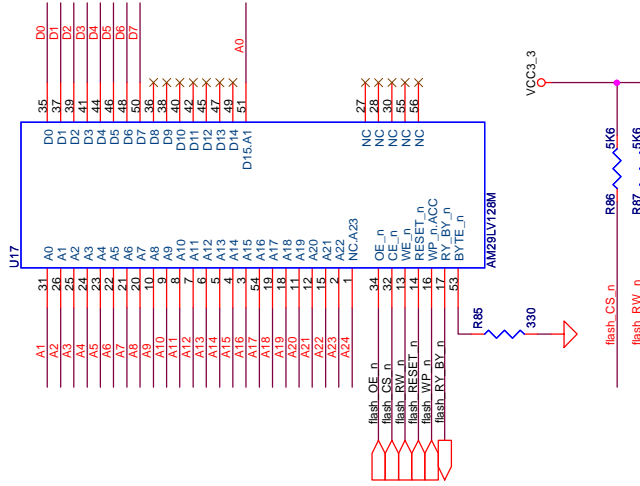
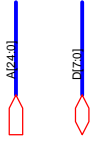
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Ethernet



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 Title: Stratix II DSP Board (Maine)  
 Size: Document Number  
 B: P06-10217  
 Date: Thursday, October 14, 2004 Sheet 14 of 40





Flash chip is 16M x 8 for 16Mbytes of flash

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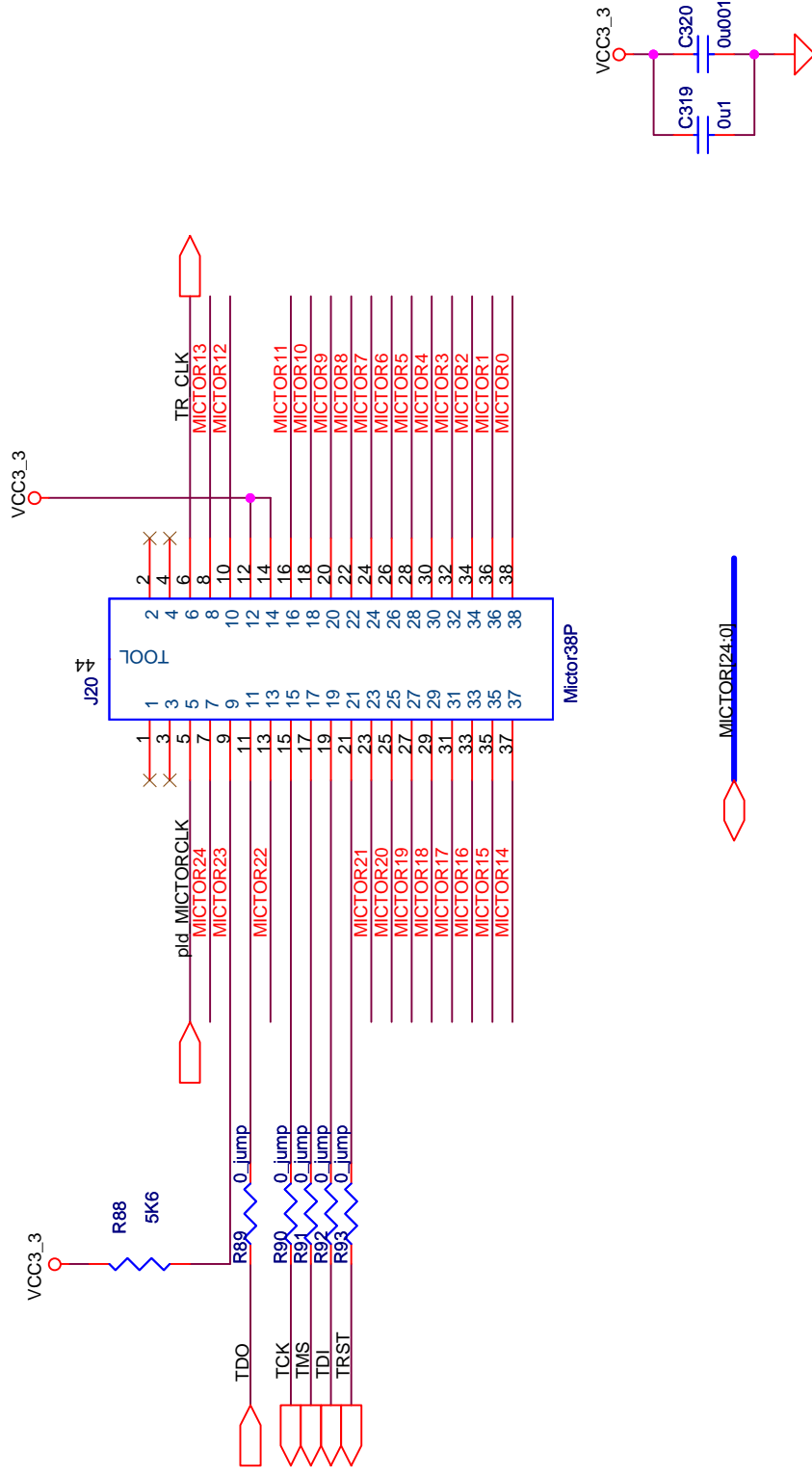
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Size: **Document Number**  
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Date: **Thursday, October 14, 2004** Sheet: **15** of **40**

Rev: **02**

# Mictor Connector



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Size

A

Document Number

P06-10217

Rev

02

Date:

Thursday, October 14, 2004

Sheet

16

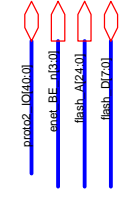
of

40



Symbol	Label	Value
flash_D0	AH30	IO.DIFFIO_RX11p
flash_D1	AH29	IO.DIFFIO_RX11p
flash_D2	AJ32	IO.DIFFIO_RX22p
flash_D3	AJ31	IO.DIFFIO_RX22n
flash_D4	AH32	IO.DIFFIO_RX33p
flash_D5	AH33	IO.DIFFIO_RX33n
flash_D6	AH32	IO.DIFFIO_RX44p
flash_D7	AH31	IO.DIFFIO_RX44n
flash_A0	AE30	IO.DIFFIO_RX5p
flash_A1	AE29	IO.DIFFIO_RX5n
flash_A2	AE28	IO.DIFFIO_RX6p
flash_A3	AE27	IO.DIFFIO_RX6n
flash_A4	AG32	IO.DIFFIO_RX7p
flash_A5	AG31	IO.DIFFIO_RX7n
flash_A6	AE32	IO.DIFFIO_RX8p
flash_A7	AE31	IO.DIFFIO_RX8n
flash_A8	AE32	IO.DIFFIO_RX9p
flash_A9	AE31	IO.DIFFIO_RX9n
flash_A10	AD32	IO.DIFFIO_RX10p
flash_A11	AD31	IO.DIFFIO_RX10n
flash_A12	AB27	IO.DIFFIO_RX11p
flash_A13	AB27	IO.DIFFIO_RX11n
flash_A14	AC32	IO.DIFFIO_RX12p
flash_A15	AC31	IO.DIFFIO_RX12n
flash_A16	AE30	IO.DIFFIO_RX13p
flash_A17	AE29	IO.DIFFIO_RX13n
flash_A18	Y29	IO.DIFFIO_RX14p
flash_A19	Y28	IO.DIFFIO_RX14n
flash_A20	AA30	IO.DIFFIO_RX15p
flash_A21	AA29	IO.DIFFIO_RX15n
flash_A22	AB32	IO.DIFFIO_RX16p
flash_A23	AB31	IO.DIFFIO_RX16n
flash_A24	Y31	IO.DIFFIO_RX17p
flash_WP_n	Y30	IO.DIFFIO_RX17n
flash_CS_n	AA32	IO.DIFFIO_RX18p
flash_CV_n	AA31	IO.DIFFIO_RX18n
flash_RW_n	W32	IO.DIFFIO_RX19p
flash_RY_BY_n	W31	IO.DIFFIO_RX19n
enel_LCLK	V31	IO.DIFFIO_RX20p
enel_LDVRTN_n	V30	IO.DIFFIO_RX20n
U32	L32	IO.CLK2pDIFFIO_RX_C1p
U31	L31	IO.CLK2nDIFFIO_RX_C1n
U30	L30	CLK3n.INPUT
U29	L29	VREFB1N.VREFB1M1
AJ30	AD28	VREFB1N0.VREFB1M0
AJ29	AG28	FPLL8CLKn.INPUT
		VREFB1N2.VREFB1M2

Symbol	Label	Value
IO.DIFFIO_TX10p	AE28	enel_CYCLE_n
IO.DIFFIO_TX10n	AE27	enel_WR_n
IO.DIFFIO_TX11p	AE26	enel_BE_i0
IO.DIFFIO_TX11n	AE25	enel_BE_r1
IO.DIFFIO_TX22p	AB24	enel_BE_i3
IO.DIFFIO_TX22n	AB23	enel_BE_r3
IO.DIFFIO_TX33p	AB24	enel_DATAGS_n
IO.DIFFIO_TX33n	AB23	enel_INTR00
IO.DIFFIO_TX44p	AC25	enel_AEN
IO.DIFFIO_TX44n	AB26	enel_D0V_n
IO.DIFFIO_TX5p	AB25	enel_OCHRDY
IO.DIFFIO_TX6p	AA25	enel_ADS_n
IO.DIFFIO_TX6n	AA24	enel_IDEV_n
IO.DIFFIO_TX8p	AA23	enel_SBDL_n
IO.DIFFIO_TX7p	AA22	enel_V1BUS_n
IO.DIFFIO_TX7n	AC27	proto2_I00
IO.DIFFIO_TX8p	AC26	proto2_O1
IO.DIFFIO_TX8n	AD27	proto2_O2
IO.DIFFIO_TX9p	AD26	proto2_O3
IO.DIFFIO_TX9n	Y23	proto2_O4
IO.DIFFIO_TX10p	Y22	proto2_O5
IO.DIFFIO_TX10n	Y24	proto2_O6
IO.DIFFIO_TX11p	Y24	proto2_O7
IO.DIFFIO_TX11n	AA27	proto2_O8
IO.DIFFIO_TX12p	Y26	proto2_O9
IO.DIFFIO_TX12n	Y27	proto2_O10
IO.DIFFIO_TX13p	Y28	proto2_O11
IO.DIFFIO_TX13n	W25	proto2_O12
IO.DIFFIO_TX14p	W24	proto2_O13
IO.DIFFIO_TX14n	W22	proto2_O14
IO.DIFFIO_TX15p	W26	proto2_O15
IO.DIFFIO_TX15n	W29	proto2_O16
IO.DIFFIO_TX16p	W28	proto2_O17
IO.DIFFIO_TX16n	Y24	proto2_O18
IO.DIFFIO_TX17p	Y23	proto2_O19
IO.DIFFIO_TX17n	Y23	proto2_O20
IO.DIFFIO_TX18p	U28	proto2_O21
IO.DIFFIO_TX18n	U28	proto2_O22
IO.DIFFIO_TX19p	U27	proto2_O23
IO.DIFFIO_TX19n	U27	proto2_O24
IO.DIFFIO_TX20p	U23	proto2_O25
IO.DIFFIO_TX20n	U22	proto2_O26
VREFB1N1.VREFB1M1	AD28	VCC3_3
VREFB1N0.VREFB1M0	W30	
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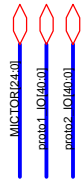
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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	
B	P06-10217	02	
Date	Thursday, October 14, 2004	Sheet	17 of 40

PLD Bank 2

U18B

pin01_00	R31	I0.DIFFIO_RX21p	T23	MICTOR0
pin01_01	R30	I0.DIFFIO_RX21n	T22	MICTOR1
pin01_02	P32	I0.DIFFIO_RX22p	T28	MICTOR2
pin01_03	P31	I0.DIFFIO_RX22n	T27	MICTOR3
pin01_04	M32	I0.DIFFIO_RX23p	R29	MICTOR4
pin01_05	M31	I0.DIFFIO_RX23n	R28	MICTOR5
pin01_06	N31	I0.DIFFIO_RX24p	R24	MICTOR6
pin01_07	N30	I0.DIFFIO_RX24n	R23	MICTOR7
pin01_08	L32	I0.DIFFIO_RX25p	R23	MICTOR8
pin01_09	L31	I0.DIFFIO_RX25n	R22	MICTOR9
pin01_10	M30	I0.DIFFIO_RX26p	R27	MICTOR10
pin01_11	N29	I0.DIFFIO_RX26n	R26	MICTOR11
pin01_12	N28	I0.DIFFIO_RX28p	P25	MICTOR12
pin01_13	N28	I0.DIFFIO_RX27p	P24	MICTOR13
pin01_14	L30	I0.DIFFIO_RX27n	P27	MICTOR14
pin01_15	L29	I0.DIFFIO_RX28p	P26	MICTOR15
pin01_16	K32	I0.DIFFIO_RX28n	P29	MICTOR16
pin01_17	K31	I0.DIFFIO_RX29p	P28	MICTOR17
pin01_18	K30	I0.DIFFIO_RX29n	N27	MICTOR18
pin01_19	K29	I0.DIFFIO_RX30p	N26	MICTOR19
pin01_20	J32	I0.DIFFIO_RX30n	N25	MICTOR20
pin01_21	H31	I0.DIFFIO_RX31p	M27	MICTOR21
pin01_22	H30	I0.DIFFIO_RX31n	M26	MICTOR22
pin01_23	H31	I0.DIFFIO_RX32p	M27	MICTOR23
pin01_24	G32	I0.DIFFIO_RX32n	M26	MICTOR24
pin01_25	G31	I0.DIFFIO_RX33p	N23	MICTOR25
pin01_26	F32	I0.DIFFIO_RX33n	N22	MICTOR26
pin01_27	F31	I0.DIFFIO_RX34p	M24	TR_CLK_3
pin01_28	E32	I0.DIFFIO_RX34n	M24	pin01_CARDSEL_0
pin01_29	E31	I0.DIFFIO_RX35p	L26	pin01_CARDSEL_n
pin01_30	H30	I0.DIFFIO_RX35n	L25	pin02_D26
pin01_31	H29	I0.DIFFIO_RX36p	M23	pin02_D27
pin01_32	H29	I0.DIFFIO_RX36n	M22	pin02_D28
pin01_33	G30	I0.DIFFIO_RX37p	K27	pin02_D29
pin01_34	F30	I0.DIFFIO_RX37n	L24	pin02_D30
pin01_35	E30	I0.DIFFIO_RX38p	L23	pin02_D31
pin01_36	D31	I0.DIFFIO_RX38n	J27	pin02_D32
pin01_37	D30	I0.DIFFIO_RX39p	J27	pin02_D33
pin01_38	D29	I0.DIFFIO_RX39n	H28	pin02_D34
pin01_39	D31	I0.DIFFIO_RX40p	H27	pin02_D35
pin01_40	D30	I0.DIFFIO_RX40n	K25	pin02_D37
pin01_CLKOUT	T32	I0.CLK0p/DIFFIO_RX_C0p	K24	pin02_D38
pin02_CLKOUT	T31	I0.CLK0n/DIFFIO_RX_C0n	K24	pin02_D38
	D30	CLK0n.INPUT	F28	VCC3_3
	D29	CLK0p.INPUT	J28	VREFB20.VREFB20
		FFL/CLK0n.INPUT	P30	VREFB22.VREFB22
		FFL/CLK0p.INPUT		



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Size	Document Number	Rev
B	P06-10217	02

Date: Thursday, October 14, 2004 Sheet 18 of 40

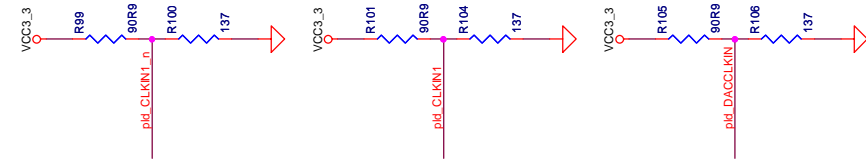
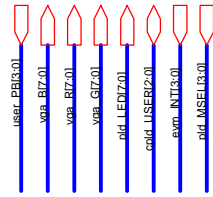


PLD Bank 4

U18D

pin_LED0	B4	IO_D00T0	K13	DIR1
pin_LED1	D5	IO_D00T1	H14	DD1
pin_LED2	E3	IO_D00T2	K16	DR1
pin_LED3	F3	IO_D00T3	L17	TXD1
pin_LED4	A5	IO_D00T4	K15	CTS1
pin_LED5	D8	IO_D01T0	L16	RXD1
pin_LED6	C8	IO_D01T1	L15	RTS1
pin_LED7	A6	IO_D01T2	K12	evm JACK
via_B0	B7	IO_D02T0	H13	evm INUM0
via_B1	E7	IO_D02T1	L12	evm CNT10
via_B2	E6	IO_D02T2	H12	evm STAT0
via_B3	A7	IO_D02T3	H12	evm DMAC0
via_B4	C3	IO_D03T0	L11	evm CLKRES0
via_B5	C8	IO_D03T1	H11	evm INT0
via_B6	A8	IO_D03T2	K14	evm INT1
via_B7	A8	IO_D03T3	H14	RT08
via_R0	D8	IO_D04T0	J14	RT08
via_R1	E8	IO_D04T1	J14	USER_PB1
via_R2	F8	IO_D04T2	L13	USER_PB2
via_R3	F10	IO_D04T3	L13	USER_PB3
via_R4	A10	IO_D04T3	J13	USER_PB3
via_R5	B10	IO_D05T0	A16	pin_CLKIN1
via_R6	D10	IO_D05T1	E16	pin_DACCLKIN
via_R7	D11	IO_D05T2	F16	pin_DACCLKIN
via_G0	E11	IO_D05T3	C2	VCC3_3
via_G1	G10	IO_D06T0	D8	pin_CLKIN1
via_G2	G11	IO_D06T1	E16	pin_DACCLKIN
via_G3	G12	IO_D06T2	F16	pin_DACCLKIN
via_G4	A12	IO_D06T3	C2	VCC3_3
via_G5	A12	IO_D07T0	C14	pin_CLKIN1
via_G6	B11	IO_D07T1	D8	pin_CLKIN1
via_G7	A12	IO_D07T2	F16	pin_DACCLKIN
via_G8	A12	IO_D07T3	F16	pin_DACCLKIN
via_CLOCK	E13	IO_D08T0	B2	pin_MSEL0
via_SYNC_n	F13	IO_D08T1	F6	pin_MSEL1
via_HSYNC	G13	IO_D08T2	J10	pin_MSEL2
via_VSYNC	F15	IO_D08T3	H10	pin_MSEL3
pin_USER0	B14	IO_D08T3	B2	pin_MSEL0
pin_USER1	D14	IO_D09T0	F6	pin_MSEL1
pin_USER2	D13	IO_D09T1	J10	pin_MSEL2
pin_USER3	D13	IO_D09T2	H10	pin_MSEL3
pin_USER4	A14	IO_D09T3	H10	pin_MSEL3
hex_0A	C4	IO_D09T3	H10	pin_MSEL3
hex_0B	C5	IO_D09T3	H10	pin_MSEL3
hex_0C	B5	IO_D09T3	H10	pin_MSEL3
hex_0D	B6	IO_D09T3	H10	pin_MSEL3
hex_0E	C7	IO_D09T3	H10	pin_MSEL3
hex_0F	C7	IO_D09T3	H10	pin_MSEL3
hex_0G	B8	IO_D09T3	H10	pin_MSEL3
hex_0DP	B8	IO_D09T3	H10	pin_MSEL3
hex_1A	F8	IO_D09T3	H10	pin_MSEL3
hex_1B	F8	IO_D09T3	H10	pin_MSEL3
hex_1C	G10	IO_D09T3	H10	pin_MSEL3
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hex_1DP	G12	IO_D09T3	H10	pin_MSEL3
pin_RECONFREQ_n	F14	IO_D09T3	H10	pin_MSEL3
evm_ACE3_n	F14	IO_D09T3	H10	pin_MSEL3
evm_INT2	G13	IO_D09T3	H10	pin_MSEL3
evm_INT3	B13	IO_D09T3	H10	pin_MSEL3

EP2560\_1020F5GA



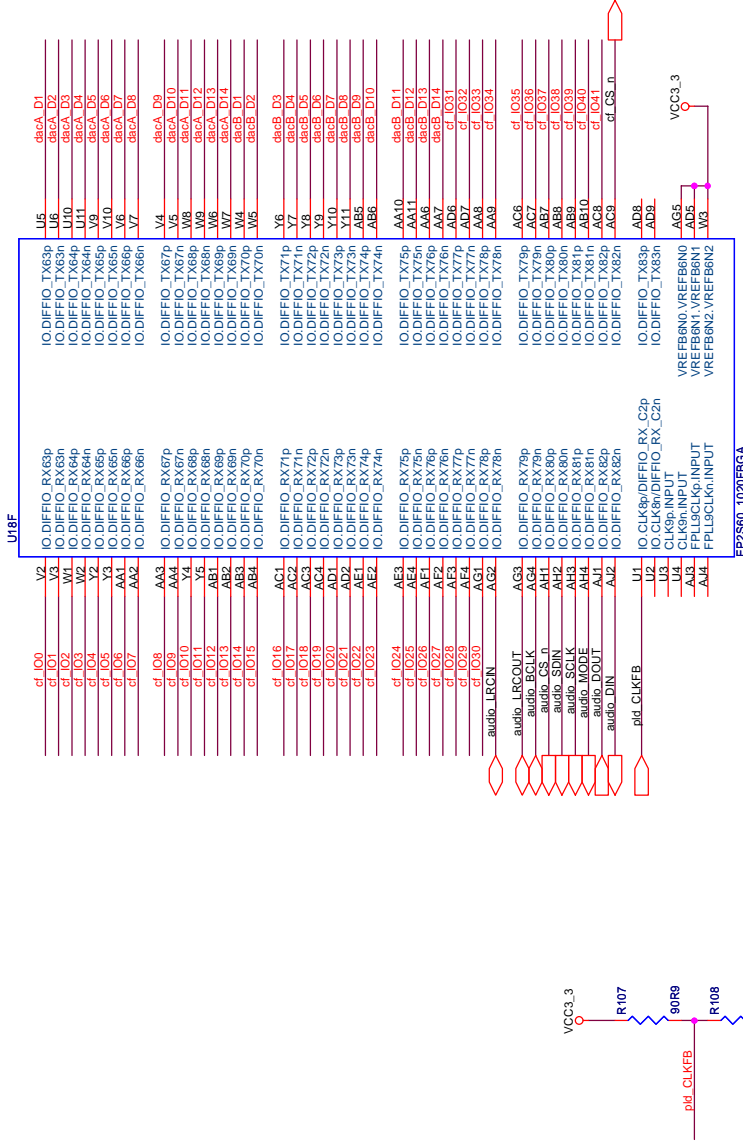
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**Altera Corporation**  
 110 Cooper St., Suite#201, Santa Cruz, CA 95060

Title: Strata II DSP Board (Maine)  
 Document Number: P06-10217  
 Date: Thursday, October 14, 2004 Sheet 20 of 40

PLD Bank 5

Pin	Signal	IO Type	IO Type
ad4A_D0	D1	IO.DIFFIO_RX43p	IO.DIFFIO_RX43p
ad4A_D1	D2	IO.DIFFIO_RX43n	IO.DIFFIO_RX43n
ad4A_D2	E3	IO.DIFFIO_RX44p	IO.DIFFIO_RX44p
ad4A_D3	E4	IO.DIFFIO_RX44n	IO.DIFFIO_RX44n
ad4A_D4	E1	IO.DIFFIO_RX45p	IO.DIFFIO_RX45p
ad4A_D5	E2	IO.DIFFIO_RX45n	IO.DIFFIO_RX45n
ad4A_D6	F4	IO.DIFFIO_RX46p	IO.DIFFIO_RX46p
ad4A_D7	F4	IO.DIFFIO_RX46n	IO.DIFFIO_RX46n
ad4A_D8	F1	IO.DIFFIO_RX47p	IO.DIFFIO_RX47p
ad4A_D9	F2	IO.DIFFIO_RX47n	IO.DIFFIO_RX47n
ad4A_D10	G3	IO.DIFFIO_RX48p	IO.DIFFIO_RX48p
ad4A_D11	G4	IO.DIFFIO_RX48n	IO.DIFFIO_RX48n
ad4B_D1	G2	IO.DIFFIO_RX49p	IO.DIFFIO_RX49p
ad4B_D2	J3	IO.DIFFIO_RX49n	IO.DIFFIO_RX49n
ad4B_D3	J4	IO.DIFFIO_RX50p	IO.DIFFIO_RX50p
ad4B_D4	J4	IO.DIFFIO_RX50n	IO.DIFFIO_RX50n
ad4B_D5	H1	IO.DIFFIO_RX51p	IO.DIFFIO_RX51p
ad4B_D6	H2	IO.DIFFIO_RX51n	IO.DIFFIO_RX51n
ad4B_D7	J1	IO.DIFFIO_RX52p	IO.DIFFIO_RX52p
ad4B_D8	J2	IO.DIFFIO_RX52n	IO.DIFFIO_RX52n
ad4B_D9	K3	IO.DIFFIO_RX53p	IO.DIFFIO_RX53p
ad4B_D10	K4	IO.DIFFIO_RX53n	IO.DIFFIO_RX53n
ad4B_D11	K2	IO.DIFFIO_RX54p	IO.DIFFIO_RX54p
ad4B_D12	K2	IO.DIFFIO_RX54n	IO.DIFFIO_RX54n
ad4_D0	L3	IO.DIFFIO_RX55p	IO.DIFFIO_RX55p
ad4_D1	L4	IO.DIFFIO_RX55n	IO.DIFFIO_RX55n
ad4_D2	N5	IO.DIFFIO_RX56p	IO.DIFFIO_RX56p
ad4_D3	N6	IO.DIFFIO_RX56n	IO.DIFFIO_RX56n
ad4_D4	M3	IO.DIFFIO_RX57p	IO.DIFFIO_RX57p
ad4_D5	M4	IO.DIFFIO_RX57n	IO.DIFFIO_RX57n
ad4_D6	L1	IO.DIFFIO_RX58p	IO.DIFFIO_RX58p
ad4_D7	L2	IO.DIFFIO_RX58n	IO.DIFFIO_RX58n
ad4_D8	N2	IO.DIFFIO_RX59p	IO.DIFFIO_RX59p
ad4_D9	N3	IO.DIFFIO_RX59n	IO.DIFFIO_RX59n
ad4_D10	M1	IO.DIFFIO_RX60p	IO.DIFFIO_RX60p
ad4_D11	M2	IO.DIFFIO_RX60n	IO.DIFFIO_RX60n
ad4_D12	R2	IO.DIFFIO_RX61p	IO.DIFFIO_RX61p
ad4_D13	R1	IO.DIFFIO_RX61n	IO.DIFFIO_RX61n
ad4_D14	P1	IO.DIFFIO_RX62p	IO.DIFFIO_RX62p
ad4_D15	P2	IO.DIFFIO_RX62n	IO.DIFFIO_RX62n
T1	IO.CLK10p/DIFFIO_RX_C3p		
T2	IO.CLK10n/DIFFIO_RX_C3n		
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D3	CLK11n.INPUT		
D4	FPLL10CLKn.INPUT		
D4	FPLL10CLKp.INPUT		
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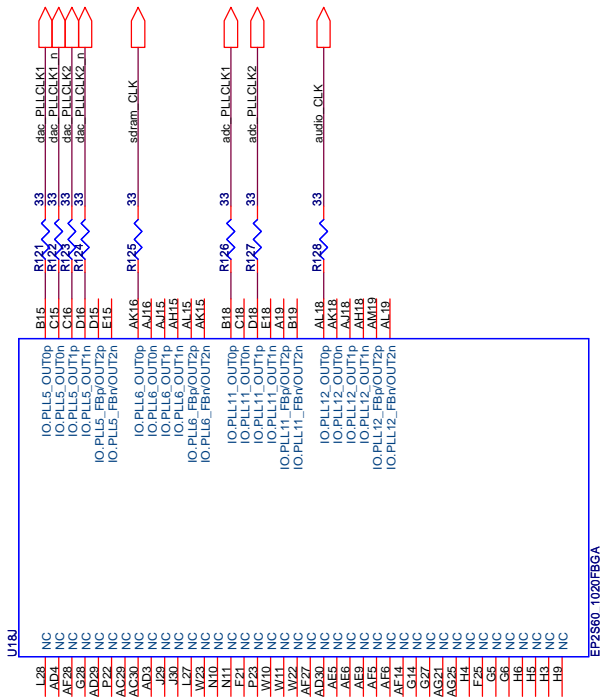
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Date	Thursday, October 14, 2004	Sheet	22	of	40
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Title: Strata II DSP Board (Maine)

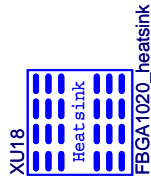
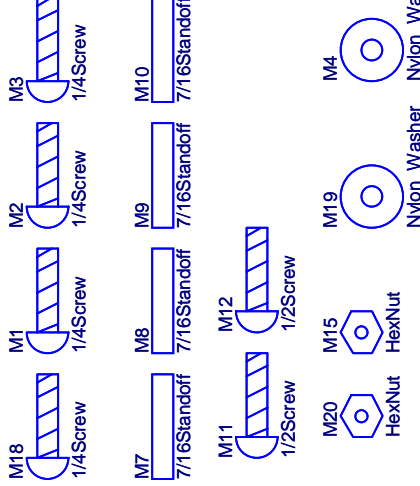
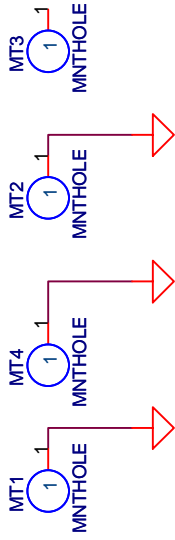
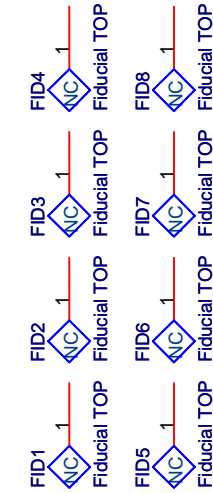
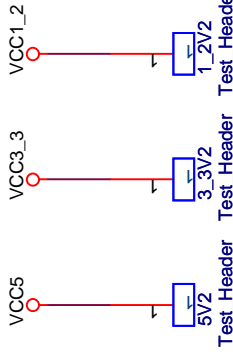
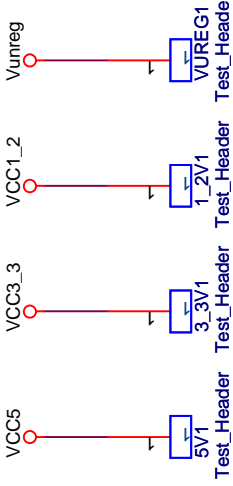
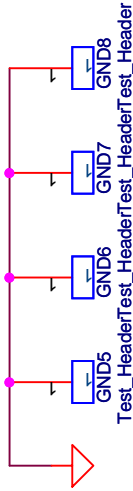
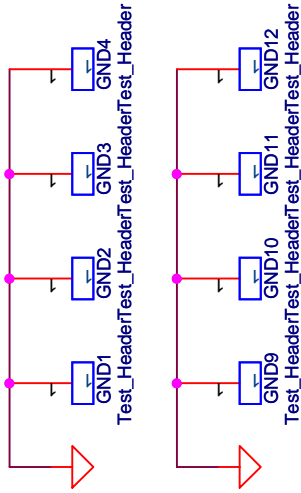
Size: B Document Number: P06-10217

Rev: 02 Date: Thursday, October 14, 2004 Sheet 26 of 40





# Reset and Test headers



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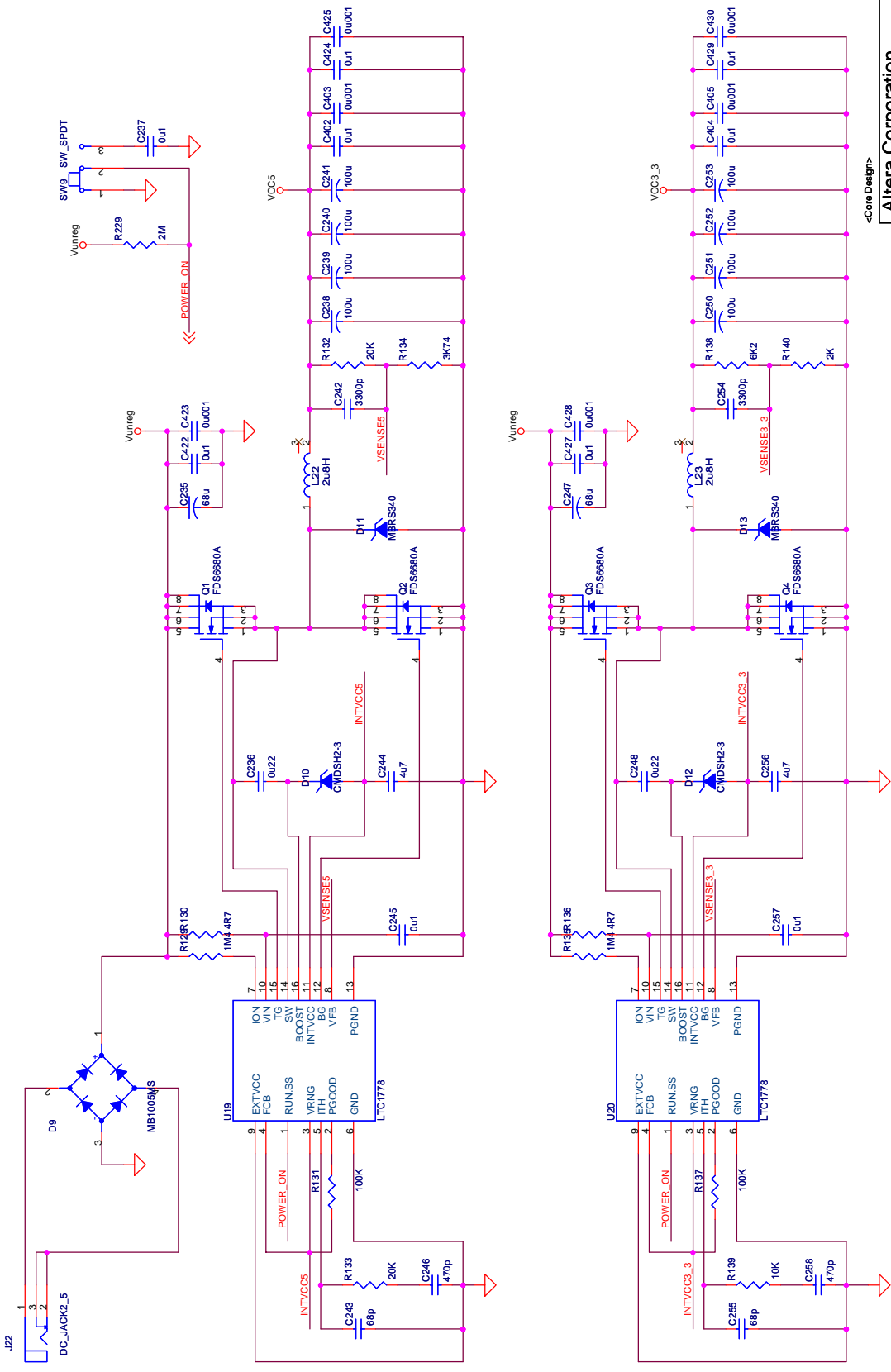
Title Stratrix II DSP Board (Maine)

Size Document Number  
A P06-10217

Rev 02

Date: Thursday, October 14, 2004

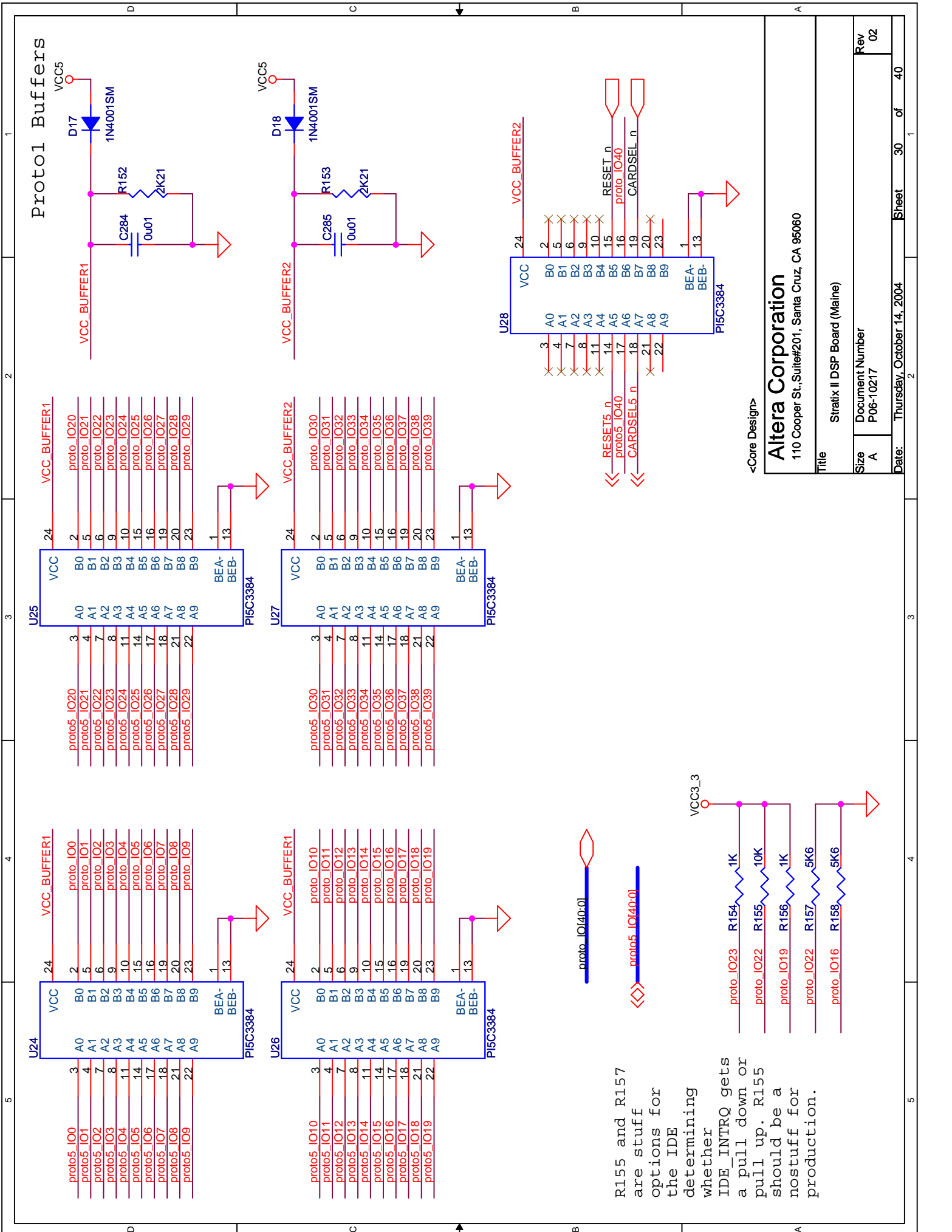
Sheet 28 of 40



<Core Design>

**Altera Corporation**  
 110 Cooper St., Suite#201, Santa Cruz, CA 95060

Title		Stratix II DSP Board (Maine)	
Size	B	Document Number	P06-10217
Date	Thursday, October 14, 2004	Sheet	28 of 40
Rev	02		



# Proto1 Buffers

U24

3	proto5_IO0	24	VCC_BUFFER1
4	proto5_IO1	2	B0
5	proto5_IO2	5	B1
6	proto5_IO3	6	B2
7	proto5_IO4	9	B3
8	proto5_IO5	10	B4
11	proto5_IO6	15	B5
14	proto5_IO7	16	B6
17	proto5_IO8	19	B7
18	proto5_IO9	20	B8
21		21	B9
22		23	B9
13	BEA-	1	BEA-
1	BEB-	13	BEB-

P15C3384

U25

3	proto5_IO20	24	VCC_BUFFER1
4	proto5_IO21	2	B0
5	proto5_IO22	5	B1
6	proto5_IO23	6	B2
7	proto5_IO24	9	B3
8	proto5_IO25	10	B4
11	proto5_IO26	15	B5
14	proto5_IO27	16	B6
17	proto5_IO28	19	B7
18	proto5_IO29	20	B8
21		21	B9
22		23	B9
13	BEA-	1	BEA-
1	BEB-	13	BEB-

P15C3384

U26

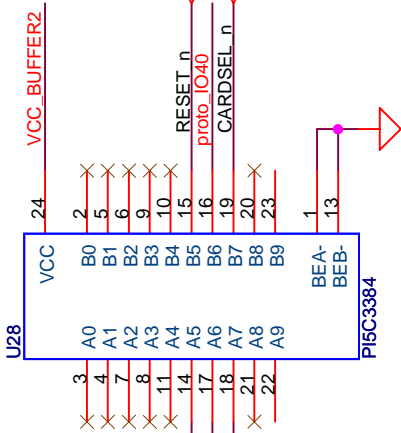
3	proto5_IO10	24	VCC_BUFFER1
4	proto5_IO11	2	B0
7	proto5_IO12	5	B1
8	proto5_IO13	6	B2
11	proto5_IO14	9	B3
14	proto5_IO15	10	B4
17	proto5_IO16	15	B5
18	proto5_IO17	16	B6
21	proto5_IO18	19	B7
22	proto5_IO19	20	B8
13	BEA-	1	BEA-
1	BEB-	13	BEB-

P15C3384

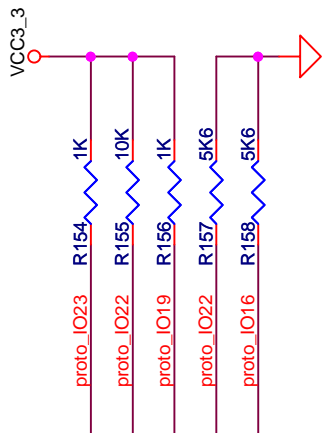
U27

3	proto5_IO30	24	VCC_BUFFER2
4	proto5_IO31	2	B0
7	proto5_IO32	5	B1
8	proto5_IO33	6	B2
11	proto5_IO34	9	B3
14	proto5_IO35	10	B4
17	proto5_IO36	15	B5
18	proto5_IO37	16	B6
21	proto5_IO38	19	B7
22	proto5_IO39	20	B8
13	BEA-	1	BEA-
1	BEB-	13	BEB-

P15C3384



R155 and R157 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R155 should be a nostuff for production.

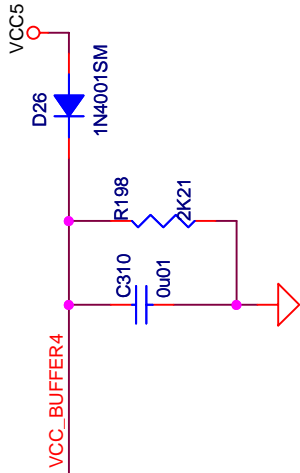
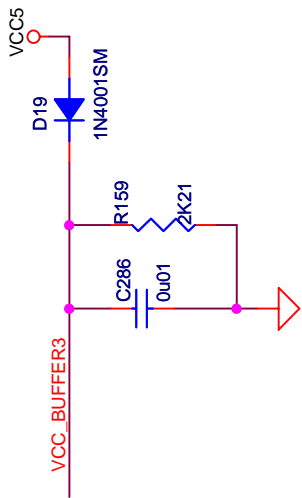
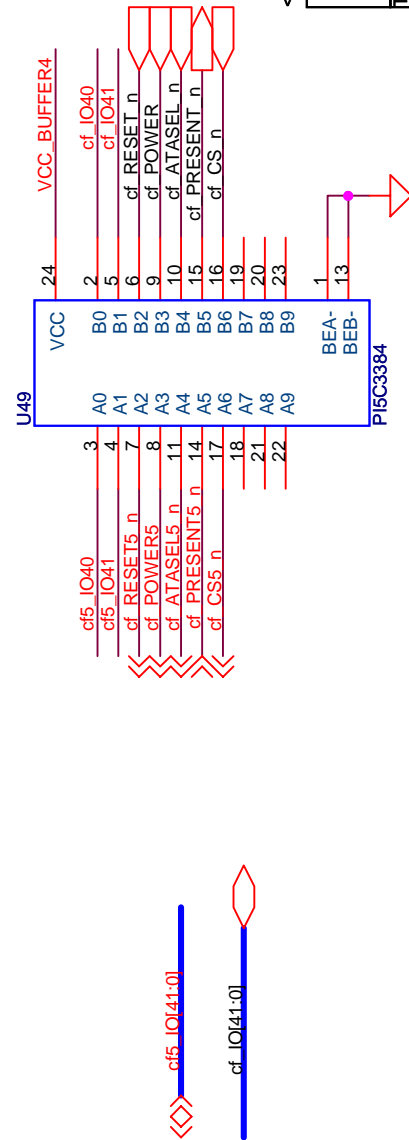
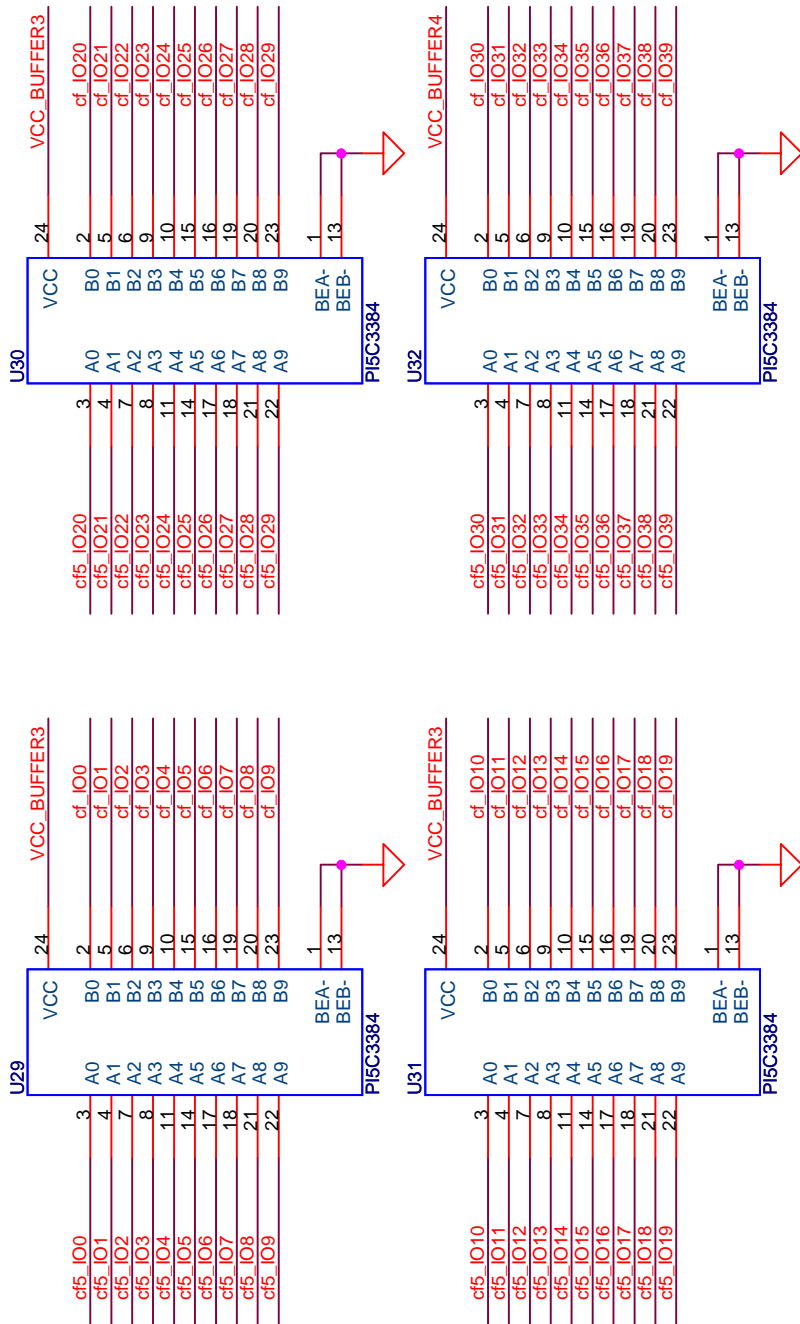


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110 Cooper St., Suite#201, Santa Cruz, CA 95060

Title	
Stratix II DSP Board (Maine)	
Size	Document Number
A	P06-10217
Date:	Thursday, October 14, 2004
Sheet	30 of 40
Rev	02

# Proto1 Buffers



<Core Design>

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110 Cooper St., Suite#201, Santa Cruz, CA 95060

Title

Stratix II DSP Board (Maine)

Size A Document Number

P06-10217

Rev

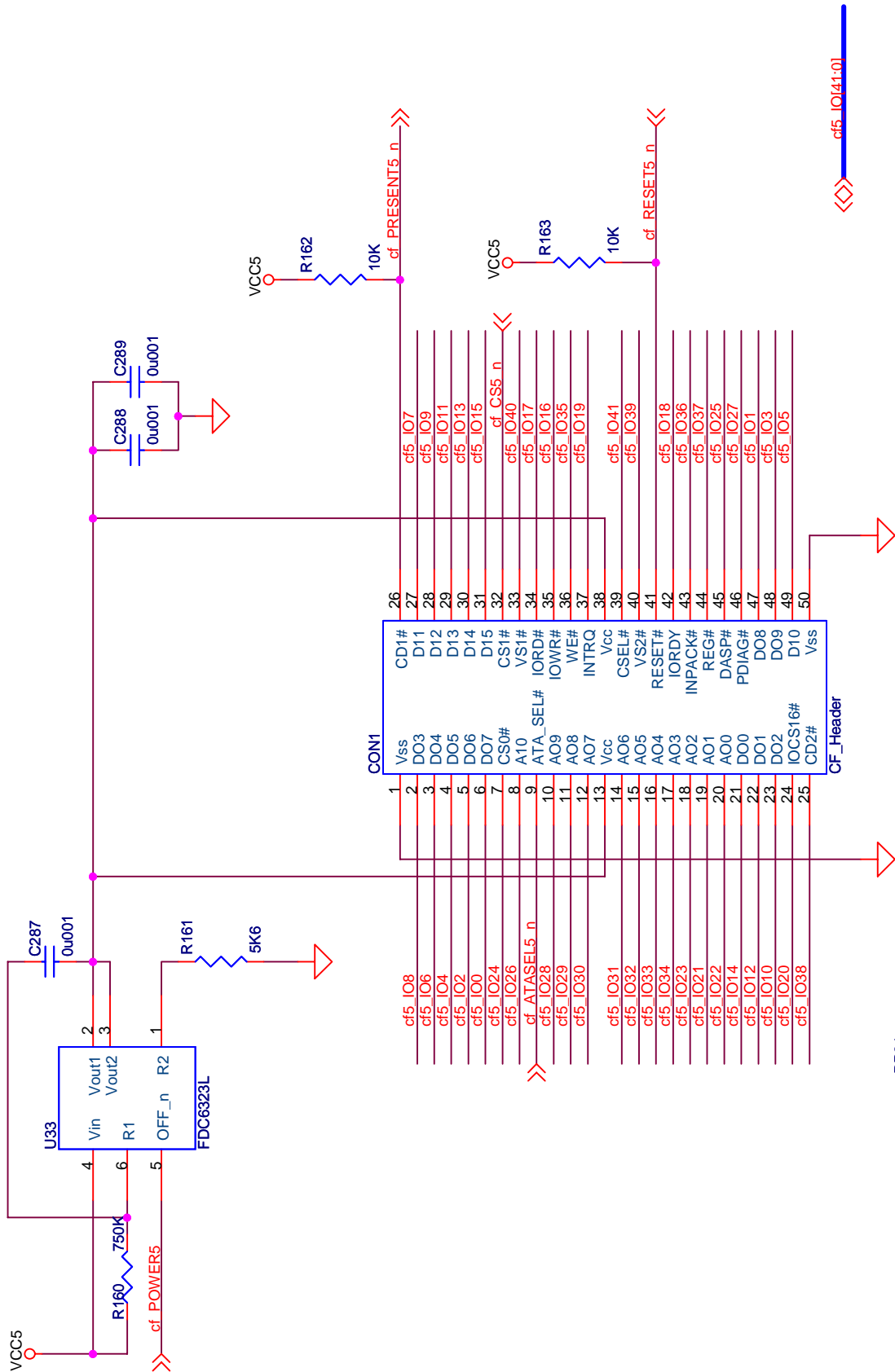
02

Date: Thursday, October 14, 2004

Sheet

31 of 40

# Compact Flash Socket

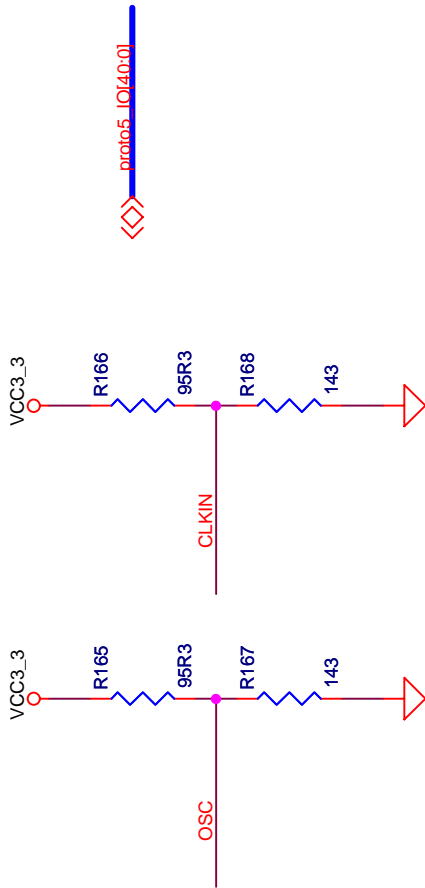
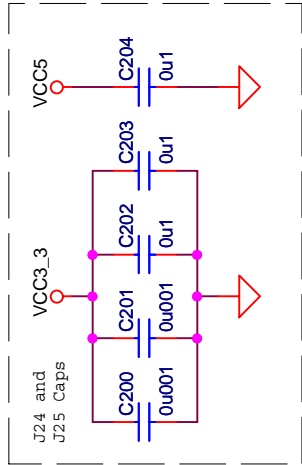
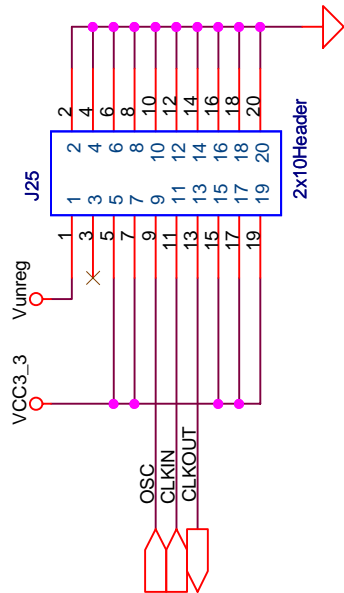
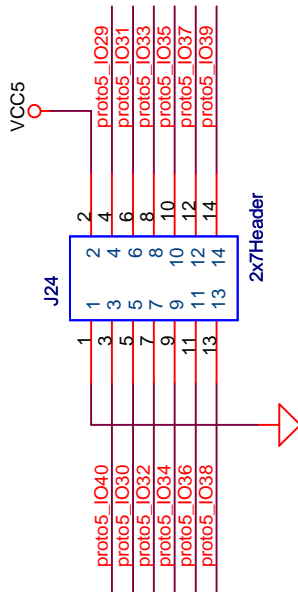
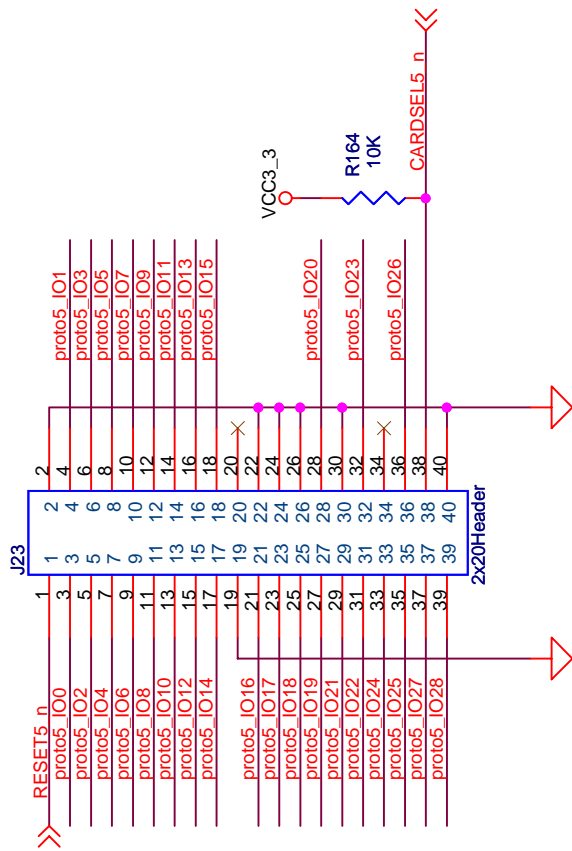


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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	
A	P06-10217	02	
Date:	Thursday, October 14, 2004	Sheet	32 of 40

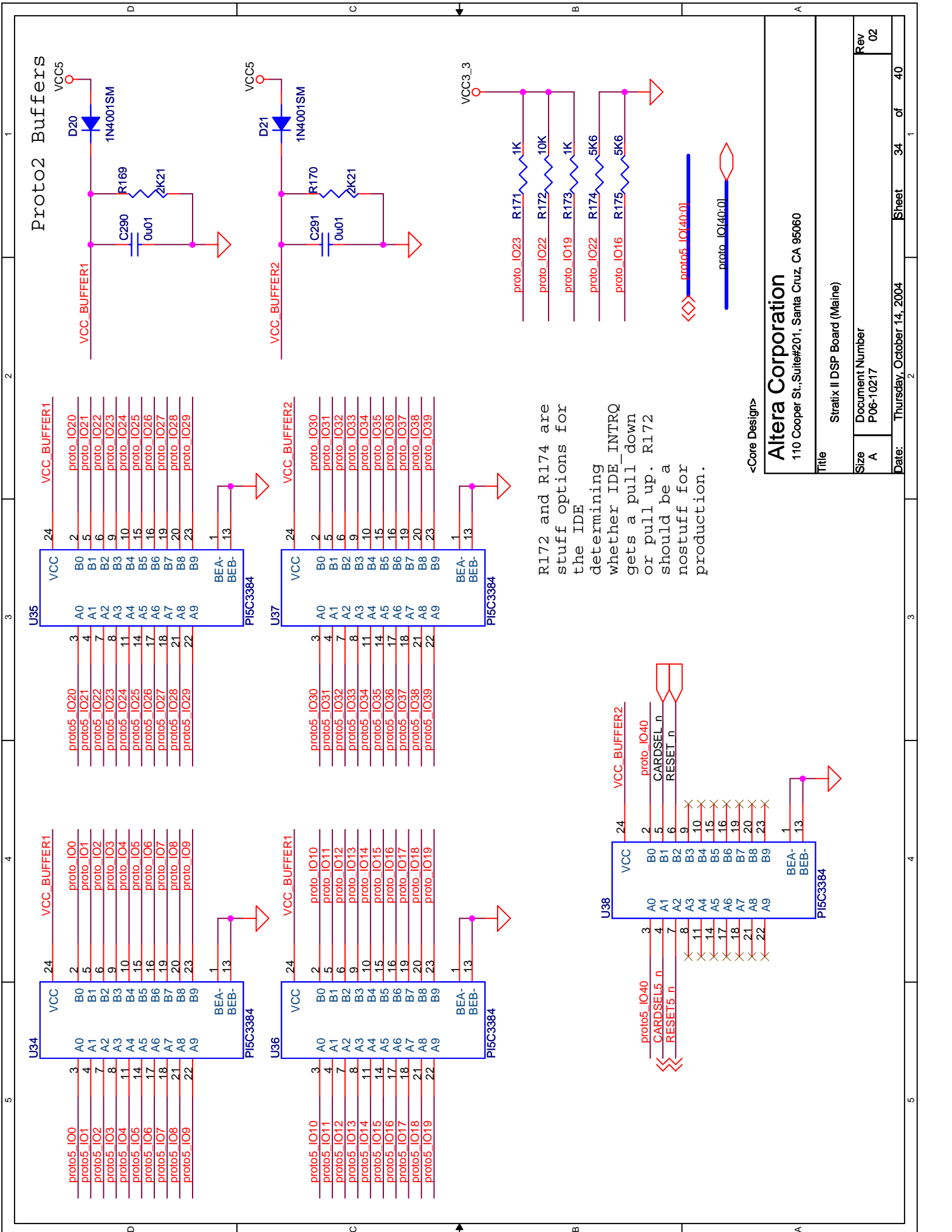




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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	02
A	P06-10217		
Date:	Thursday, October 14, 2004	Sheet	33 of 40



### Proto2 Buffers

R172 and R174 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R172 should be a nostuff for production.

<Core Design>

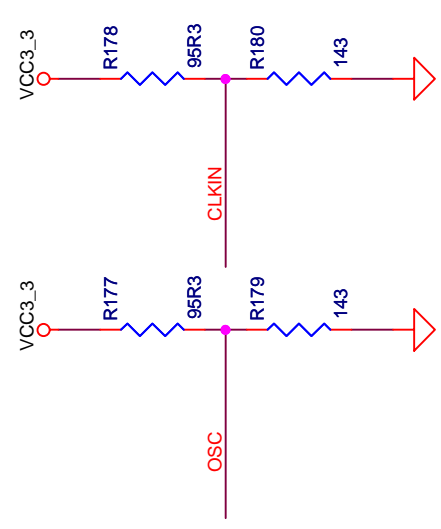
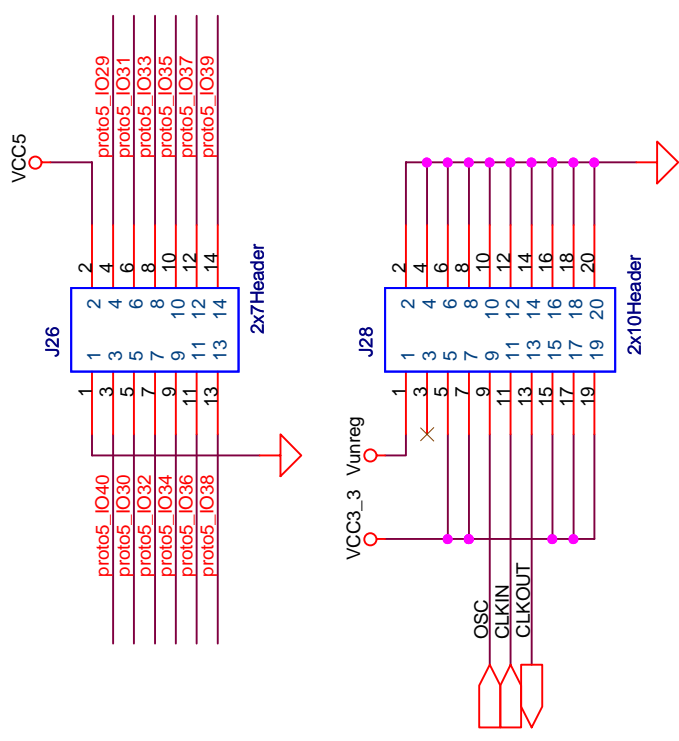
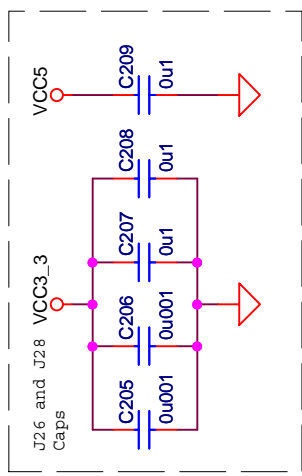
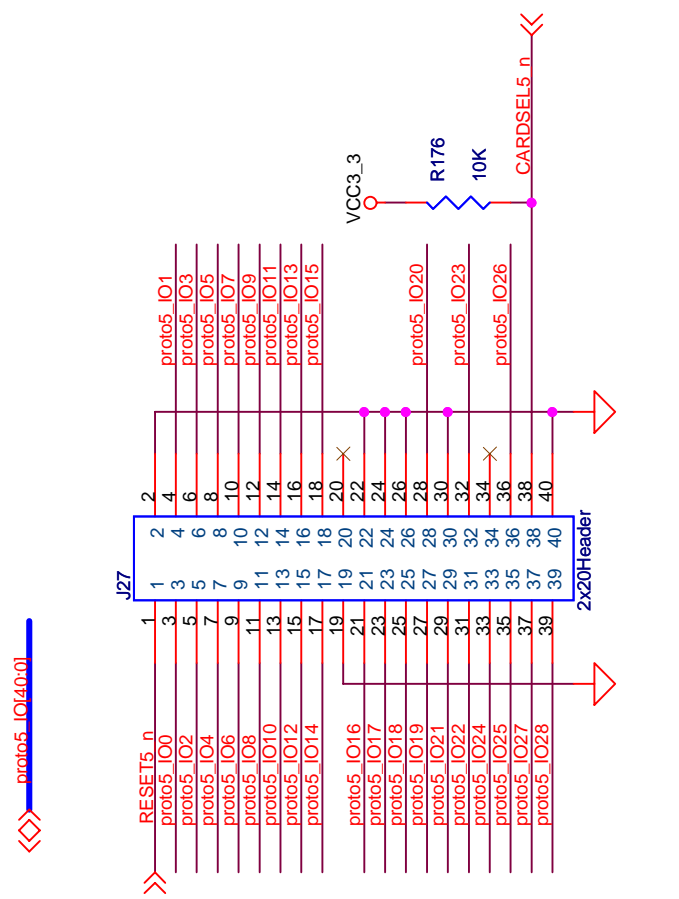
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Title: StratiX II DSP Board (Maine)

Size	Document Number	Rev
A	P06-10217	02

Date: Thursday, October 14, 2004 Sheet 34 of 40

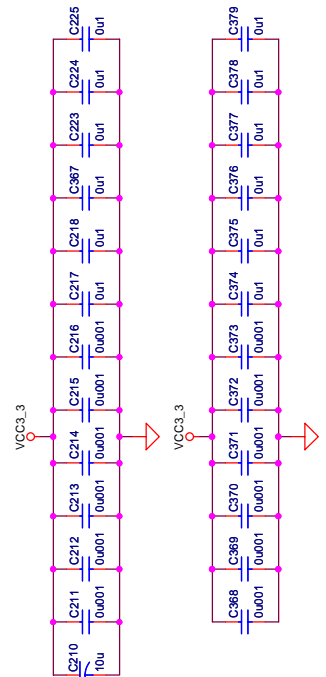
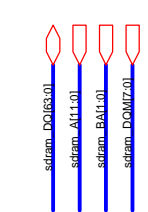
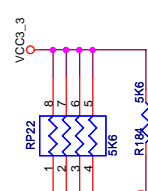
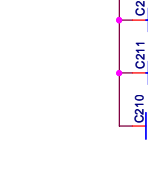
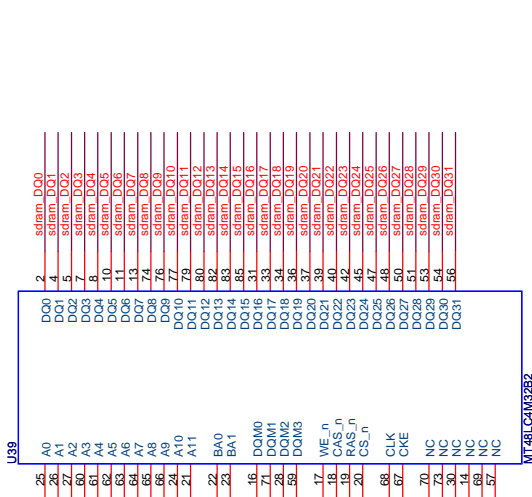
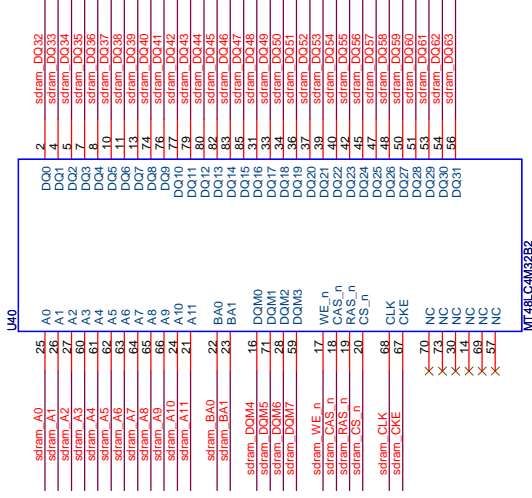
# Proto2 Headers



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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	02
A	P06-10217		
Date:	Thursday, October 14, 2004	Sheet	35 of 40



<Core Design>

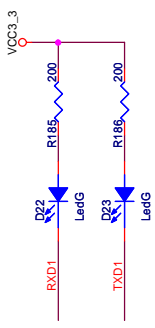
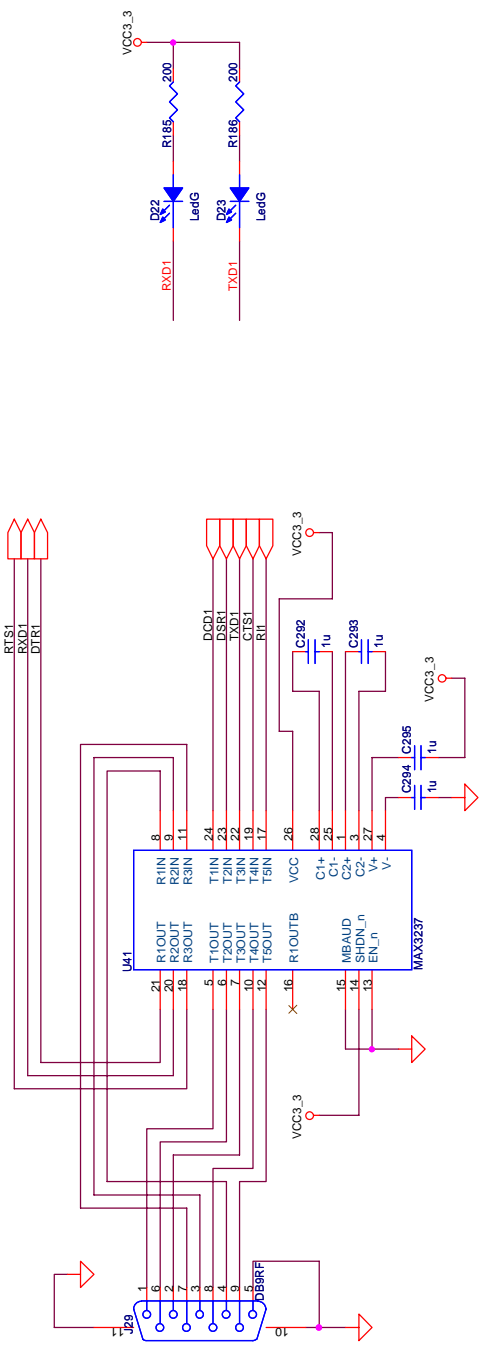
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Title: Stratix II DSP Board (Maine)

Size	Document Number	Rev
B	P06-10217	02

Date: Thursday, October 14, 2004 Sheet 36 of 40

Serial Ports

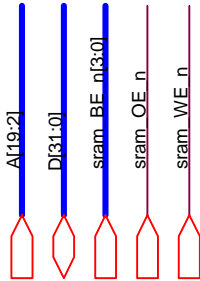
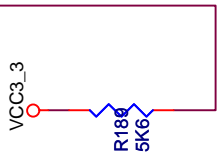
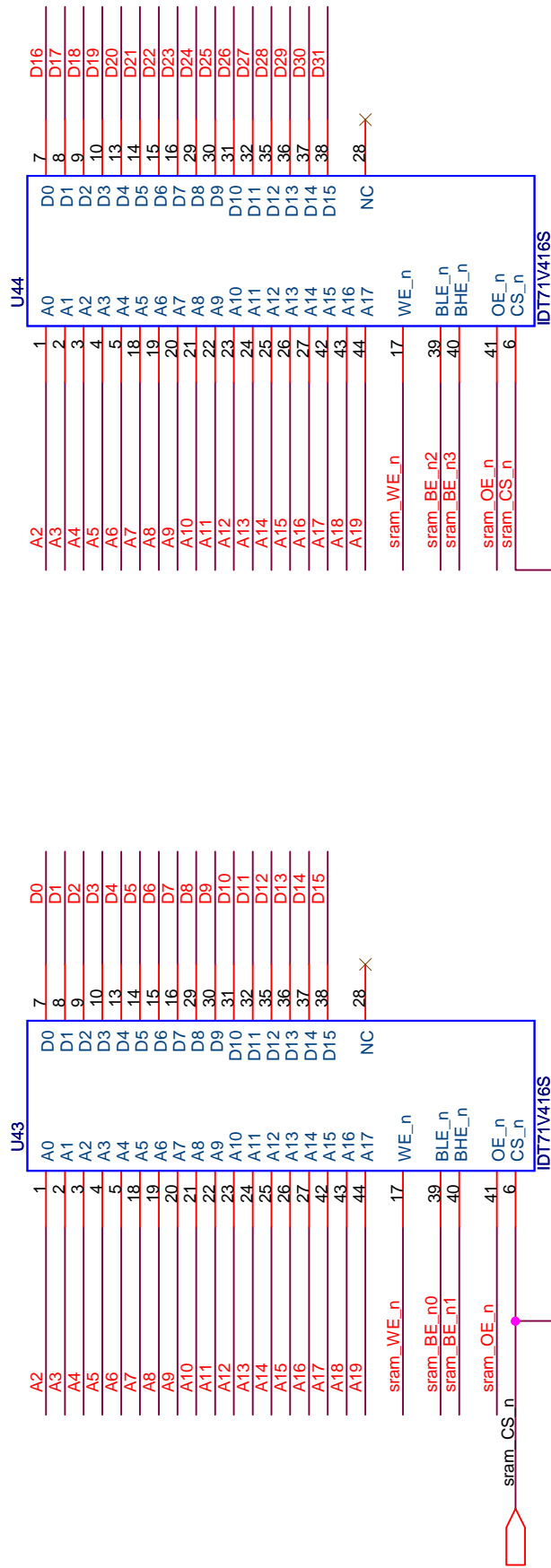


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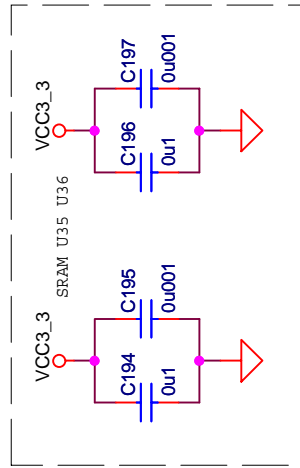
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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	
B	P06-10217	02	
Date:	Thursday, October 14, 2004	Sheet	37 of 40

SRAM



One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM  
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 110 Cooper St., Suite#201, Santa Cruz, CA 95060

Title

Stratix II DSP Board (Maine)

Size

A Document Number

Rev

02

Date:

Thursday, October 14, 2004

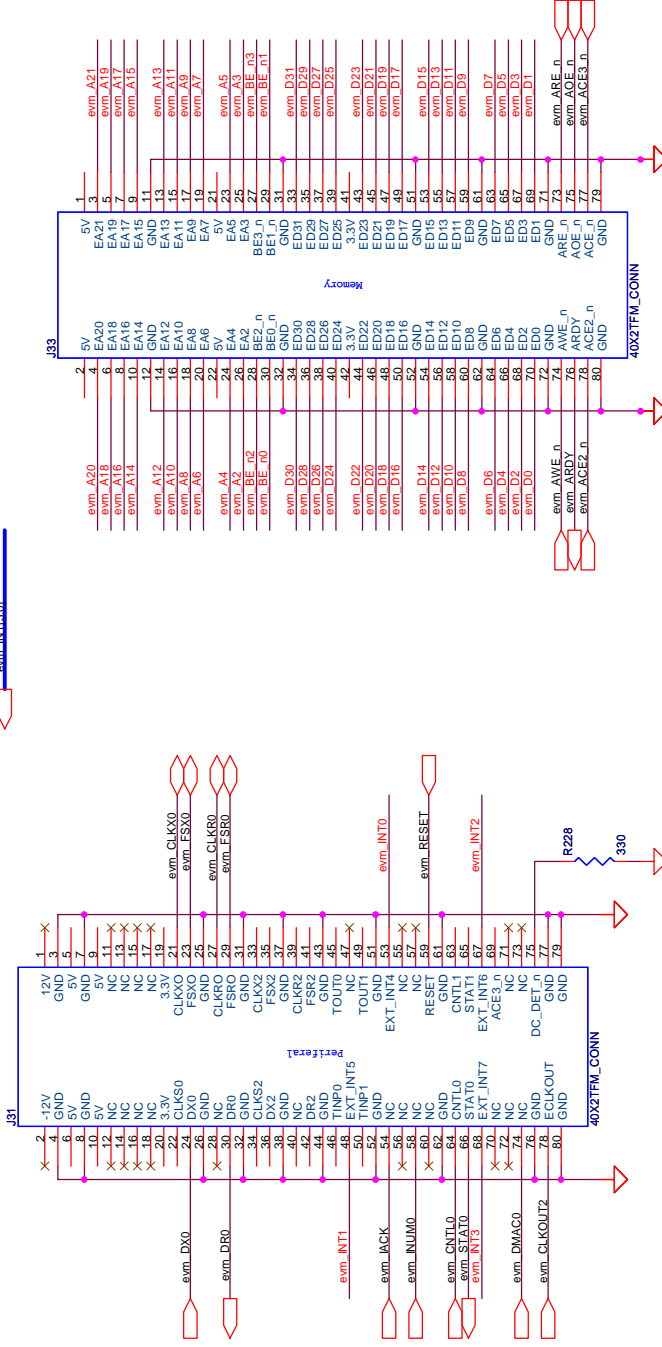
Sheet

38 of 40

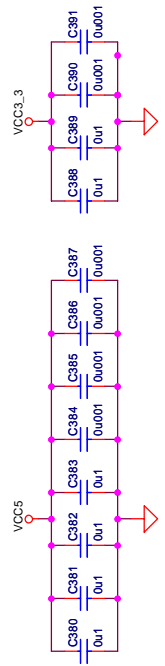
TI EVM Connector



3.00" apart



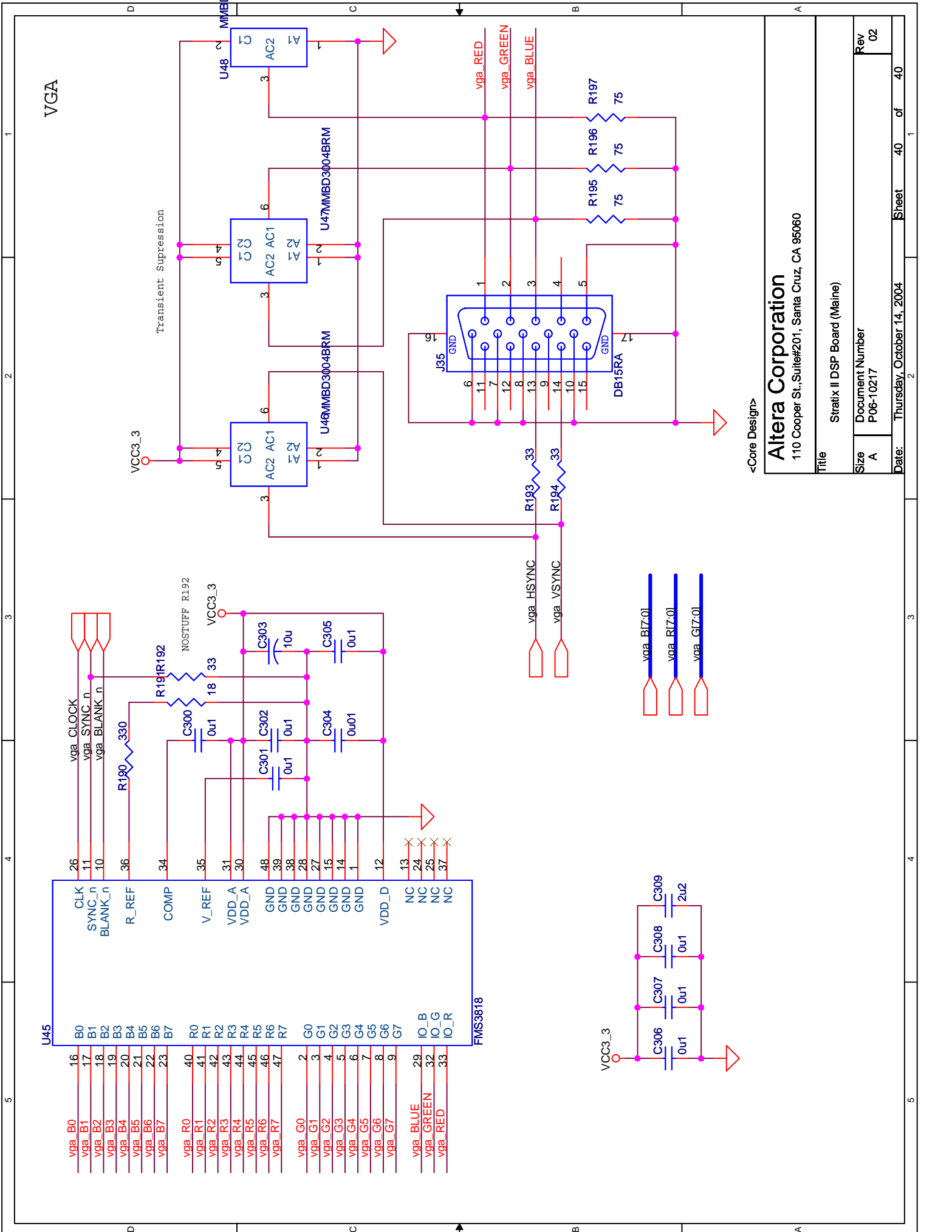
These connectors reference the TI 6416 board



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Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	
B	P06-10217	02	
Date:	Thursday, October 14, 2004	Sheet	39 of 40



VGA

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110 Cooper St., Suite#201, Santa Cruz, CA 95060

Title		Stratix II DSP Board (Maine)	
Size	Document Number	Rev	
A	P06-10217	02	
Date:	Thursday, October 14, 2004	Sheet	40 of 40