

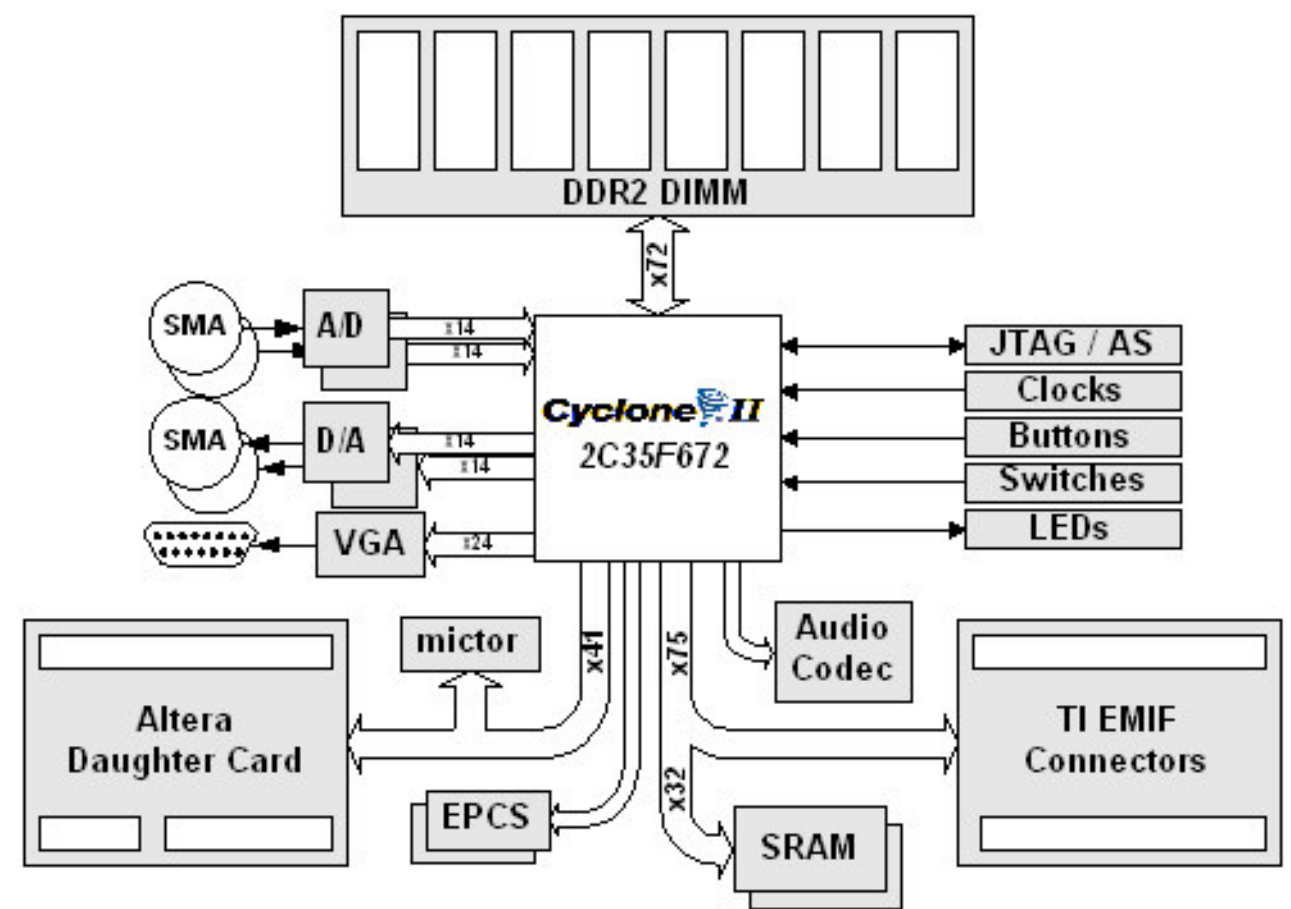
NOTES:

- Project Drawing Numbers:
 - Raw PCB 100-0310202-B1
 - Gerber Files 110-0310202-B1
 - PCB Design Files 120-0310202-B1
 - Assembly Drawing 130-0310202-B1
 - Fab Drawing 140-0310202-B1
 - Schematic Drawing 150-0310202-B1
 - PCB Film 160-0310202-B1
 - Bill of Materials 170-0310202-B1
 - Schematic Design Files 180-0310202-B1
 - Functional Specification 210-0310202-B1
 - PCB Layout Guidelines 220-0310202-B1
 - Assembly Rework 320-0310202-B1

2. 894 Parts, 63 Library Parts, 874 Nets, 4299 Pins

REV	DATE	PAGES	DESCRIPTION
A	01/26/2005	----	Released for Prototype Production
B	02/17/2005	----	Fixed clock buffer U27 pinout. Fixed SSRAM U22 pinout to remove rework. Fixed EVM_CE2/CE3 short on T1 EVM Interface. Fixed VTT Regulator U8 decoupling by adding ceramic output caps.

System Block Diagram



PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	FPGA Package I/O Diagram & Design Notes
3	Clock Circuitry
4	Cyclone II Banks 1 & 2
5	Cyclone II Banks 3 & 4
6	Cyclone II Banks 5 & 6
7	Cyclone II Banks 7 & 8
8	DDR2 DIMM
9	DDR2 Termination
10	Cyclone II Configuration Circuitry
11	ADC Channel A
12	ADC Channel B
13	DAC Channel A
14	DAC Channel B
15	Video DAC
16	AIC23 Audio Codec
17	Buttons, Switches, LEDs
18	SRAM, TI EVM Connectors
19	Altera Daughter Card & Mictor Connector
20	Cyclone II Power and Decoupling
21	Digital Power Supplies
22	Analog Power Supplies
23	----
24	----
25	----

- ADC Ground
- DAC Ground
- PLL Ground
- Digital Ground



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Cyclone II DSP Board**

Size B Document Number: **150-0310202-B1** Rev **B**

Date: Thursday, March 24, 2005 Sheet 1 of 22

- Notes:**
- FPGA Schematic Symbol Breakdown:
 - Bank1 - I/O
 - Bank2 - I/O
 - Bank3 - I/O
 - Bank4 - I/O
 - Bank5 - I/O
 - Bank6 - I/O
 - Bank7 - I/O
 - Bank8 - I/O
 - Configuration
 - Clocks
 - VCCint, GND
 - VCCio, GND

2. PCB Supports 2C35 - 2C50 - 2C70 Migration

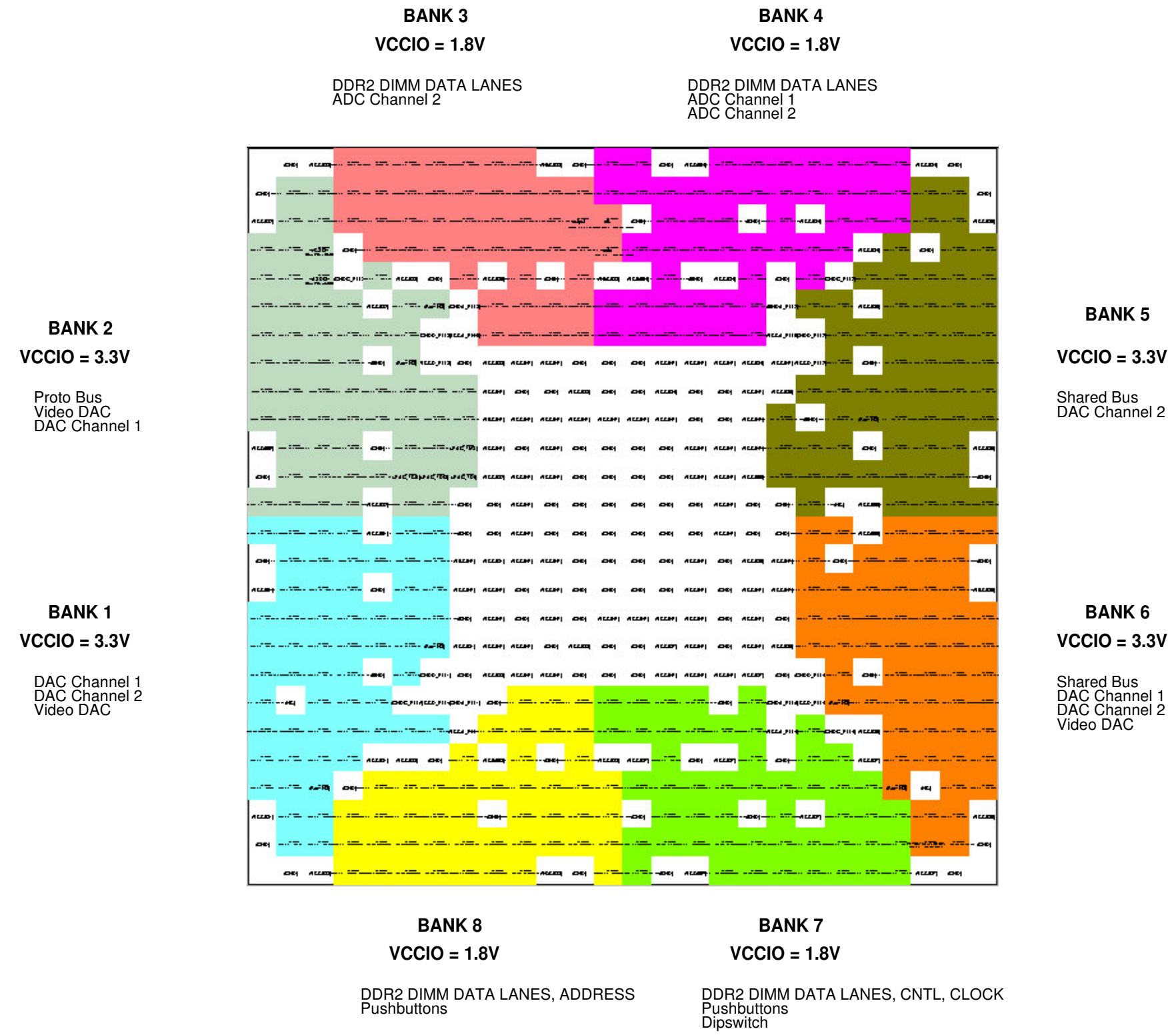
No additional I/O of 2C35 or 2C50 used as the 2C70 has the fewest I/O of the group due to additional VCCINT, GND, and VREF pins on the larger 2C50 and 2C70 devices.

3. Some I/O pins are connected to 1.2V and GND. These are the additional VCC and GND pins of the larger 2C50 and 2C70.

--- WARNING ---
DO NOT DRIVE UNUSED I/O TO GND IN QUARTUS

Leaving 1.2V-connected I/O pins as outputs driving GND causes high I/O current and increased temperature which can lead to device damage if left over a long period of time.

FPGA Package Top View
(2C70 Device Shown)

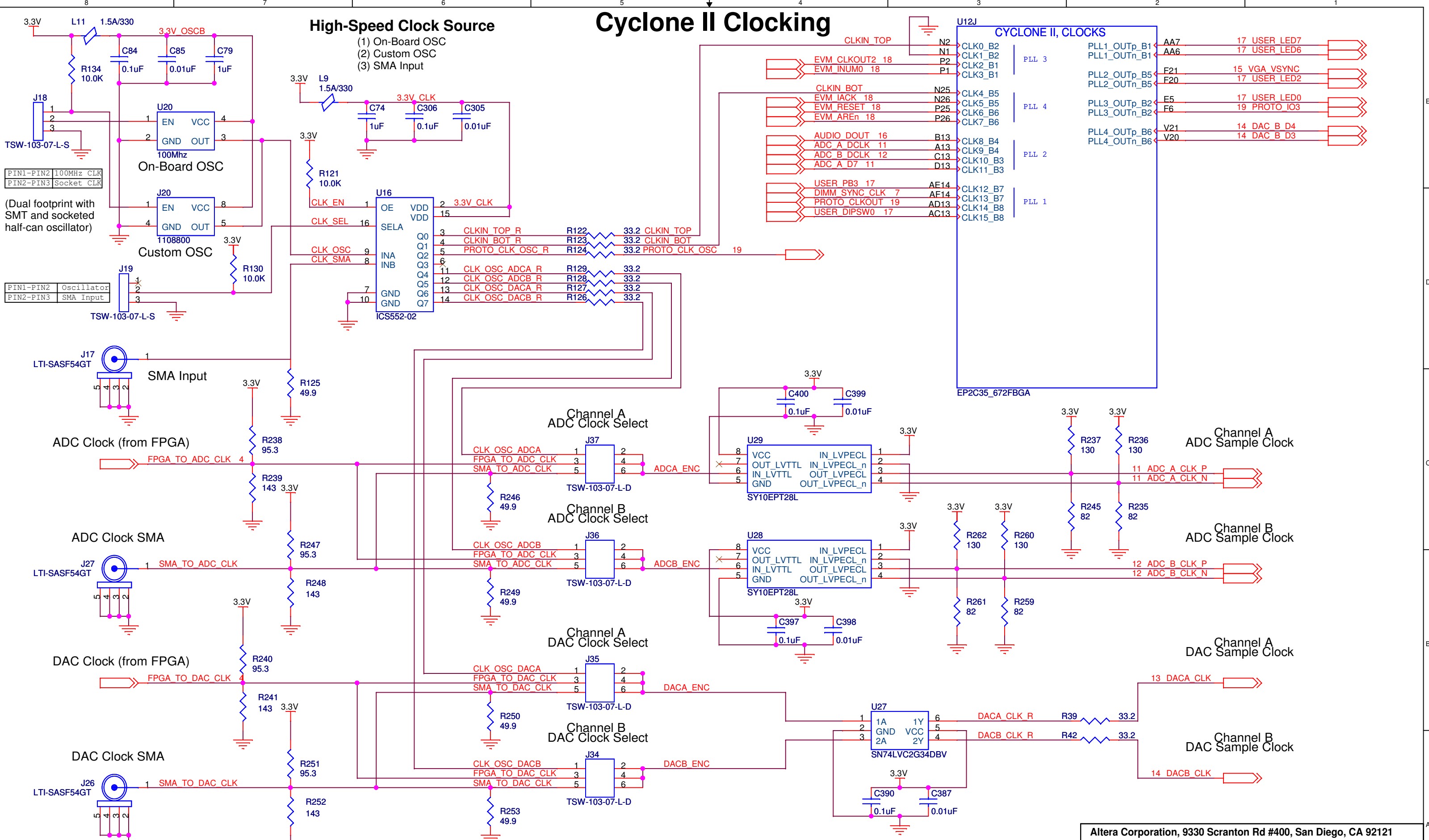


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 2	of 22

Cyclone II Clocking

High-Speed Clock Source

- (1) On-Board OSC
- (2) Custom OSC
- (3) SMA Input



PIN1-PIN2 | 100MHz CLK
PIN2-PIN3 | Socket CLK

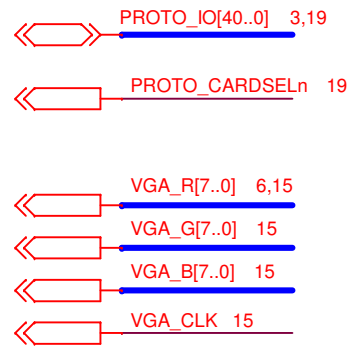
(Dual footprint with SMT and socketed half-can oscillator)

PIN1-PIN2 | Oscillator
PIN2-PIN3 | SMA Input

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 3	of 22



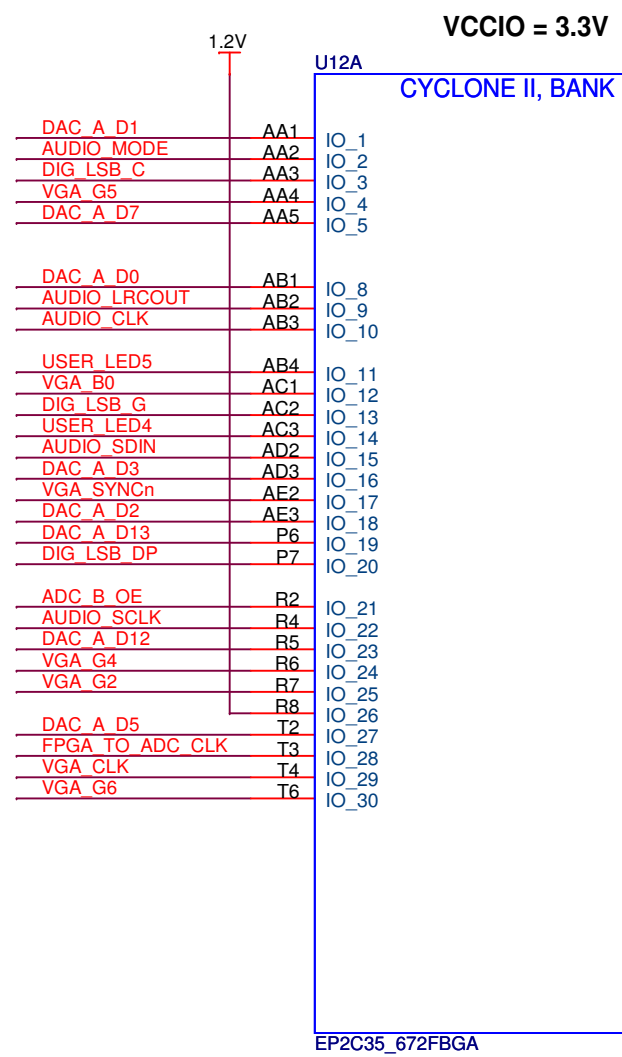
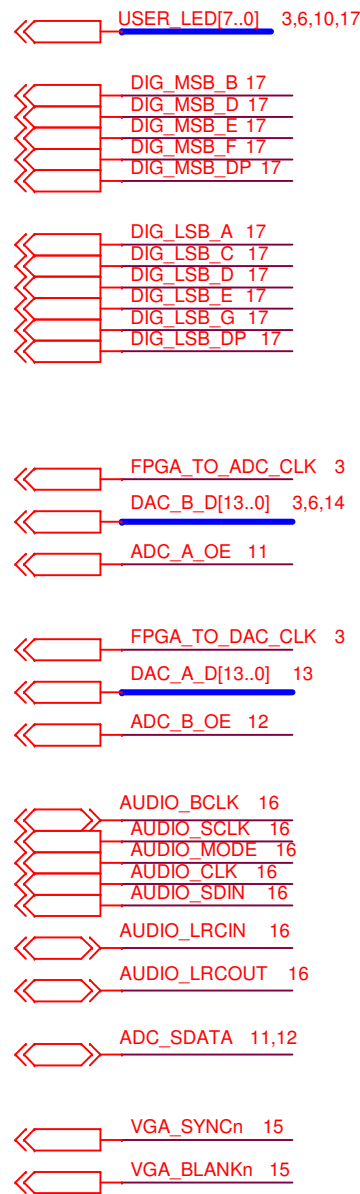
CYCLONE II BANKS 1 & 2



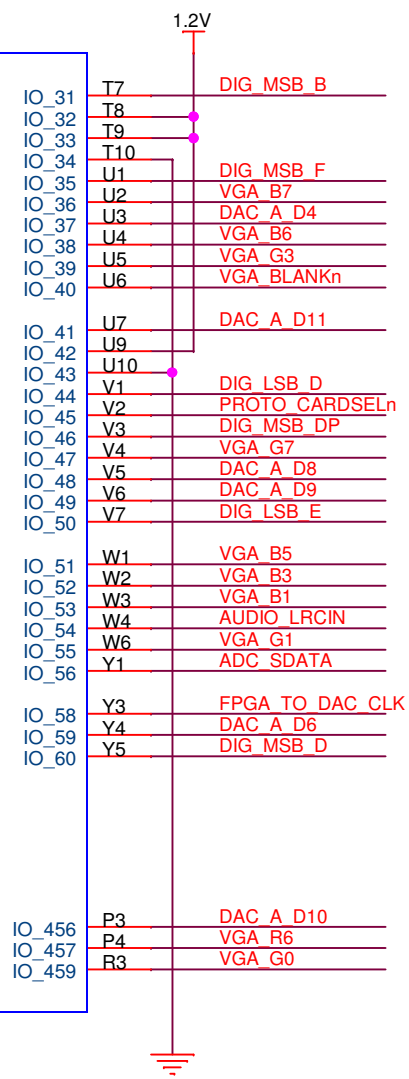
These pins are connected to VCCINT on 2C70.

These pins are connected to VCCINT on 2C70.

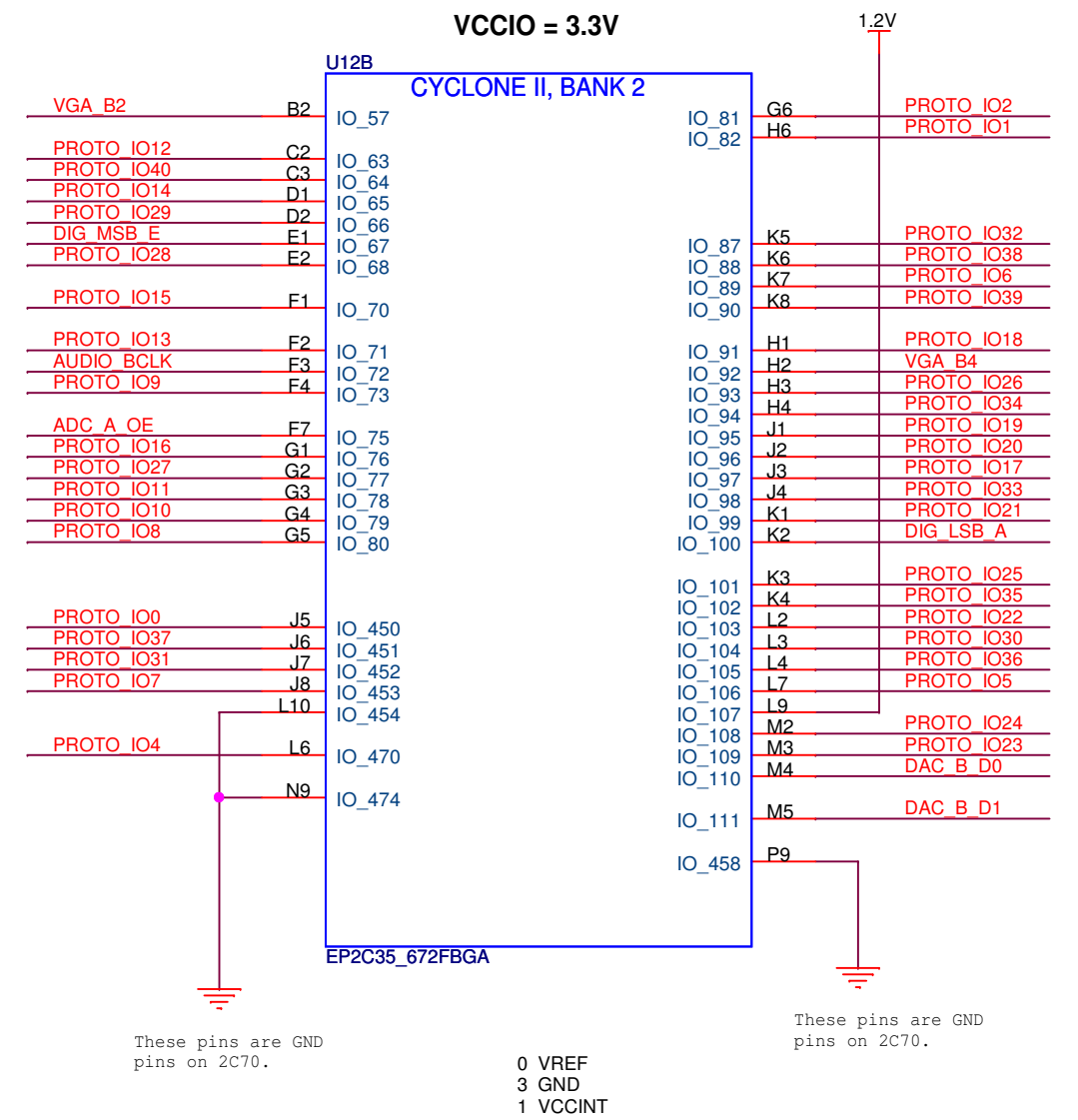
These pins are connected to VCCINT on 2C70.



0 VREF
2 GND
4 VCCINT



These pins are GND pins on 2C70.



These pins are GND pins on 2C70.

These pins are GND pins on 2C70.

0 VREF
3 GND
1 VCCINT



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 4	of 22

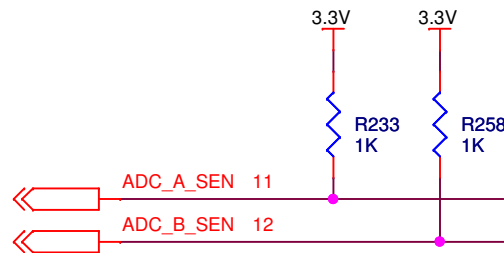
CYCLONE II BANKS 3 & 4

- DIMM_DQ[71..0] 7,8,9
- DIMM_DQS[8..0] 7,8,9
- DIMM_A_R[15..0] 7,9
- DIMM_BA_R[2..0] 7,9
- DIMM_DM[8..0] 7,8,9

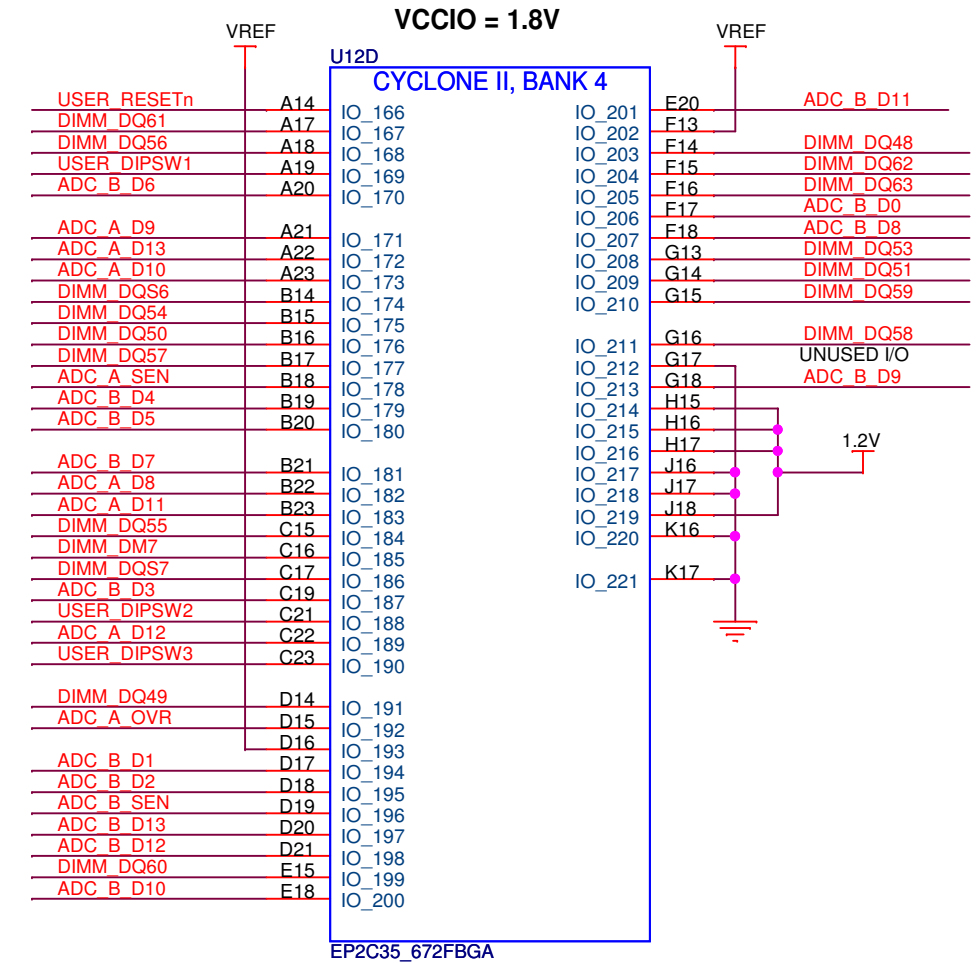
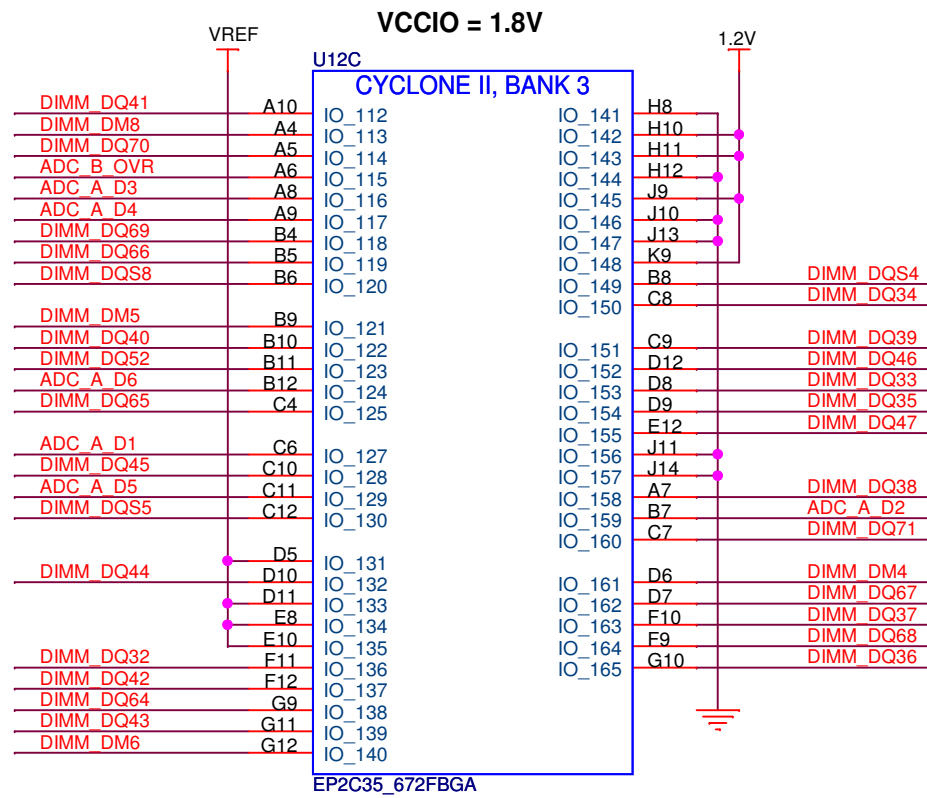
- DIMM_RASn_R 7,9
- DIMM_CASn_R 7,9
- DIMM_WEn_R 7,9
- DIMM_CSn_R0 7,9
- DIMM_CSn_R1 7,9
- DIMM_CKE_R0 7,9
- DIMM_CKE_R1 7,9
- DIMM_ODT_R0 7,9
- DIMM_ODT_R1 7,9

- ADC_A_D[13..0] 3,10,11
- ADC_A_OVR 11
- ADC_B_D[13..0] 12
- ADC_B_OVR 12

- USER_DIPSW[7:0] 3,7,17
- USER_RESETn 17,19



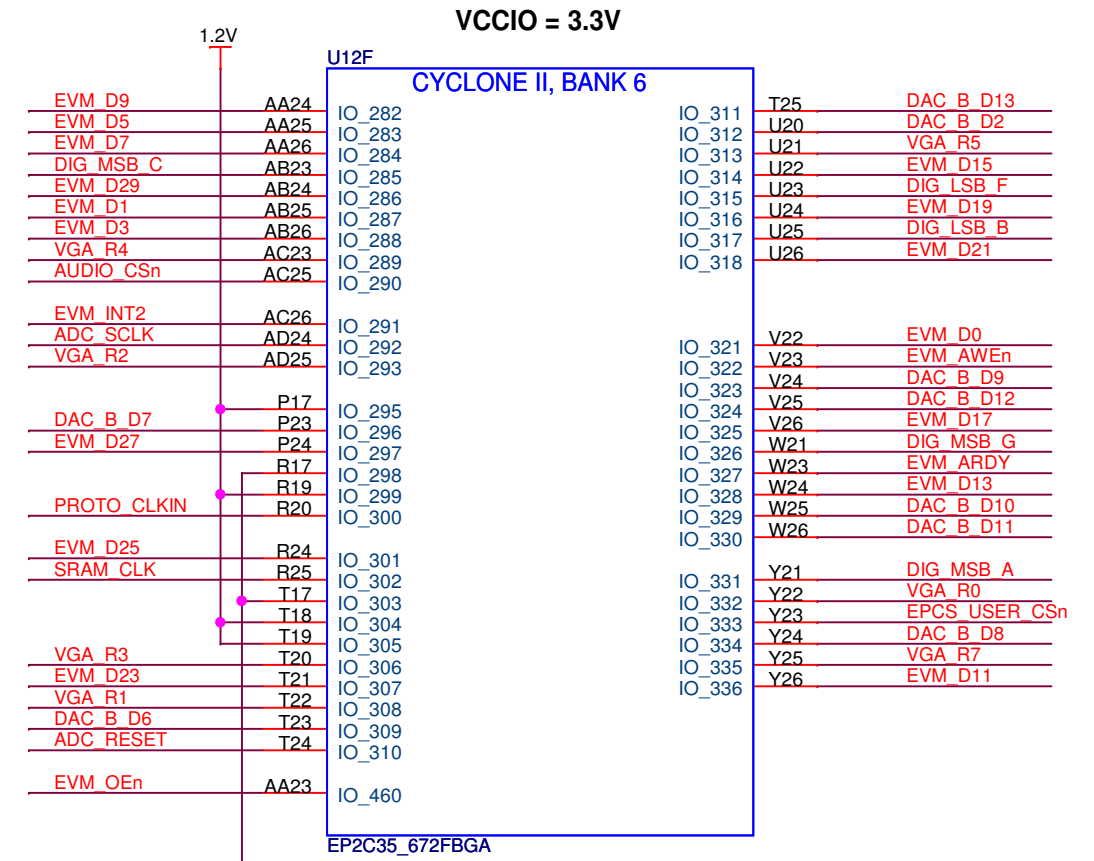
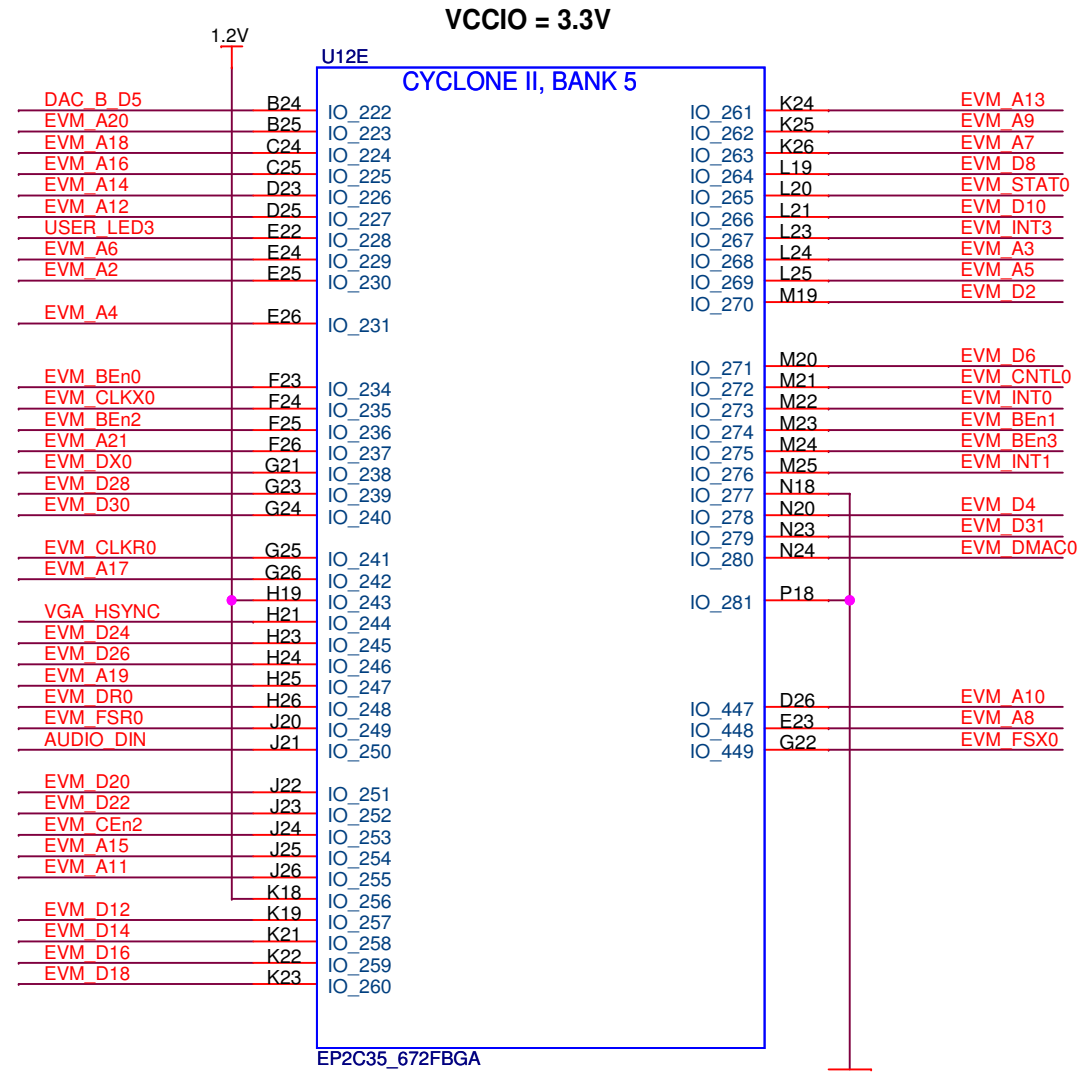
1.8V driving 3.3V logic must be driven as open-drain



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 5	of 22

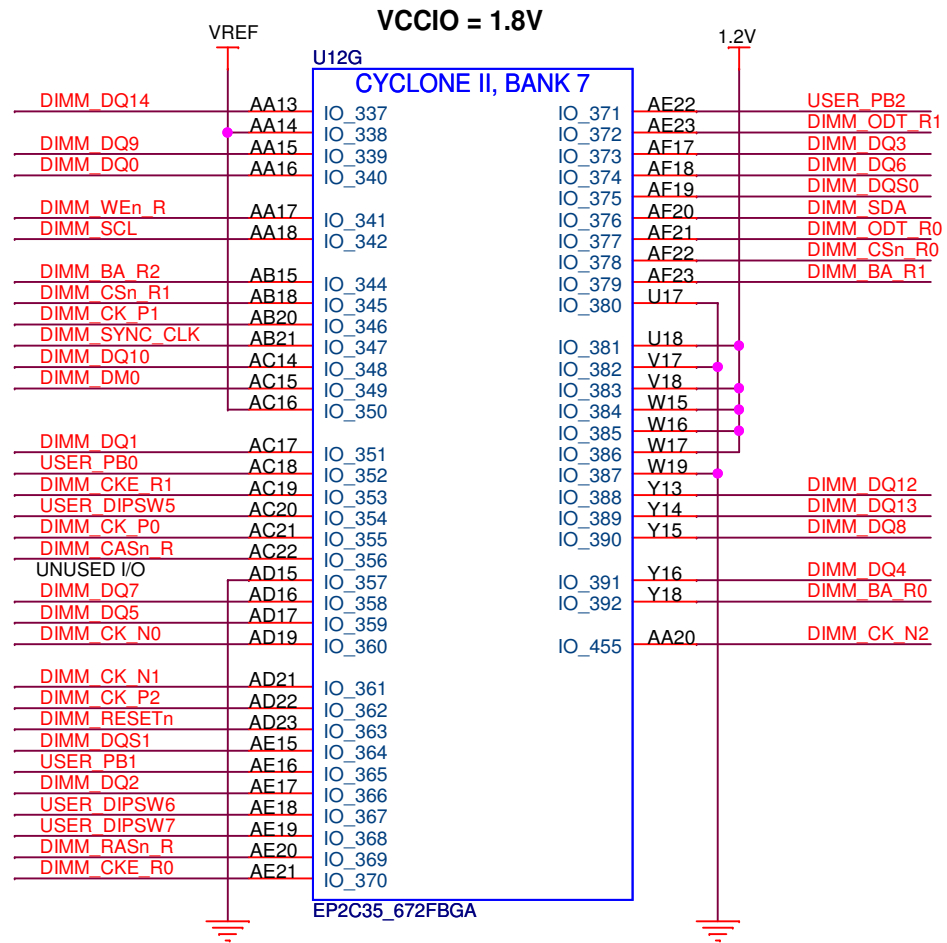
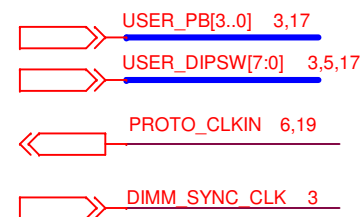
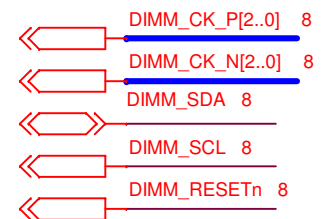
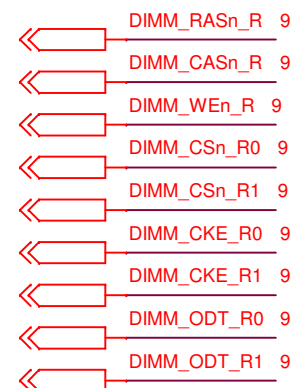
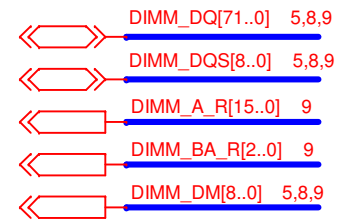
CYCLONE II BANKS 5 & 6

- ← DAC_A_D[13..0] 4,13
- ← DAC_B_D[13..0] 3,4,14
- ← EVM_A[21..2] 18
- ← EVM_D[31..0] 18
- ← EVM_BEn[3..0] 18
- ← EVM_INT[3..0] 18
- ← EVM_CEn[3..2] 10,18
- ← EVM_DX0 18
- ← EVM_CNTL0 18
- ← EVM_STAT0 18
- ← EVM_DMAC0 18
- ← EVM_AWEn 18
- ← EVM_DR0 18
- ← EVM_OEn 18
- ← EVM_ARDY 18
- ← EVM_CLKX0 18
- ← EVM_FSX0 18
- ← EVM_CLKR0 18
- ← EVM_FSR0 18
- ← USER_LED[7..0] 3,4,10,17
- ← AUDIO_CSn 16
- ← AUDIO_DIN 16
- ← EVM_RESET 3,18
- ← VGA_HSYNC 15
- ← VGA_R[7..0] 4,15
- ← VGA_B[7..0] 4,15
- ← DIG_MSB_A 17
- ← DIG_MSB_C 17
- ← DIG_MSB_G 17
- ← DIG_LSB_B 17
- ← DIG_LSB_F 17
- ← ADC_RESET 11,12
- ← ADC_SCLK 11,12
- ← ADC_B_SEN 5,12
- ← EPCS_USER_CSn 10
- ← SRAM_CLK 18
- ← PROTO_CLKIN 19

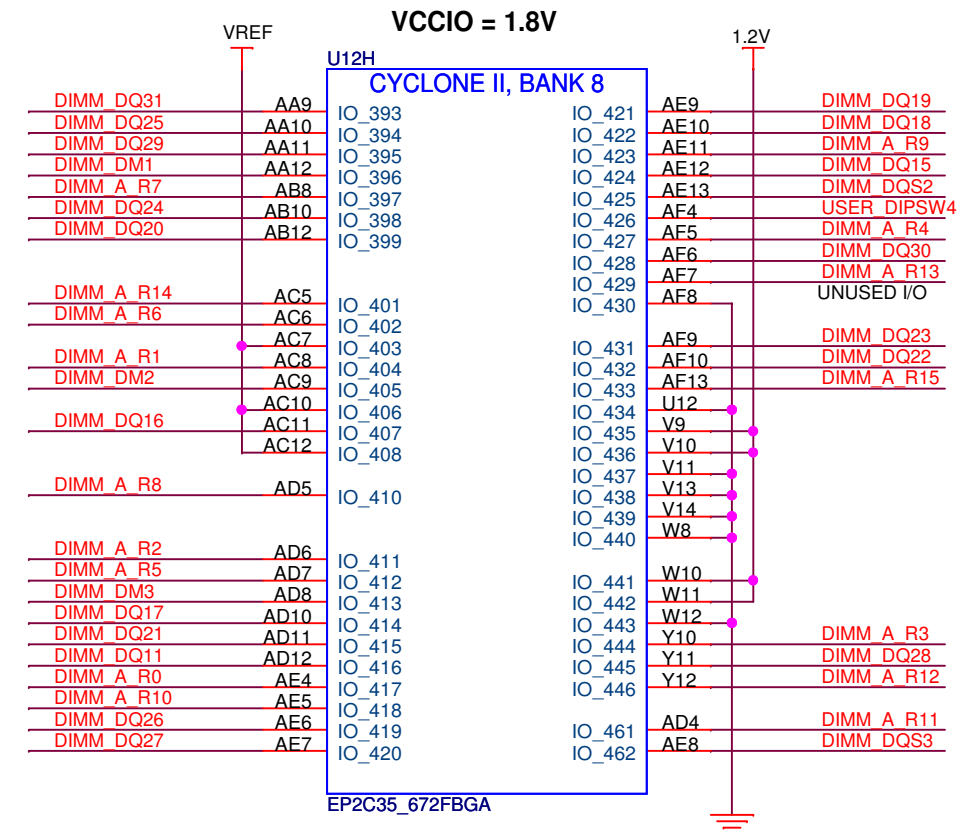


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 6	of 22

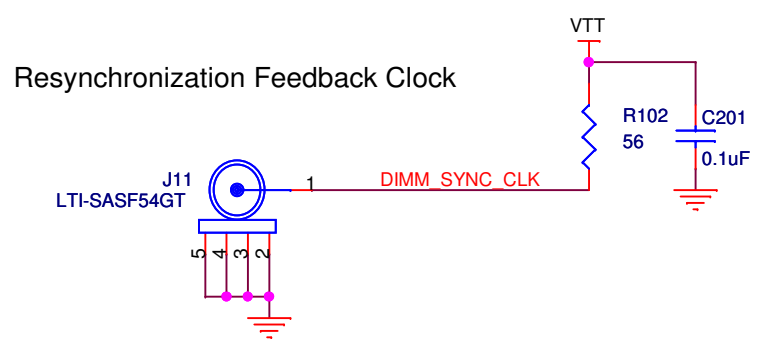
CYCLONE II BANKS 7 & 8



2 VREF
4 GND
5 VCCINT



3 VREF
7 GND
4 VCCINT

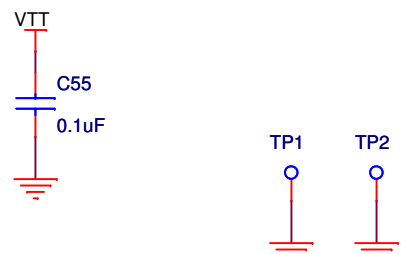
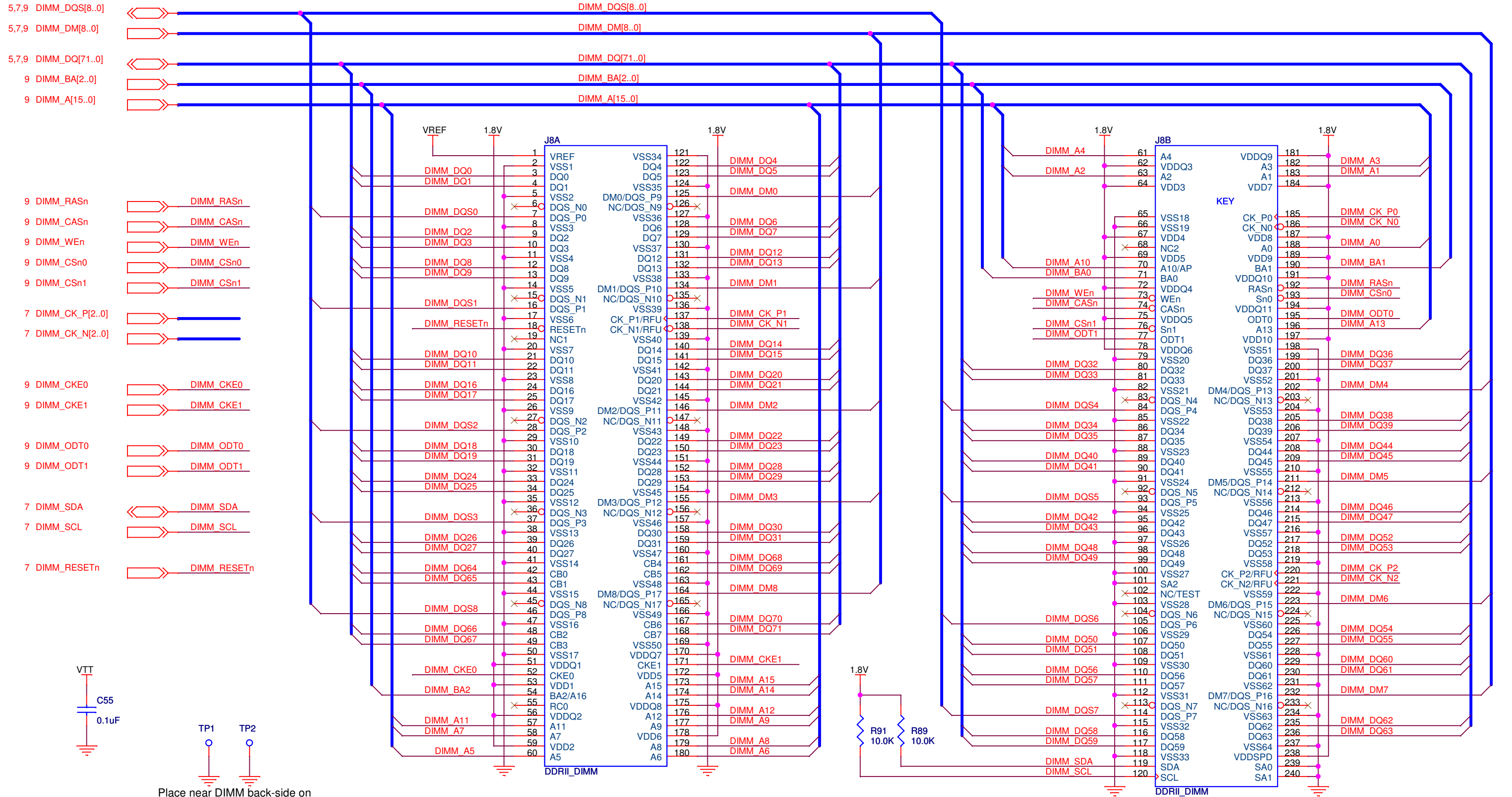


SMA for External Clock Input / Eye Diagram Output
(secondary use)



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 7	of 22

DDR2 SDRAM DIMM



Place near DIMM back-side on component side of PCB

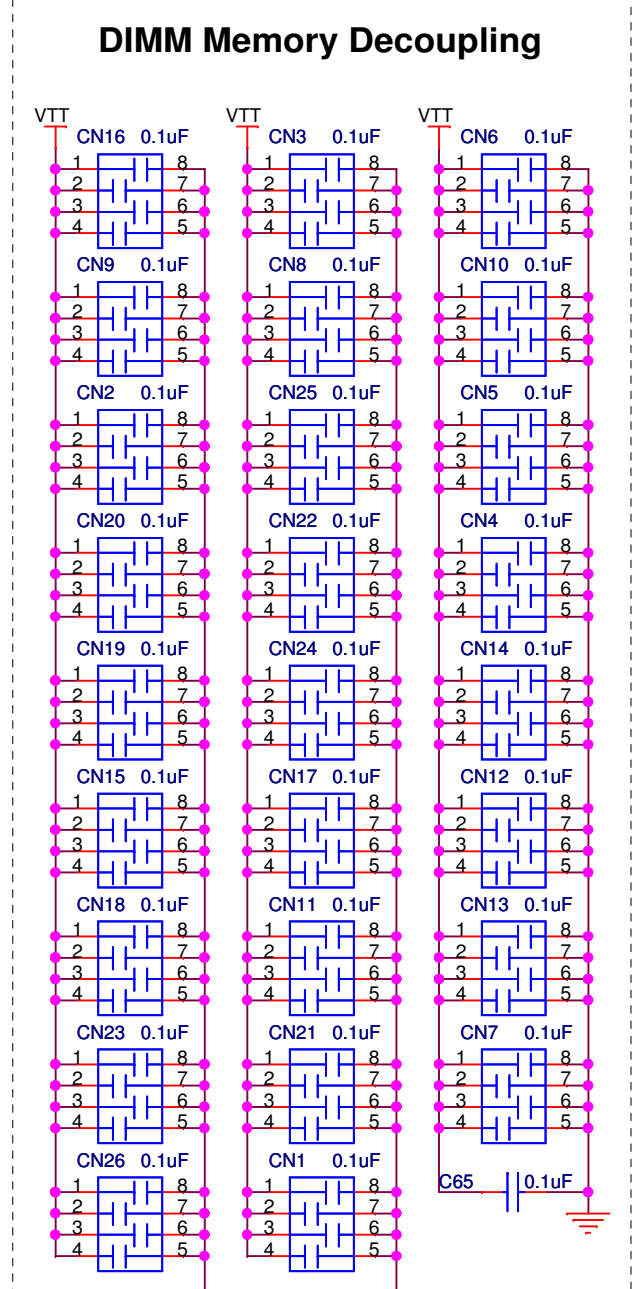
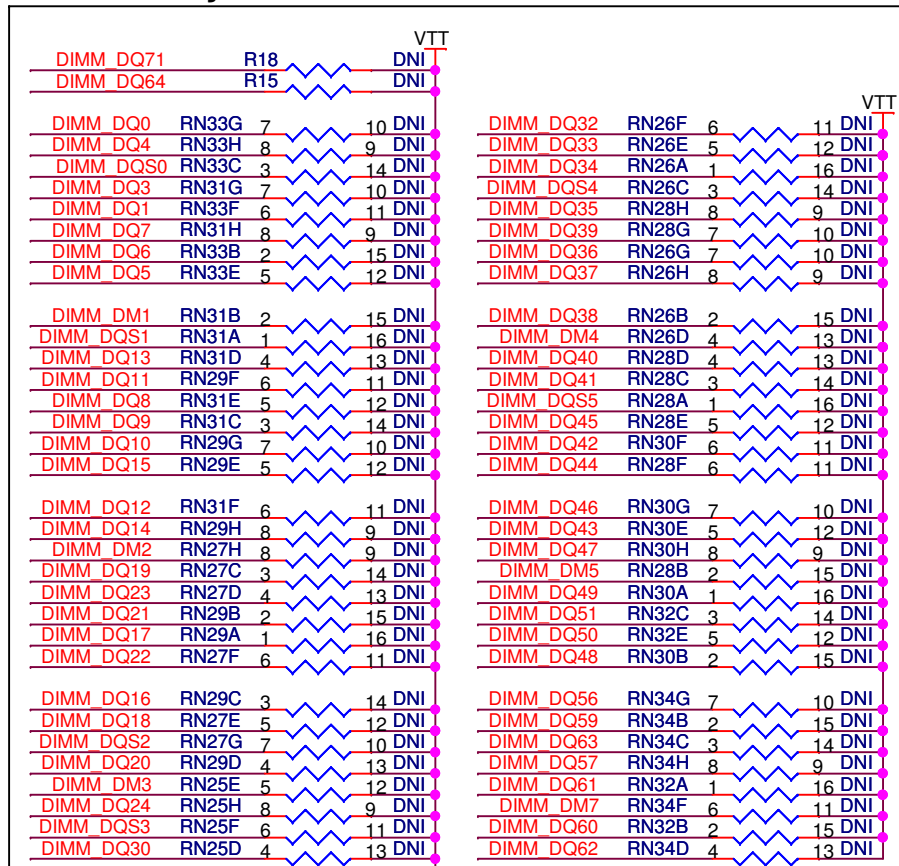


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title		
Cyclone II DSP Board		
Size	Document Number	Rev
B	150-0310202-B1	B
Date:	Thursday, March 24, 2005	Sheet 8 of 22

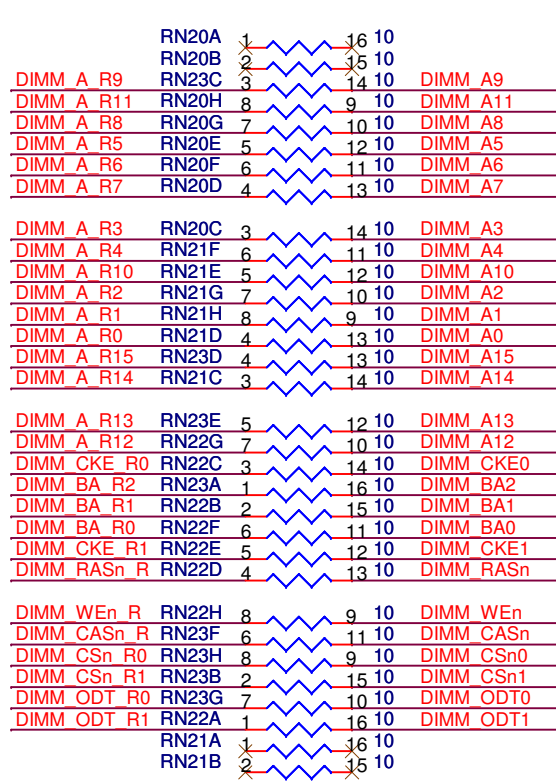
DDR2 SDRAM DIMM Terminations

Cyclone II-Side Termination Resistors

DIMM-Side Termination Resistors

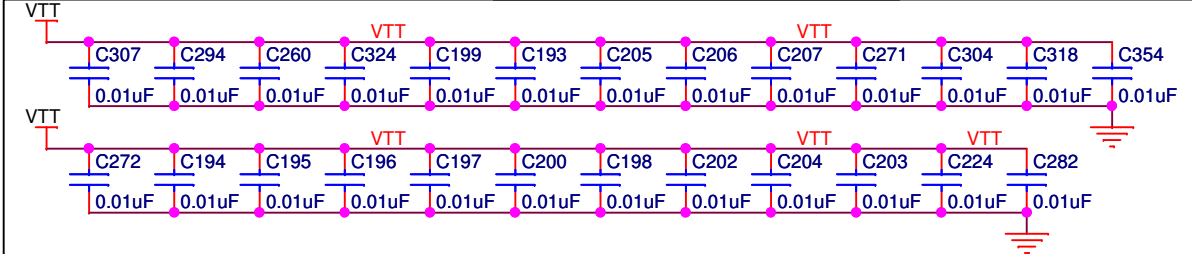
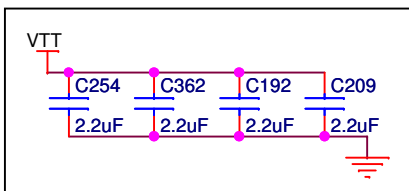


Cyclone II-Side Termination Resistors



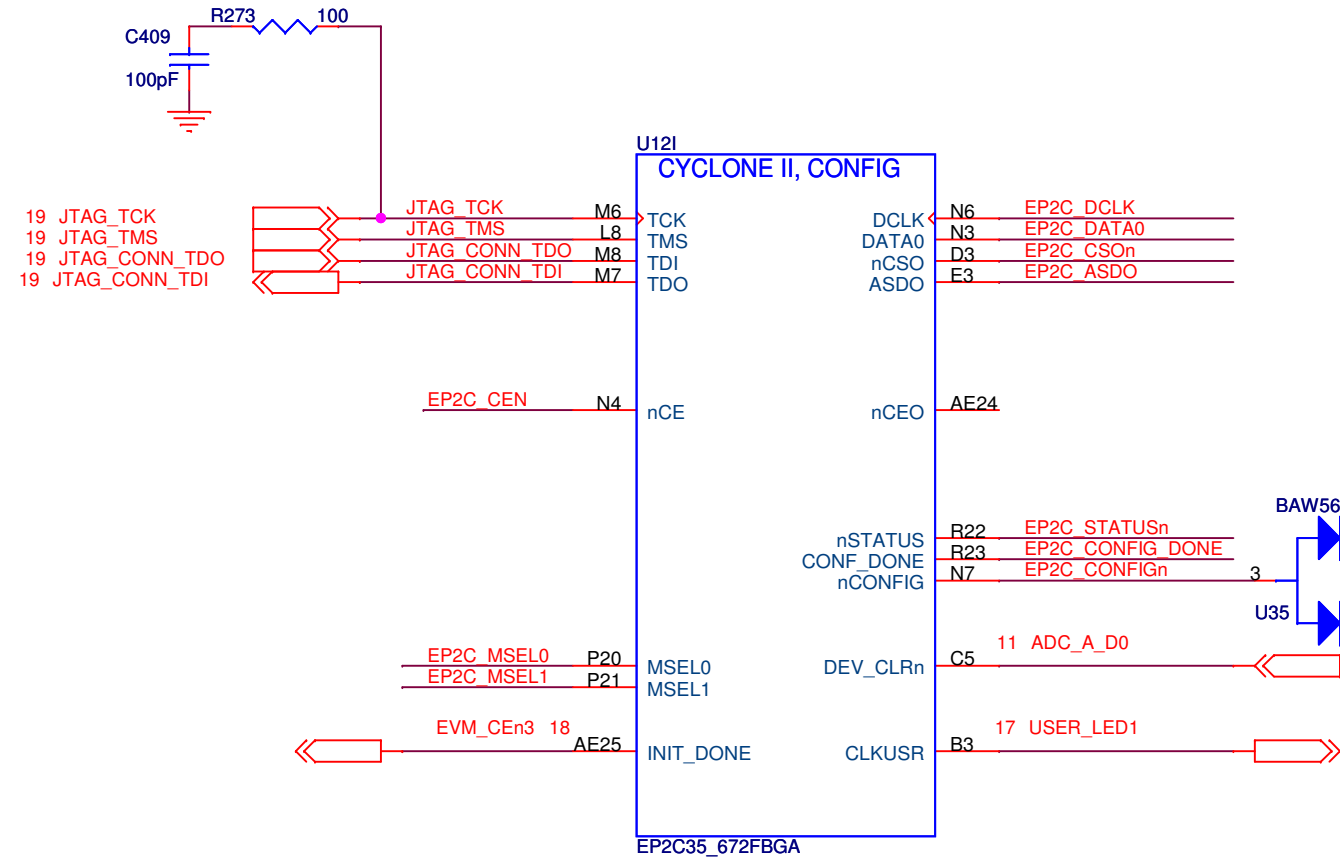
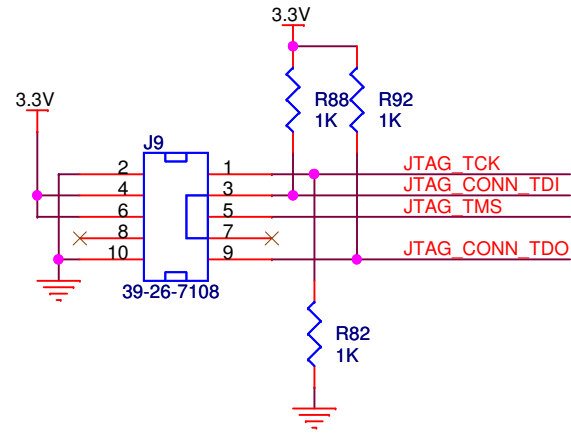
The following resistors can be installed for Class II Termination:

- RN24, RN25, RN26, RN27, RN28, RN29, RN30, RN31, RN32, RN33, RN34, R15, R18

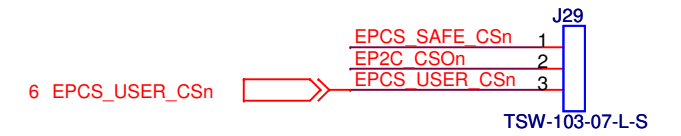


CONFIGURATION CIRCUITRY

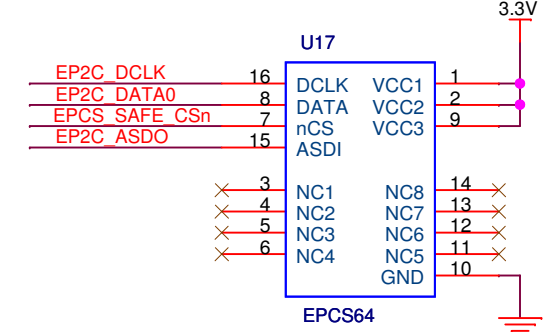
RIGHT ANGLE JTAG HEADER



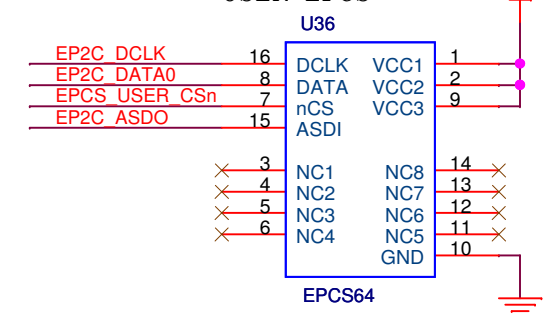
EPCS SELECT



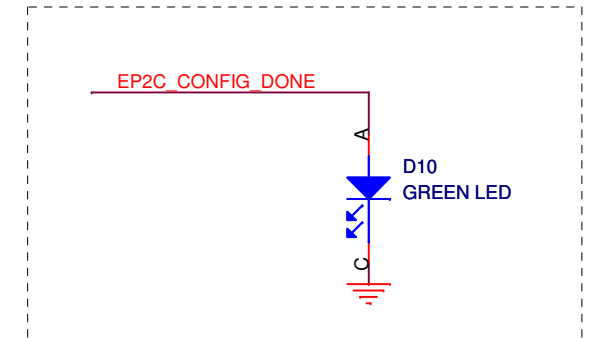
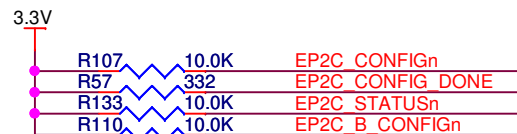
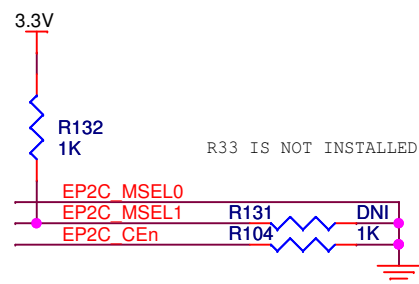
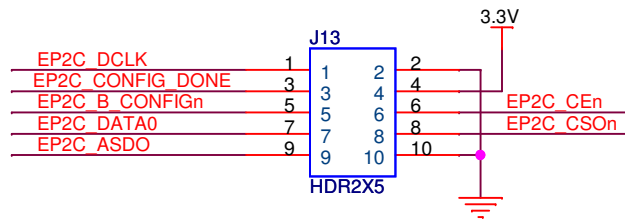
SAFE EPCS



USER EPCS



SURFACE MOUNT ACTIVE SERIAL HEADER



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 10	of 22

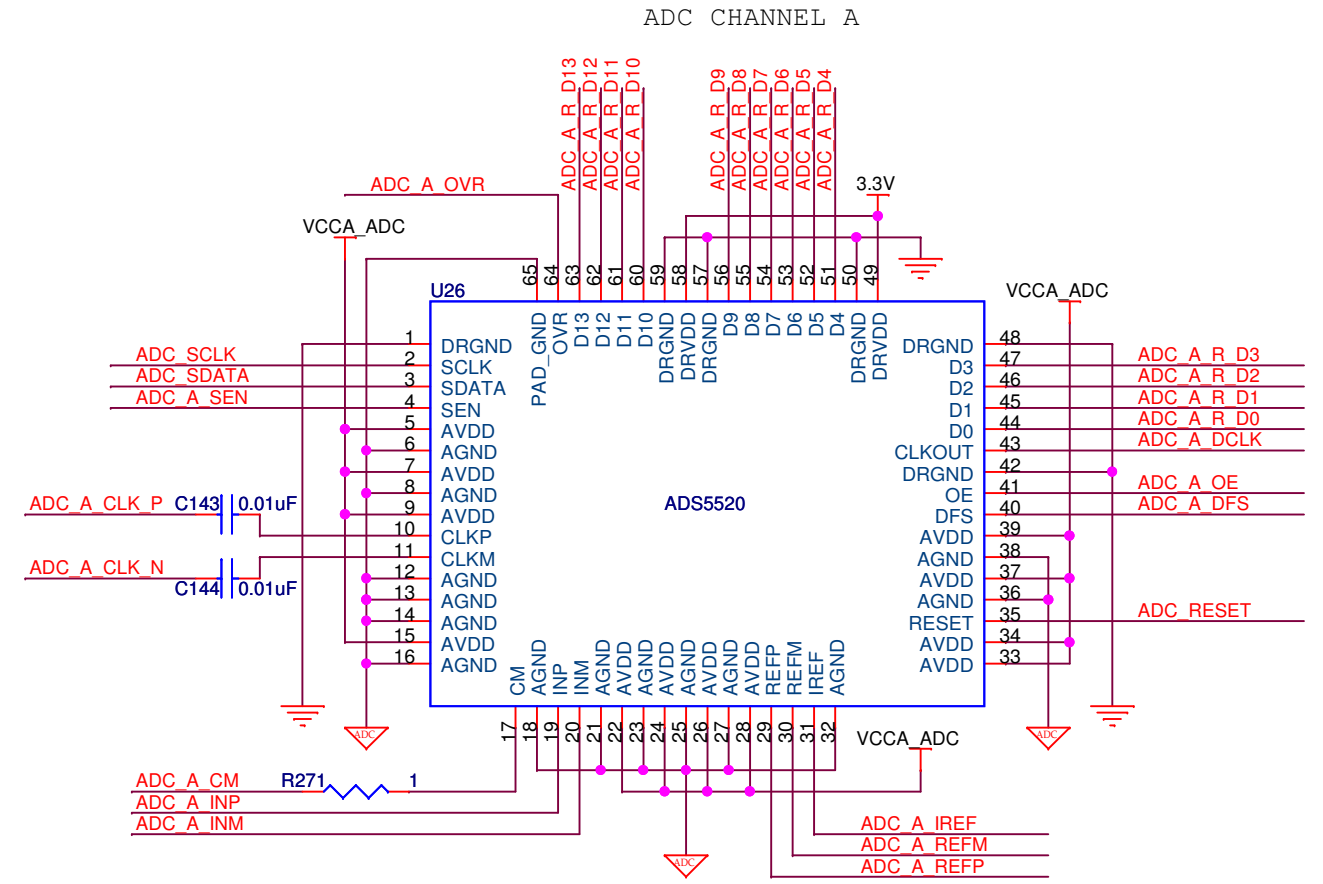
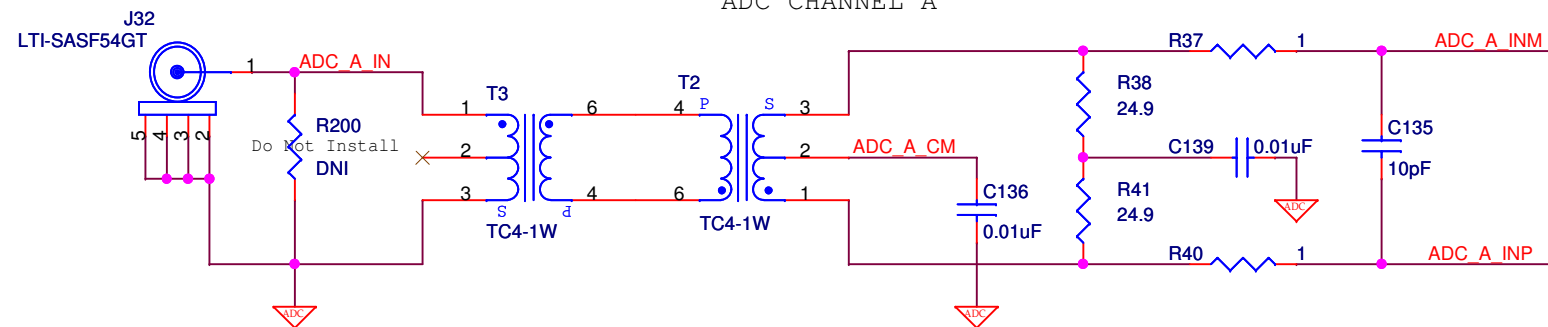
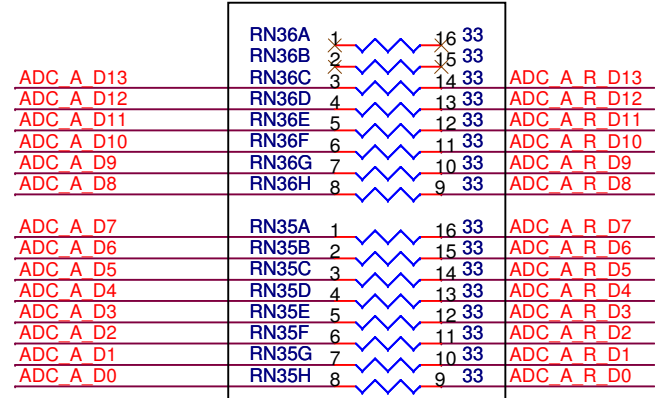
ADC Channel A

ADC SCLK 6,12
 ADC SDATA 4,12
 ADC A SEN 5

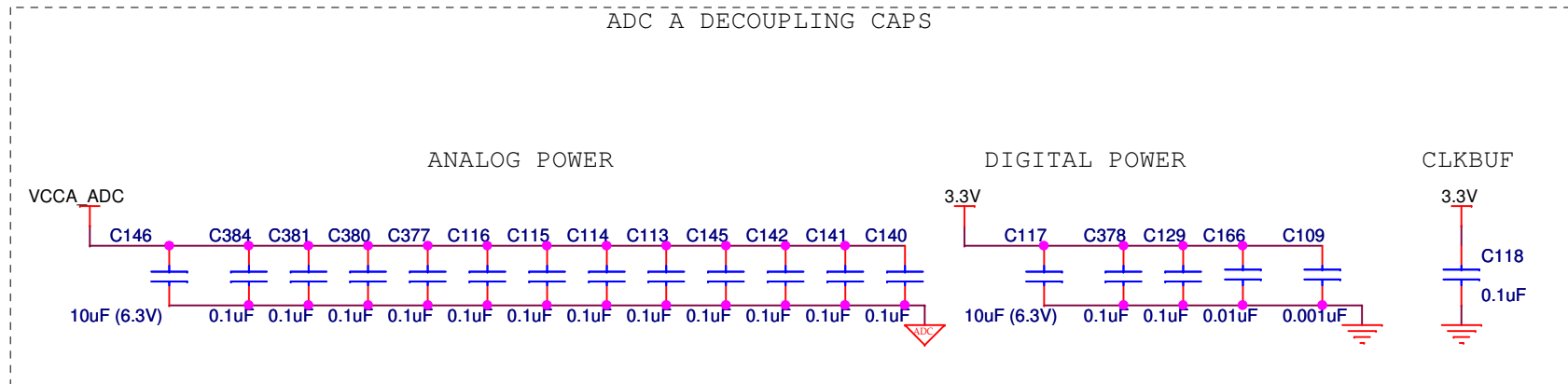
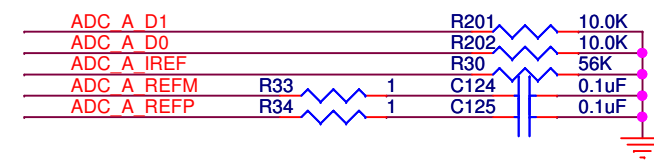
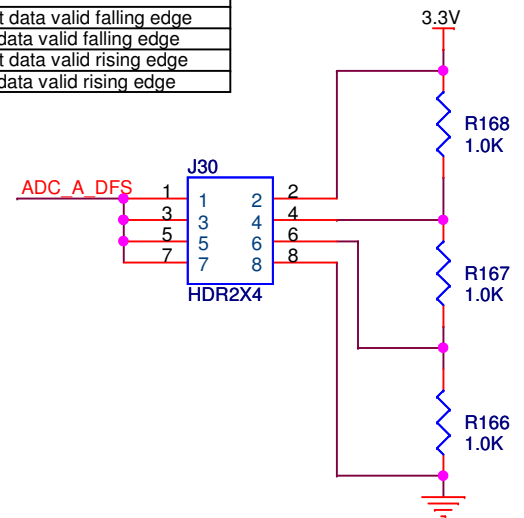
ADC A CLK P 3
 ADC A CLK N 3

ADC A OE 4
 ADC A OVR 5
 ADC RESET 6,12

ADC A DCLK 3
 ADC A D[13..0] 3,5,10



J30 Position	Data Output Format
Pin 1-2	2's Complement data valid falling edge
Pin 3-4	Straight Binary data valid falling edge
Pin 5-6	2's Complement data valid rising edge
Pin 7-8	Straight Binary data valid rising edge



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 11	of 22

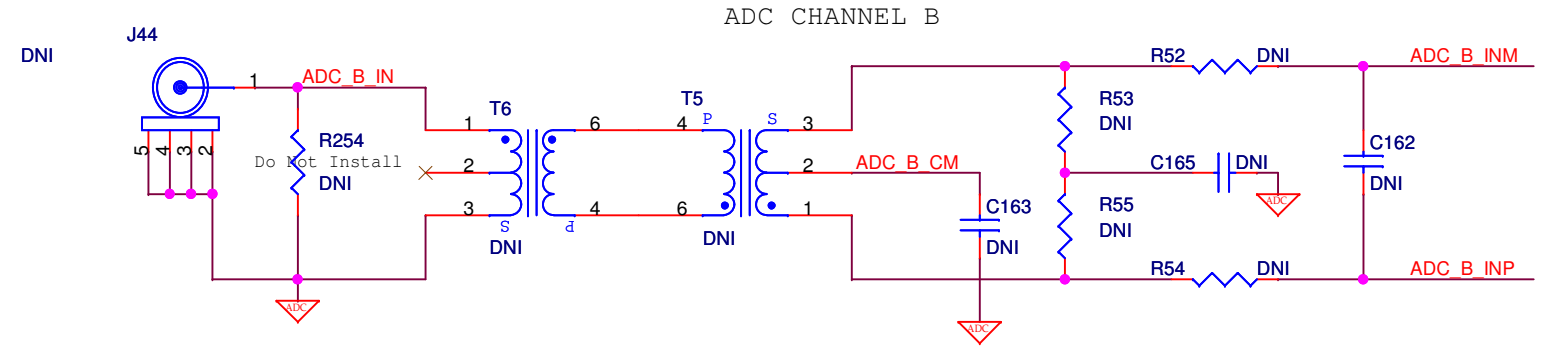
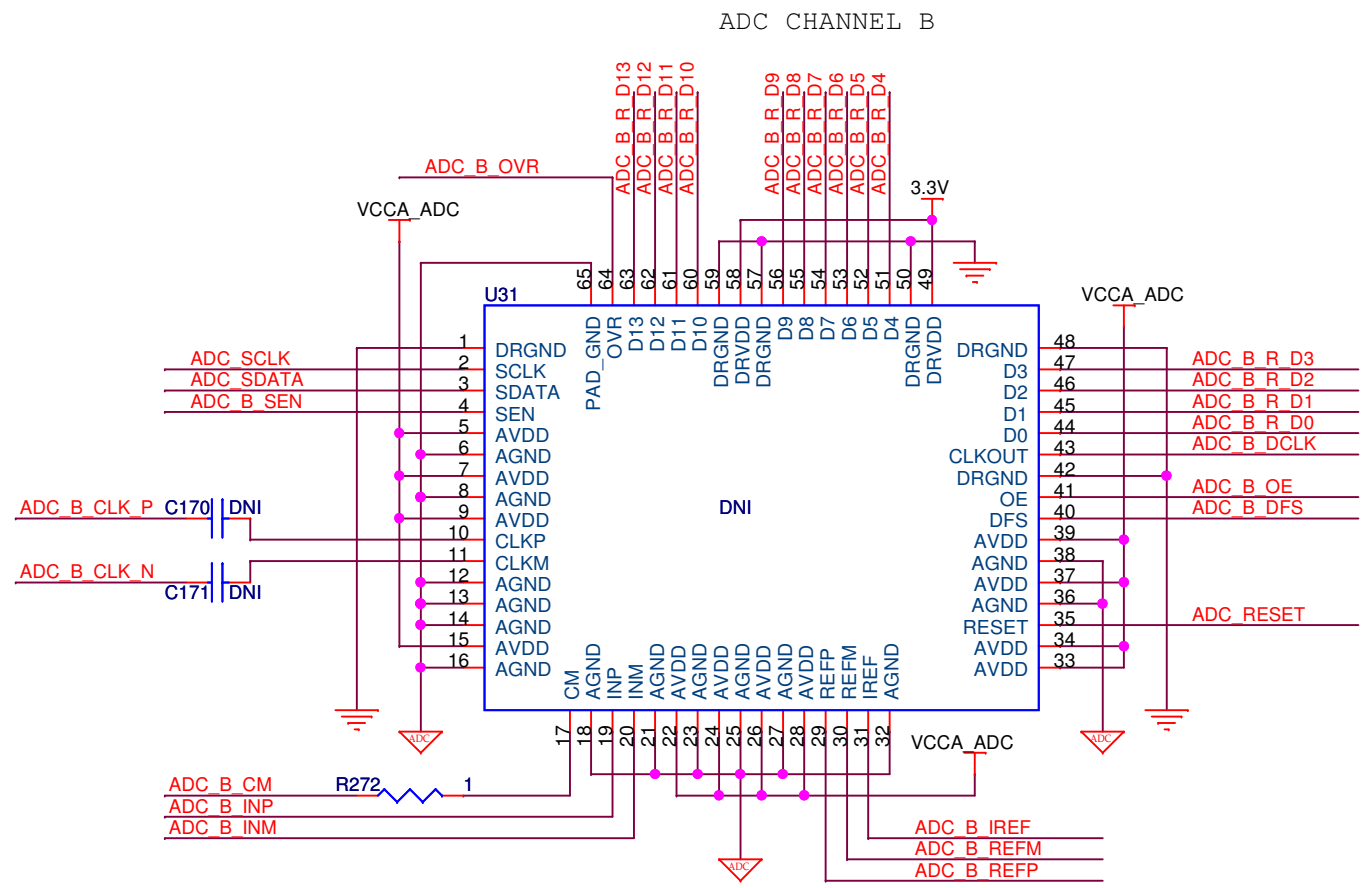
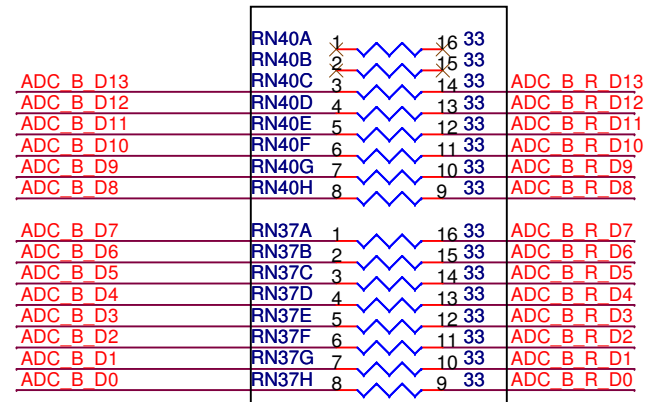
ADC Channel B

ADC SCLK 6,11
ADC SDATA 4,11
ADC B SEN 5

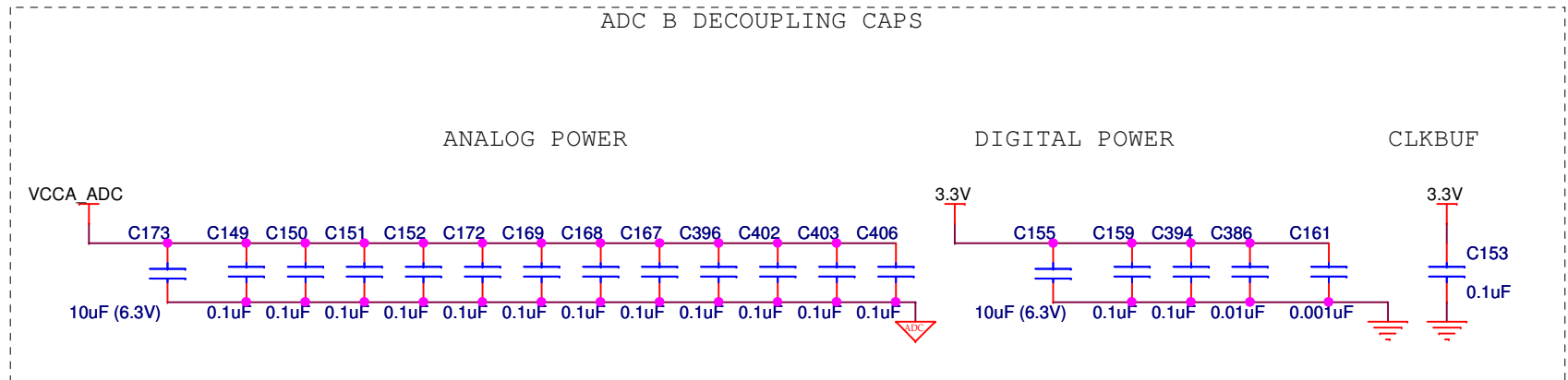
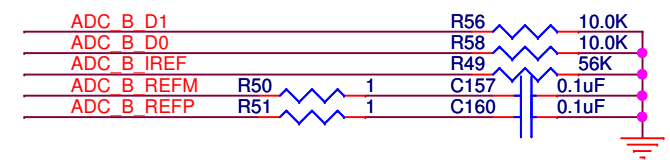
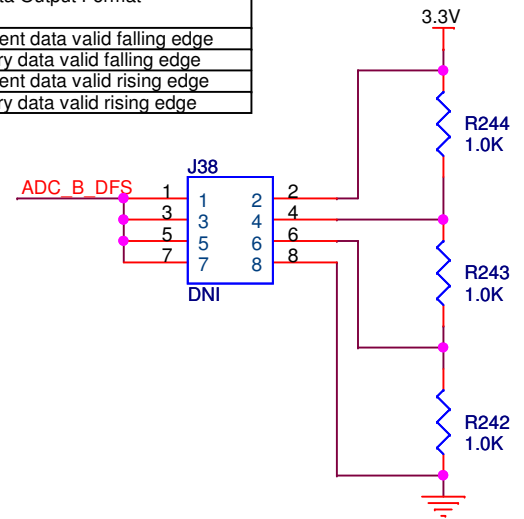
ADC B CLK P 3
ADC B CLK N 3

ADC B OE 4
ADC B OVR 5
ADC RESET 6,11

ADC B DCLK 3
ADC B D[13..0] 5



J38 Position	Data Output Format
Pin 1-2	2's Complement data valid falling edge
Pin 3-4	Straight Binary data valid falling edge
Pin 5-6	2's Complement data valid rising edge
Pin 7-8	Straight Binary data valid rising edge



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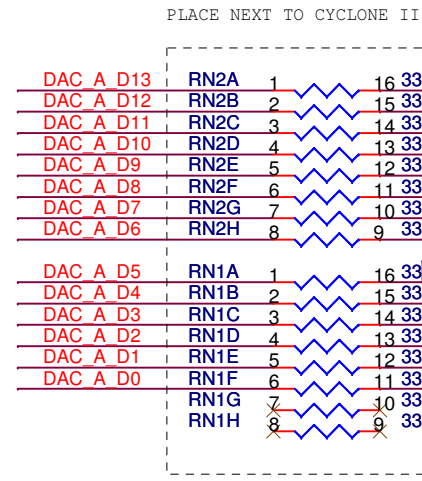
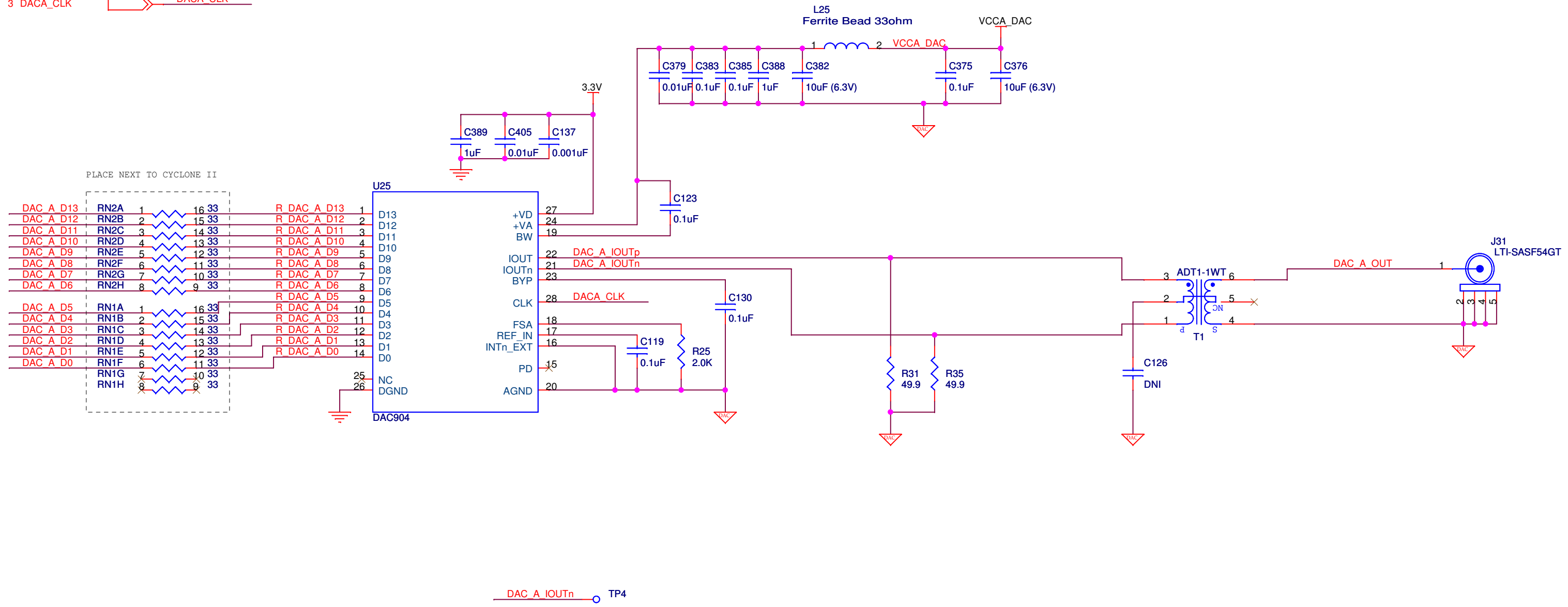
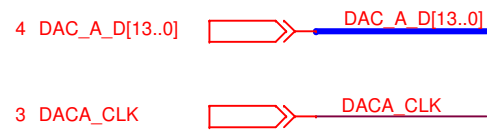
Title: **Cyclone II DSP Board**

Size B Document Number: **150-0310202-B1** Rev **B**

Date: Thursday, March 24, 2005 Sheet 12 of 22



DAC CHANNEL A

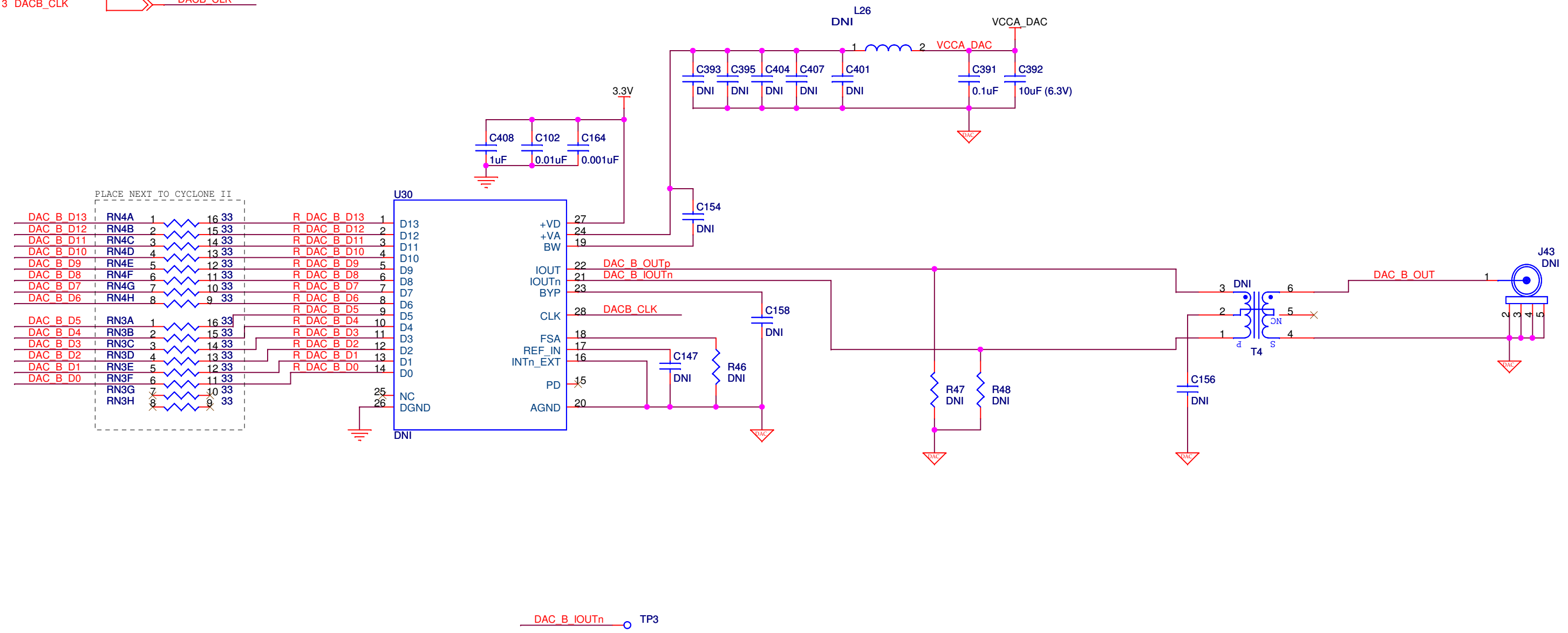


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title		
Cyclone II DSP Board		
Size B	Document Number	Rev B
	150-0310202-B1	
Date:	Thursday, March 24, 2005	Sheet 13 of 22

DAC CHANNEL B

3,4,6 DAC_B_D[13..0] → DAC_B_D[13..0]

3 DACB_CLK → DACB_CLK



DAC_B_IOUTn ○ TP3

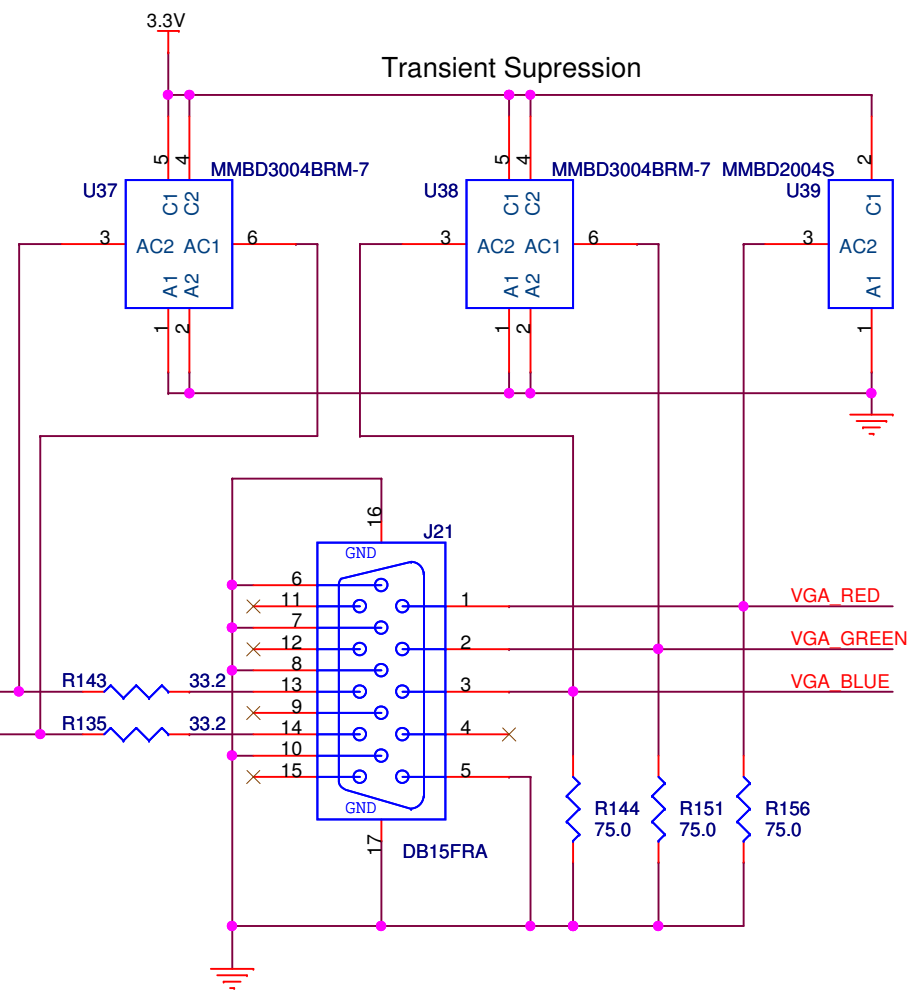
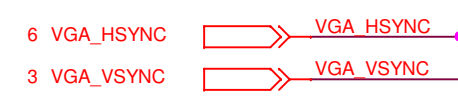
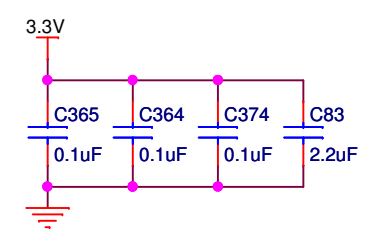
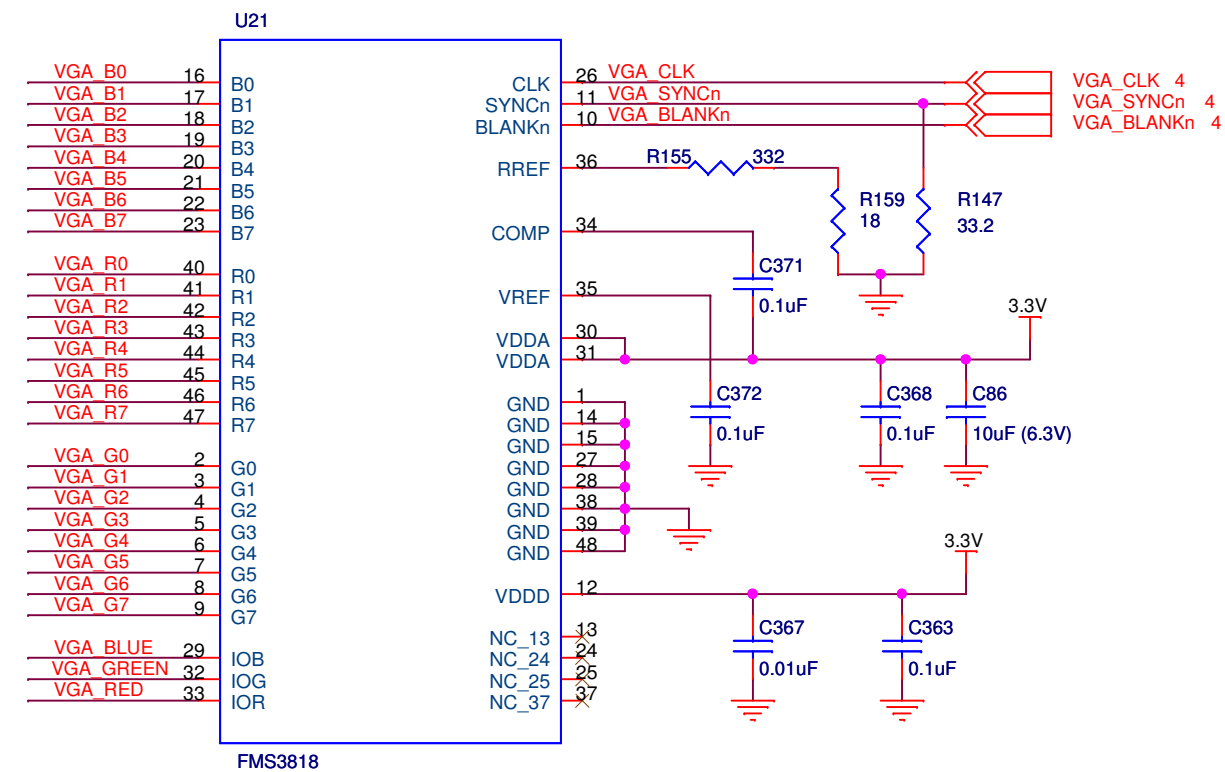
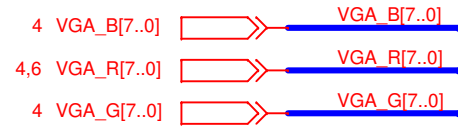
PLACE NEXT TO CYCLONE II

DAC B D13	RN4A	1	16	33	R DAC B D13	1	D13
DAC B D12	RN4B	2	15	33	R DAC B D12	2	D12
DAC B D11	RN4C	3	14	33	R DAC B D11	3	D11
DAC B D10	RN4D	4	13	33	R DAC B D10	4	D10
DAC B D9	RN4E	5	12	33	R DAC B D9	5	D9
DAC B D8	RN4F	6	11	33	R DAC B D8	6	D8
DAC B D7	RN4G	7	10	33	R DAC B D7	7	D7
DAC B D6	RN4H	8	9	33	R DAC B D6	8	D6
DAC B D5	RN3A	1	16	33	R DAC B D4	9	D5
DAC B D4	RN3B	2	15	33	R DAC B D3	10	D4
DAC B D3	RN3C	3	14	33	R DAC B D2	11	D3
DAC B D2	RN3D	4	13	33	R DAC B D1	12	D2
DAC B D1	RN3E	5	12	33	R DAC B D0	13	D1
DAC B D0	RN3F	6	11	33		14	D0
	RN3G	7	10	33			
	RN3H	8	9	33			



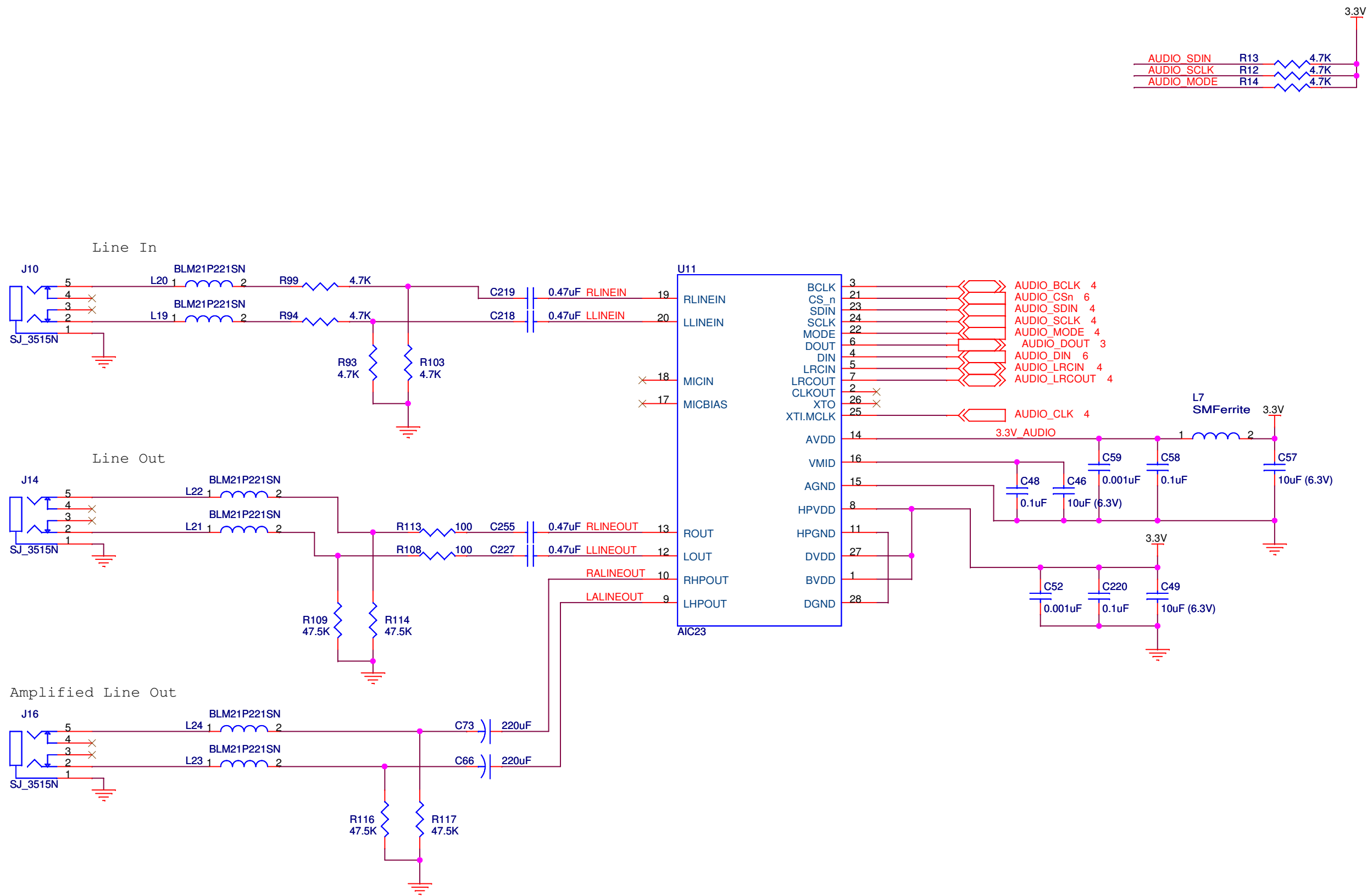
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 14	of 22

VIDEO DAC



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 15	of 22

AIC23 AUDIO CODEC

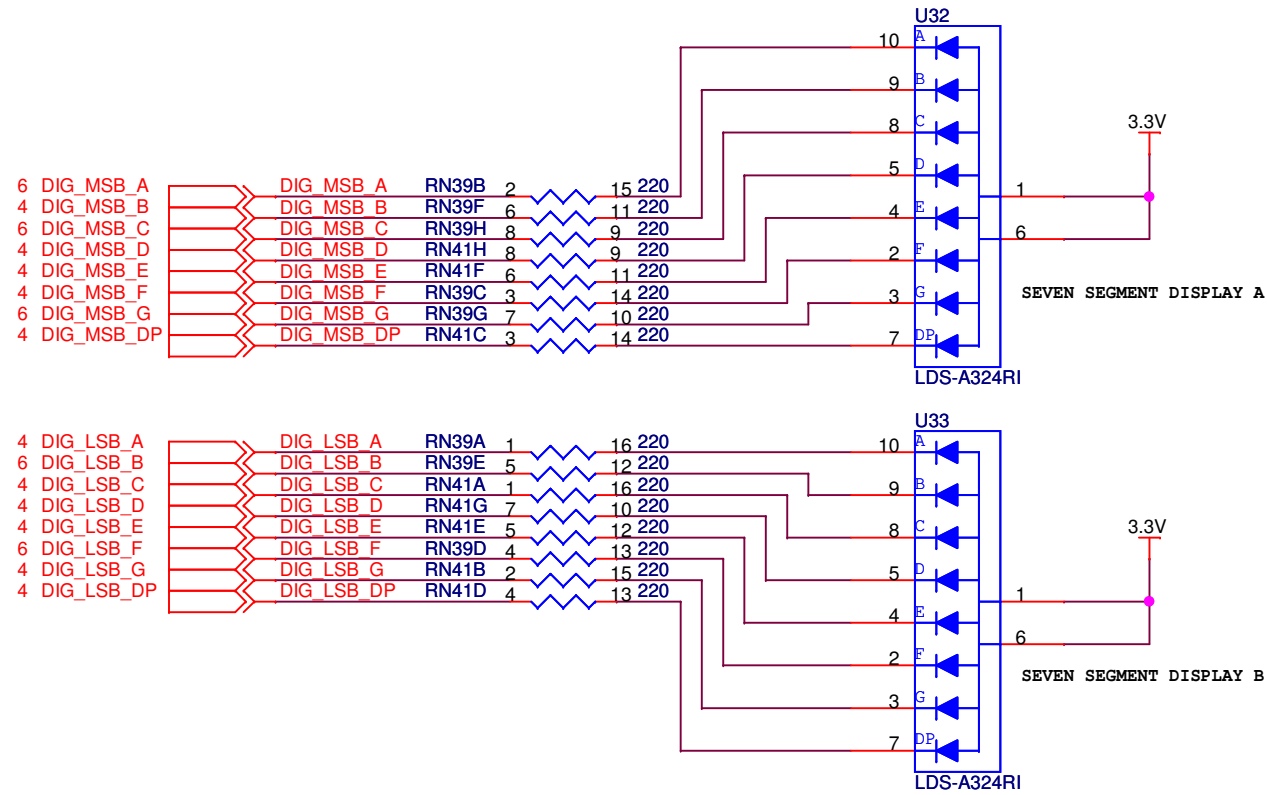


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title		
Cyclone II DSP Board		
Size	Document Number	Rev
B	150-0310202-B1	B
Date:	Thursday, March 24, 2005	Sheet 16 of 22

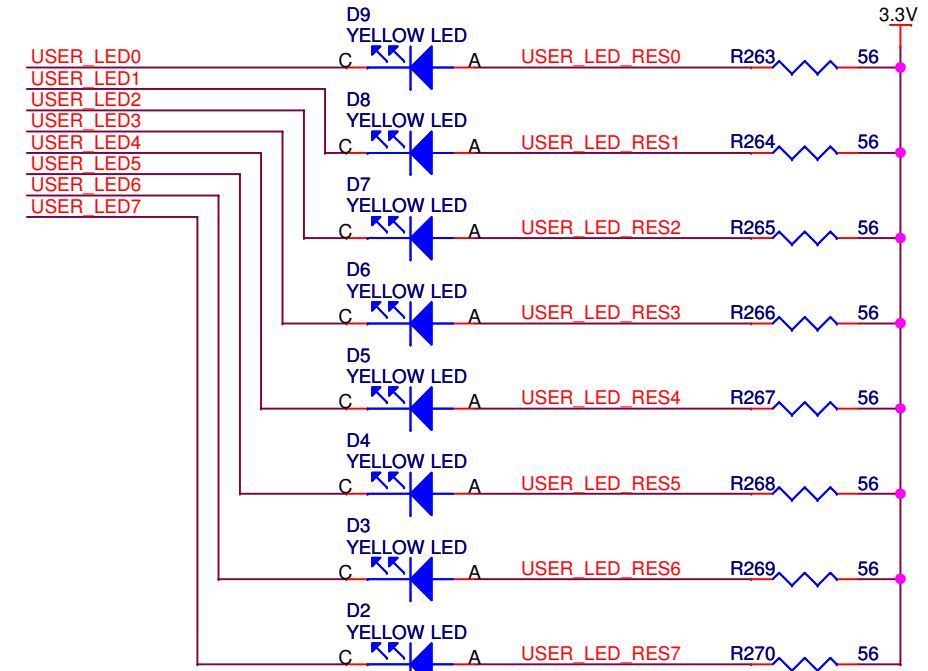


USER IO

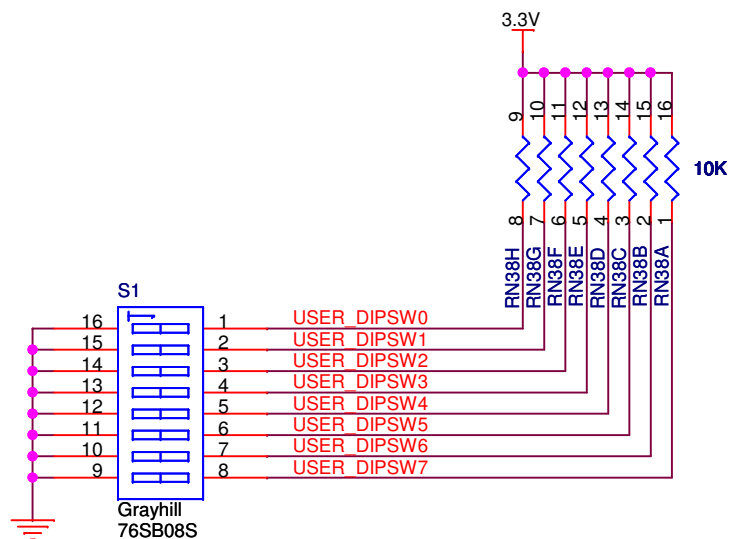
7-Segment Displays



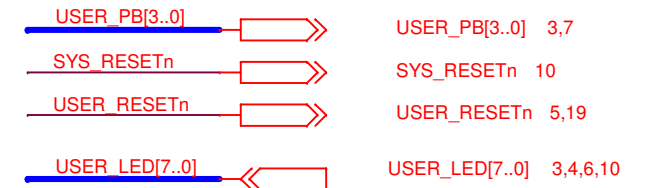
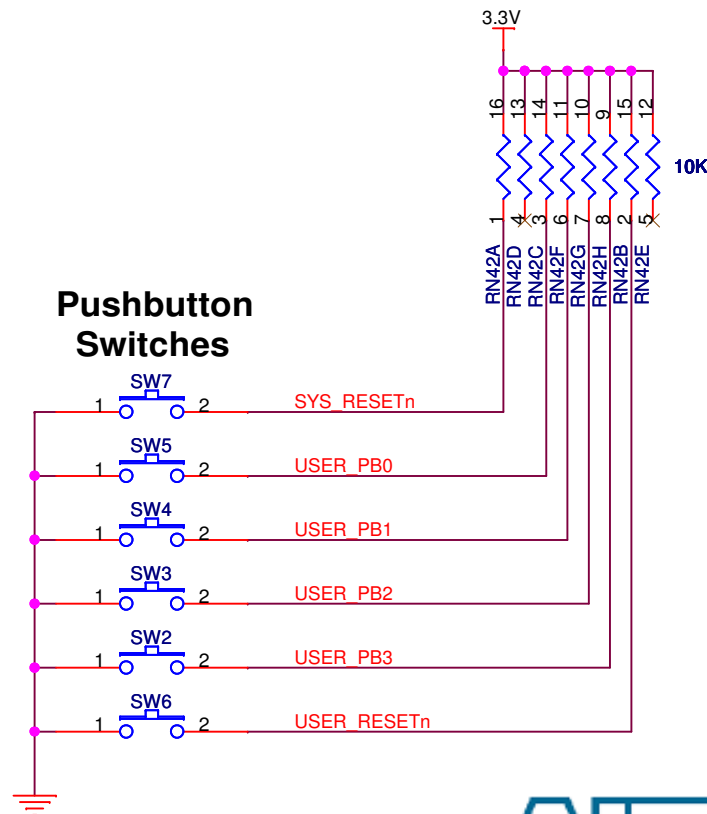
User LEDs



3,5,7 USER_DIPSW[7:0] ← USER_DIPSW[7:0]

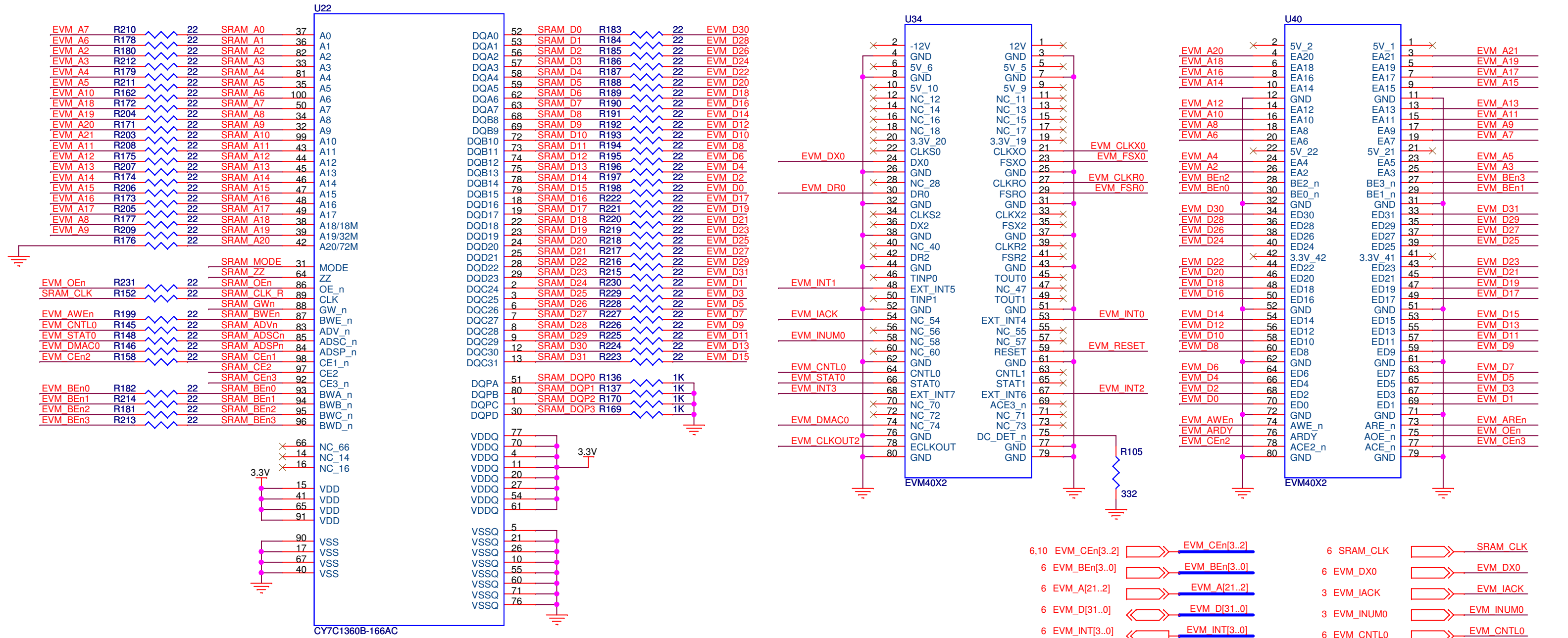


Pushbutton Switches



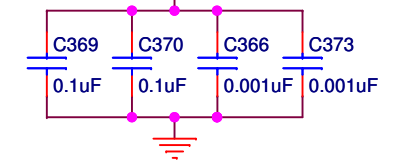
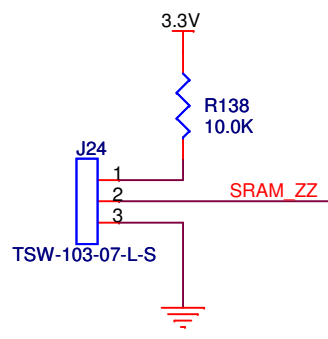
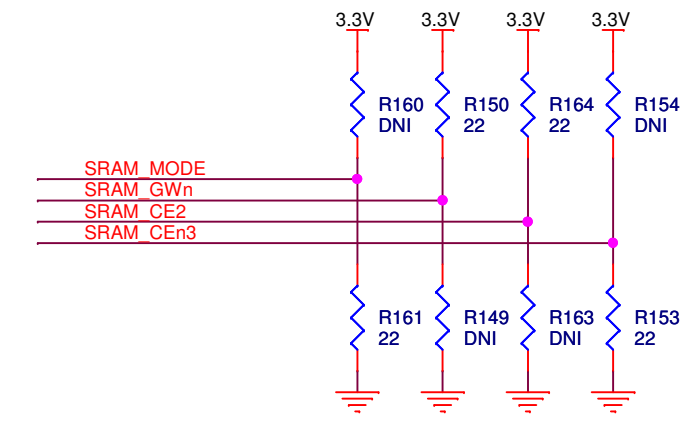
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title Cyclone II DSP Board		
Size B	Document Number 150-0310202-B1	Rev B
Date: Thursday, March 24, 2005	Sheet 17	of 22

SSRAM, TI EVM Connectors



Default SRAM Settings

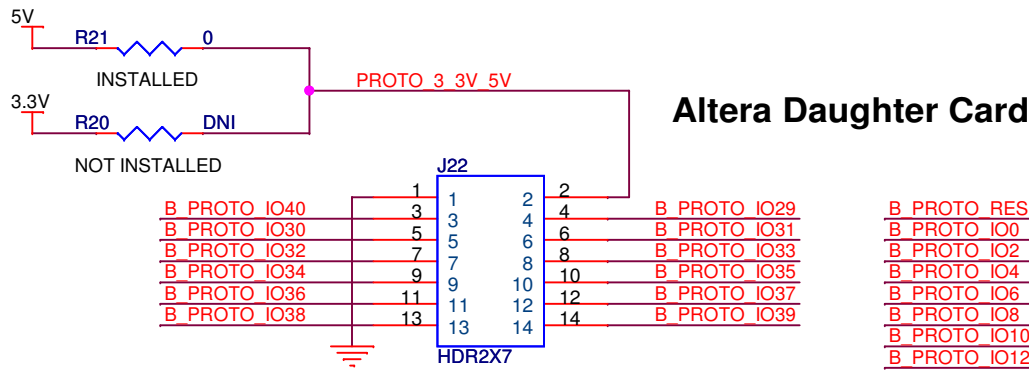
- MODE = Linear Burst (GND)
- GWn = Global Write Disable (VCC)
- CE2 = Always Enabled (VCC)
- CEn3 = Always Enabled (GND)
- ZZ = Always Enabled (jumper GND)



- 6,10 EVM_CEn[3..2] → EVM CEn[3..2]
- 6 EVM_BEEn[3..0] → EVM BEEn[3..0]
- 6 EVM_A[21..2] → EVM A[21..2]
- 6 EVM_D[31..0] → EVM D[31..0]
- 6 EVM_INT[3..0] → EVM INT[3..0]
- 6 EVM_CLKX0 → EVM CLKX0
- 6 EVM_FSX0 → EVM FSX0
- 6 EVM_CLKR0 → EVM CLKR0
- 6 EVM_FSR0 → EVM FSR0
- 6 SRAM_CLK → SRAM CLK
- 6 EVM_DX0 → EVM DX0
- 3 EVM_IACK → EVM IACK
- 3 EVM_INUM0 → EVM INUM0
- 6 EVM_CNTL0 → EVM CNTL0
- 6 EVM_STAT0 → EVM STAT0
- 3 EVM_DMAC0 → EVM DMAC0
- 3 EVM_CLKOUT2 → EVM CLKOUT2
- 3 EVM_RESET → EVM RESET
- 6 EVM_AWEn → EVM AWEEn
- 6 EVM_OEn → EVM OEn
- 3 EVM_AREn → EVM AREEn
- 6 EVM_DR0 → EVM DR0
- 6 EVM_ARDY → EVM ARDY

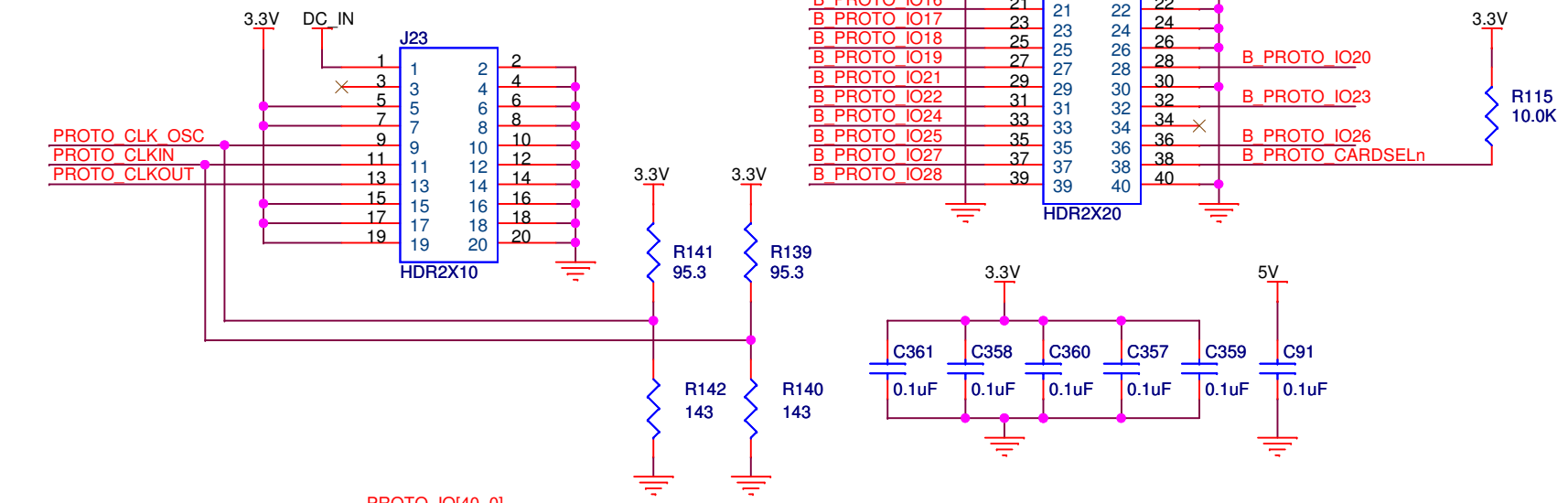
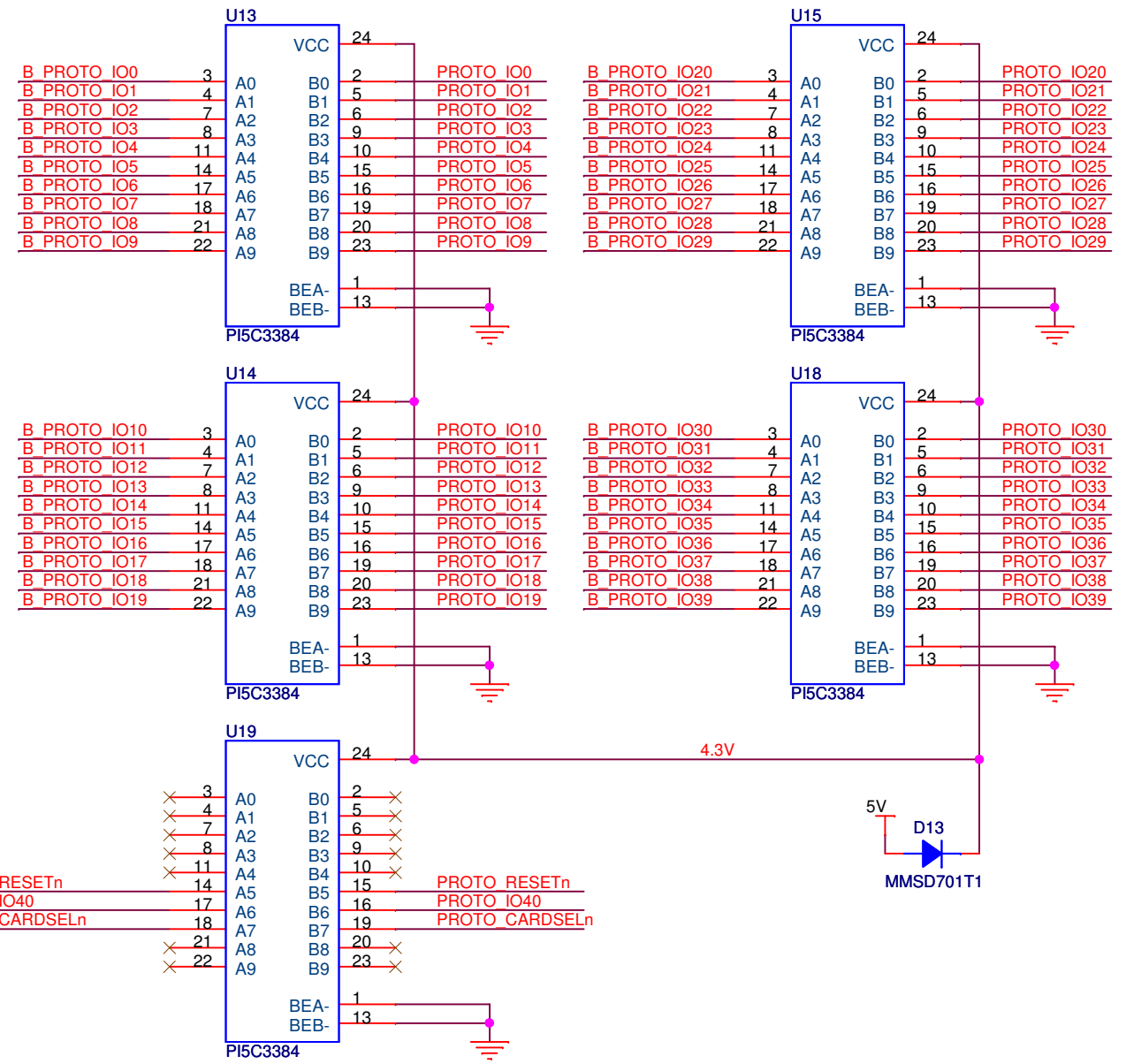


Altera Daughter Card, Mictor Connector

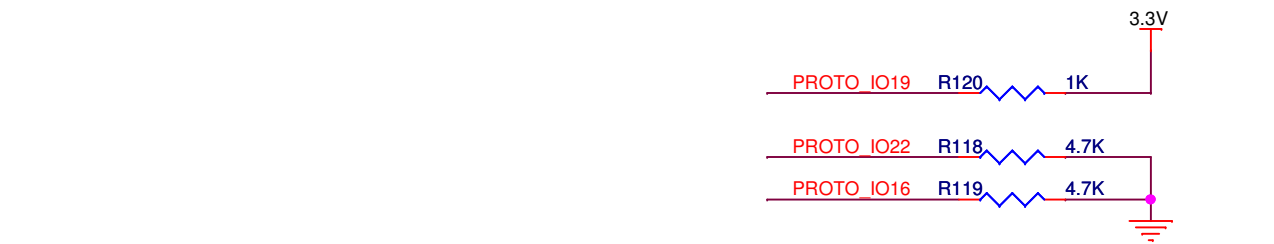
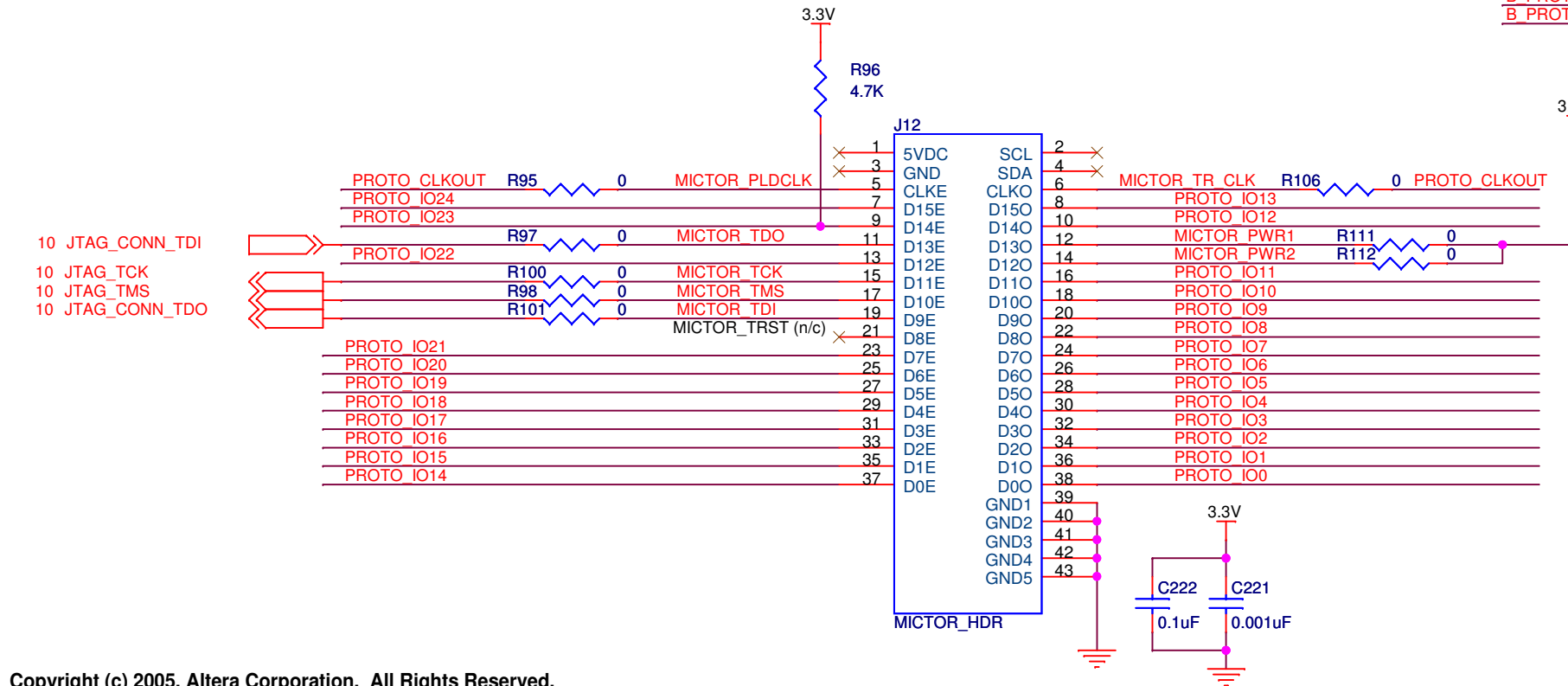
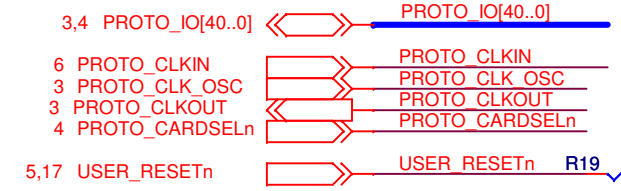


Altera Daughter Card

Altera Daughter Card Voltage Limiters
(for 5V compatibility)

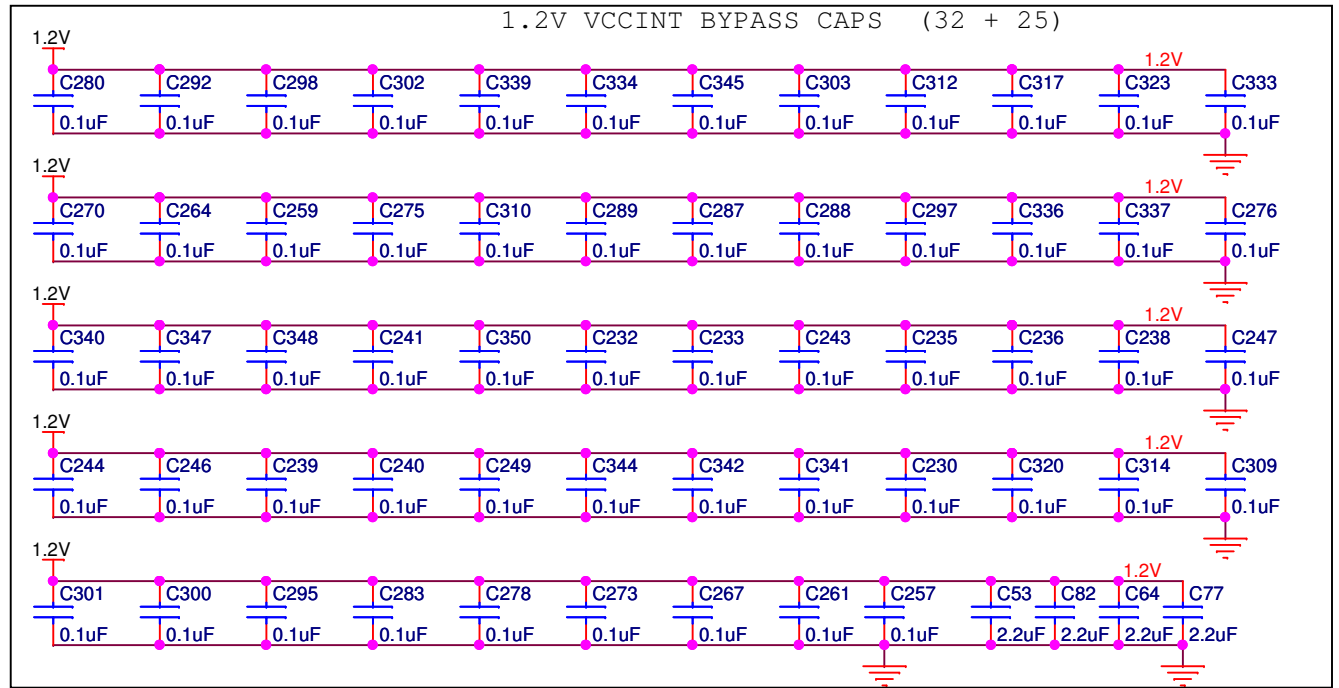
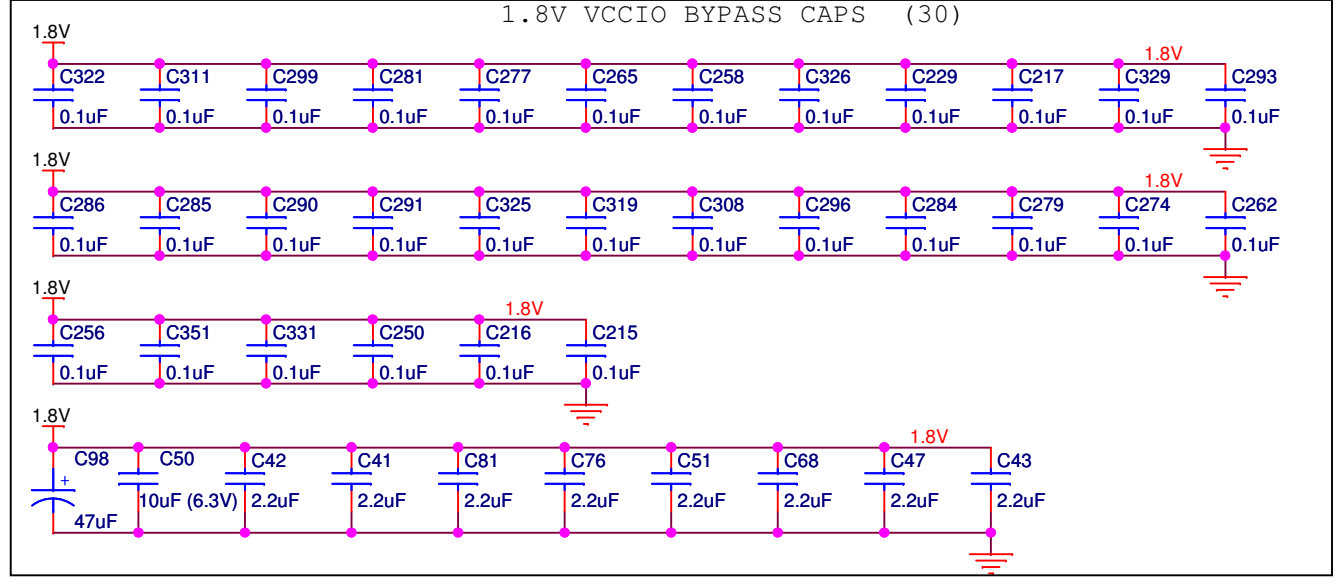
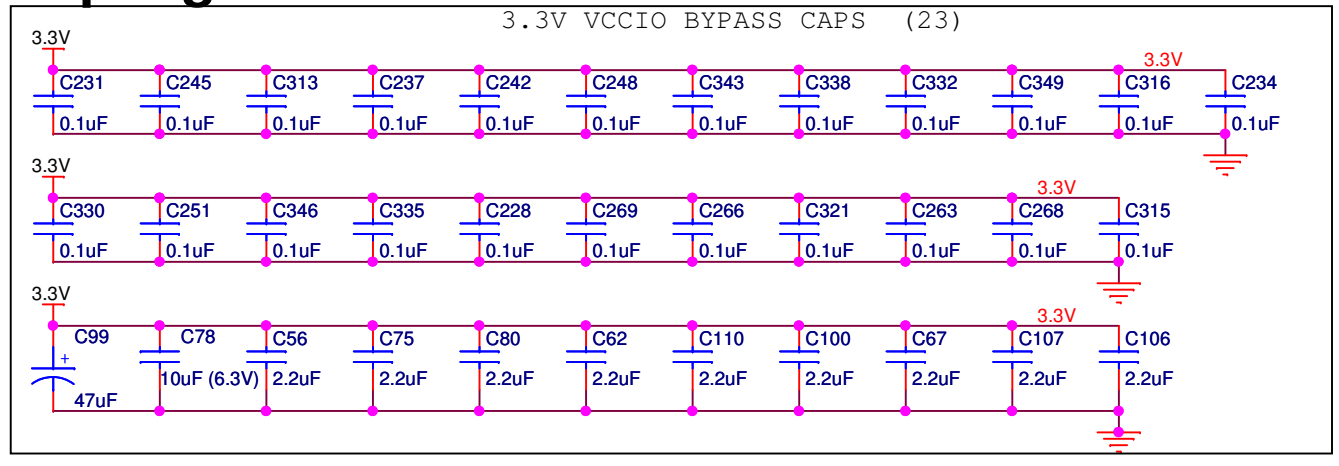
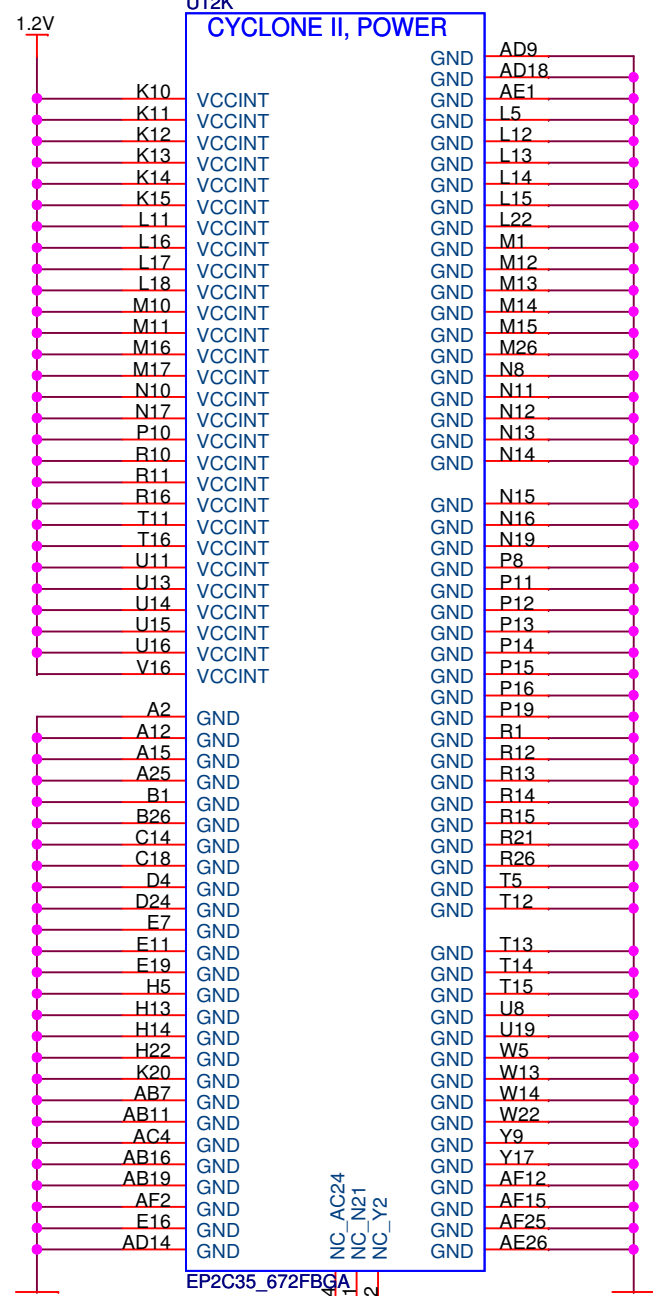
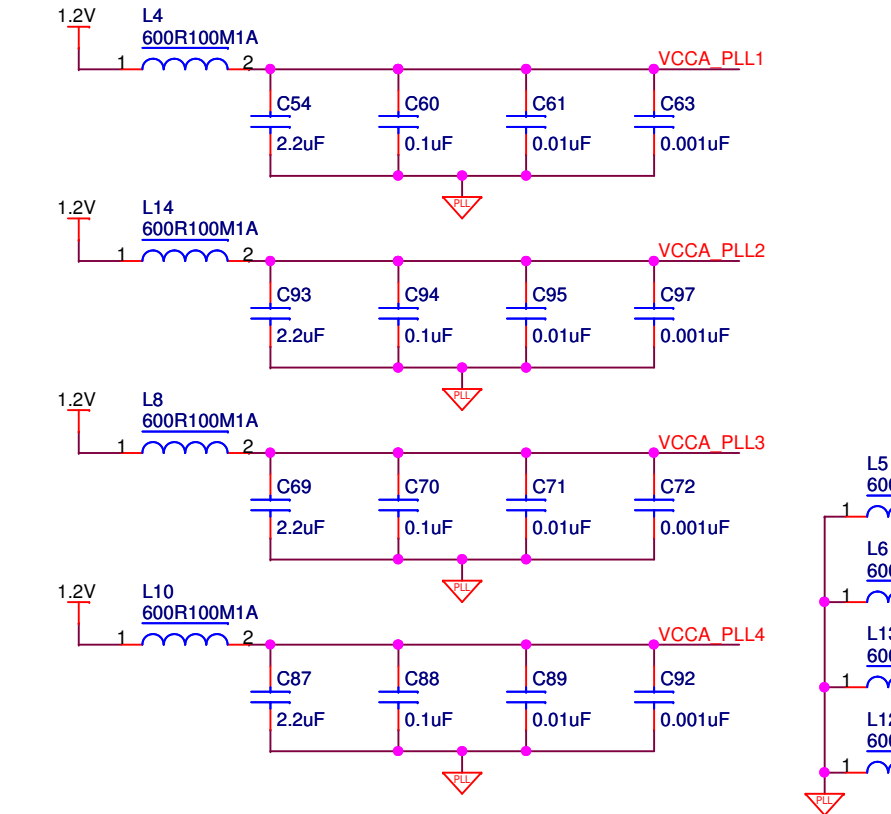
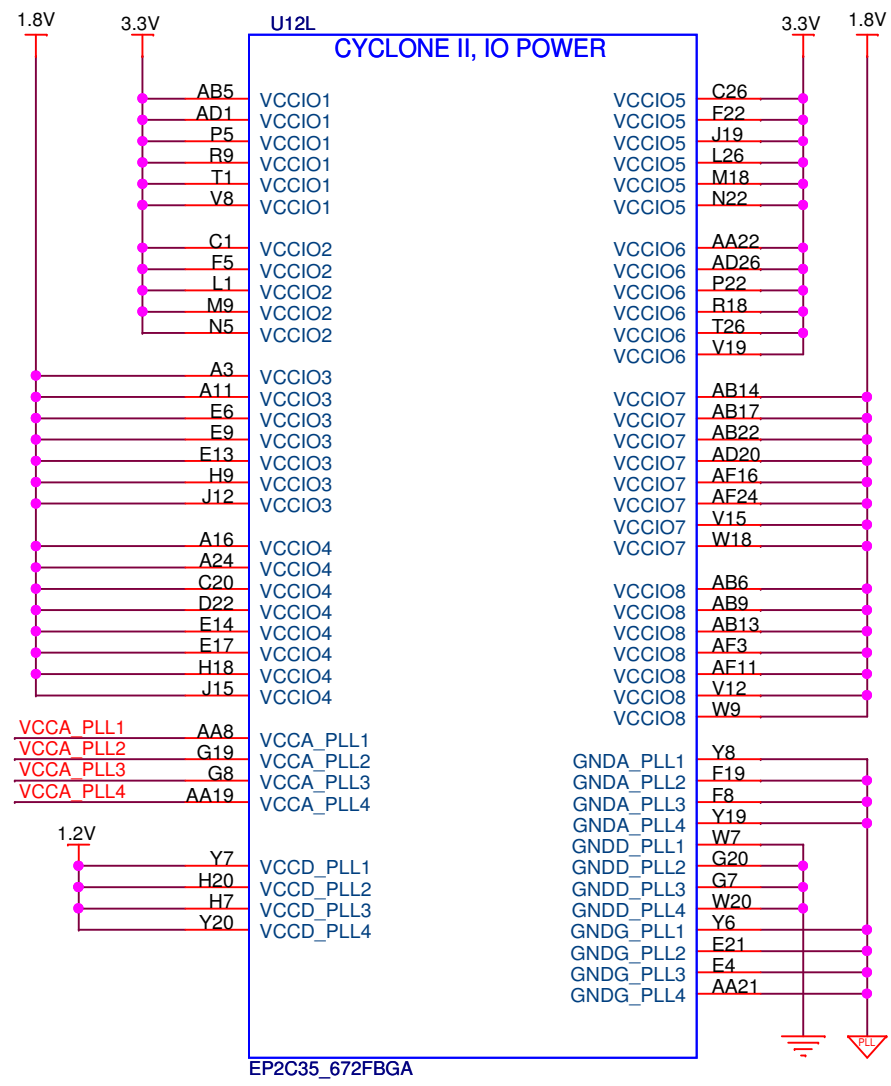


Mictor Connector
(pinned out for FS2 hardware trace module)



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title		
Cyclone II DSP Board		
Size	Document Number	Rev
B	150-0310202-B1	B
Date:	Thursday, March 24, 2005	Sheet 19 of 22

Cyclone II Power & Decoupling

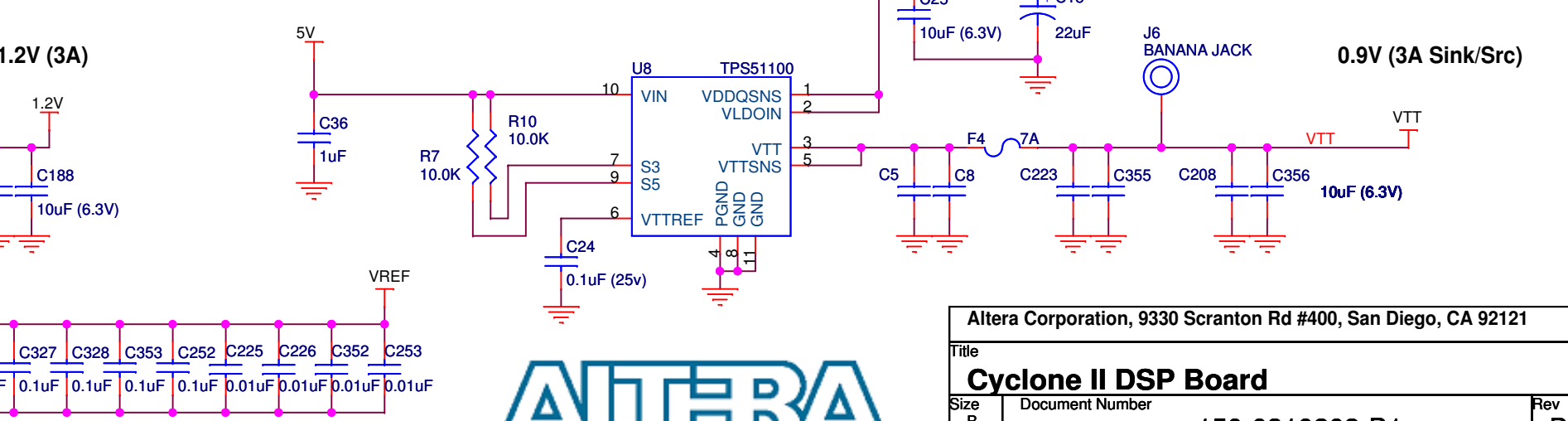
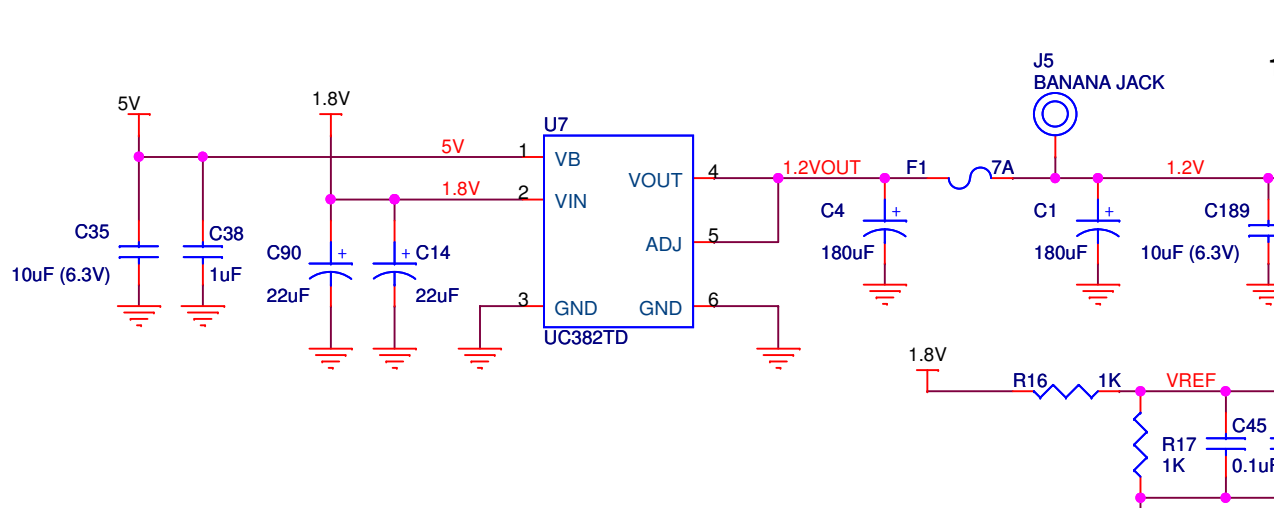
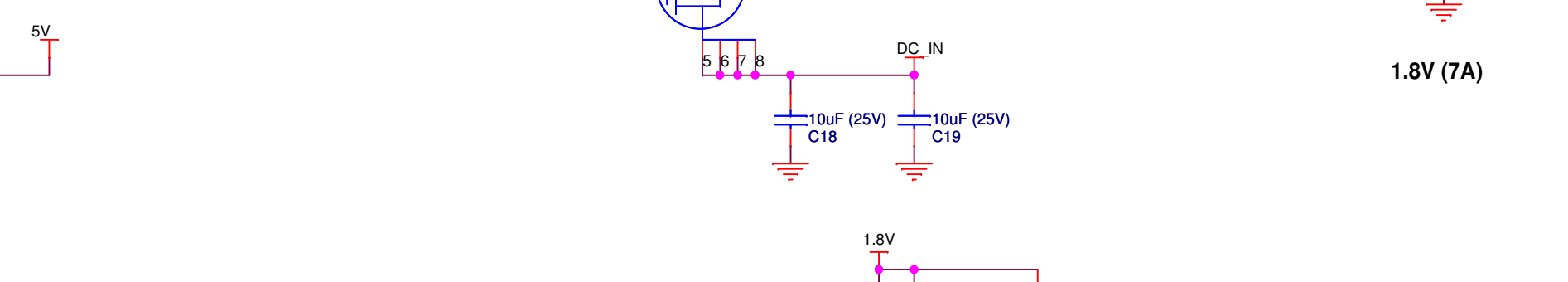
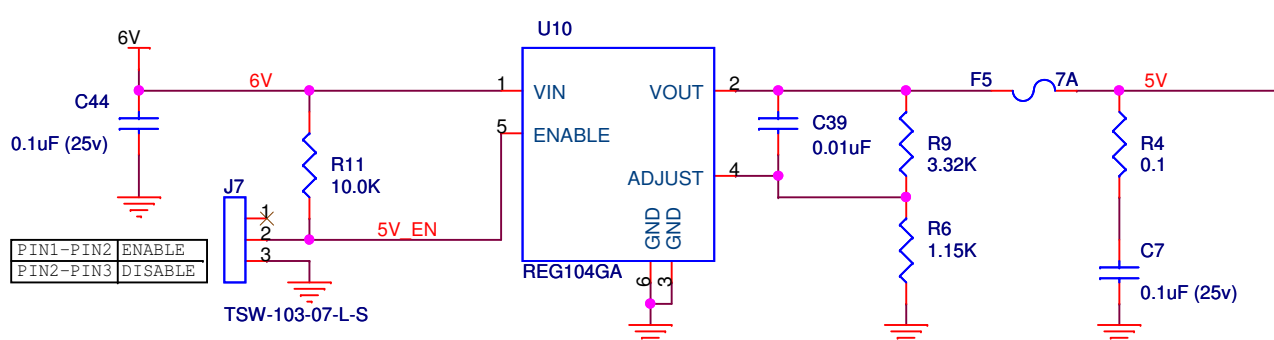
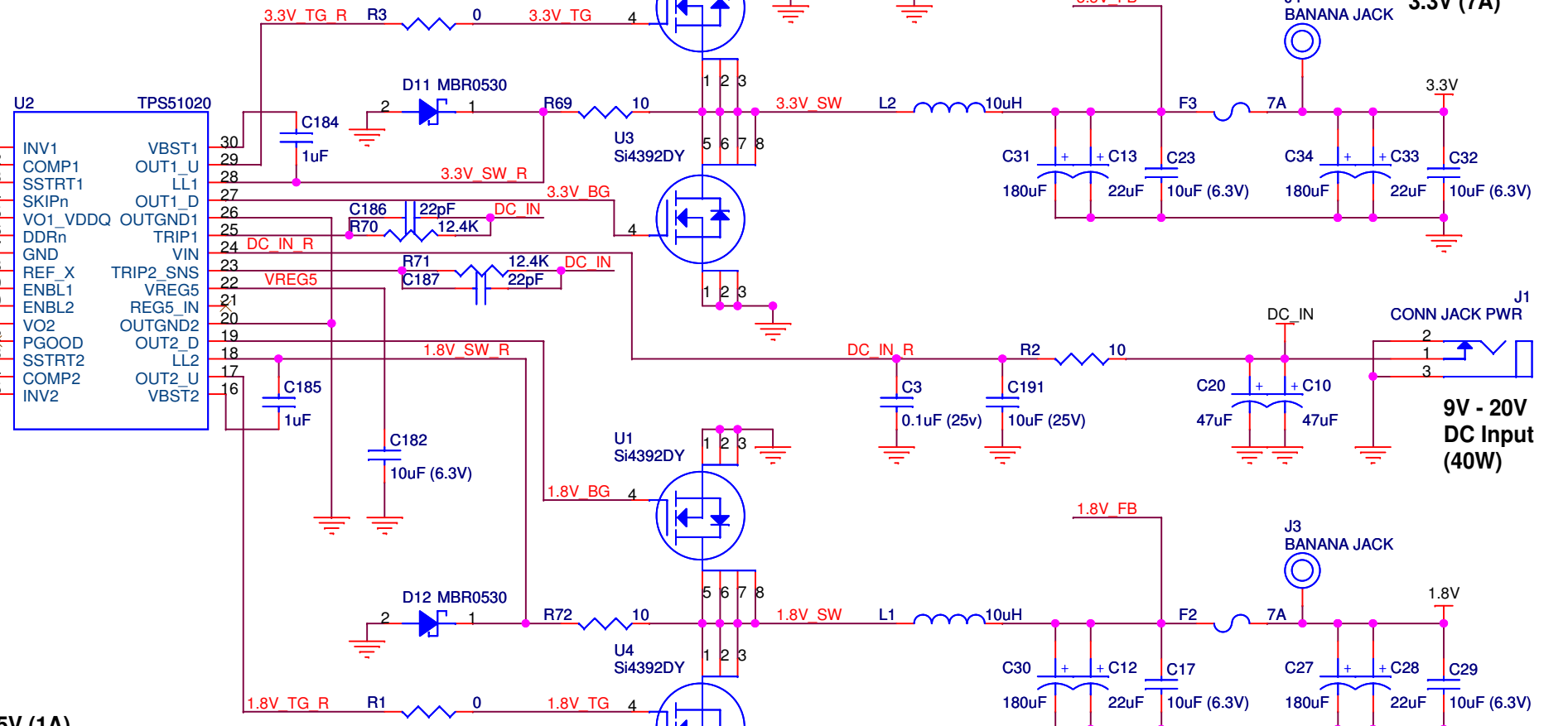
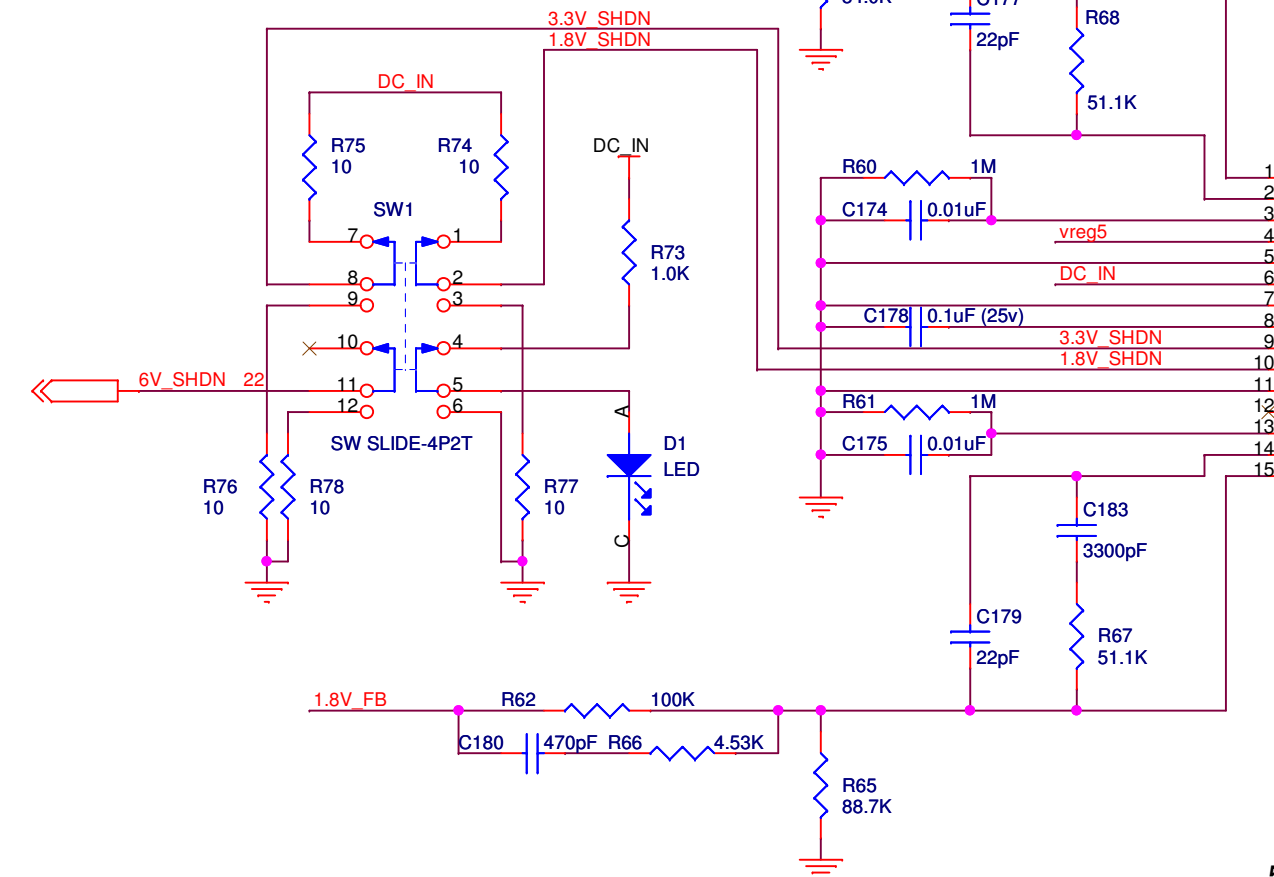


Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title		
Cyclone II DSP Board		
Size B	Document Number	Rev B
Date: Thursday, March 24, 2005		Sheet 20 of 22
150-0310202-B1		



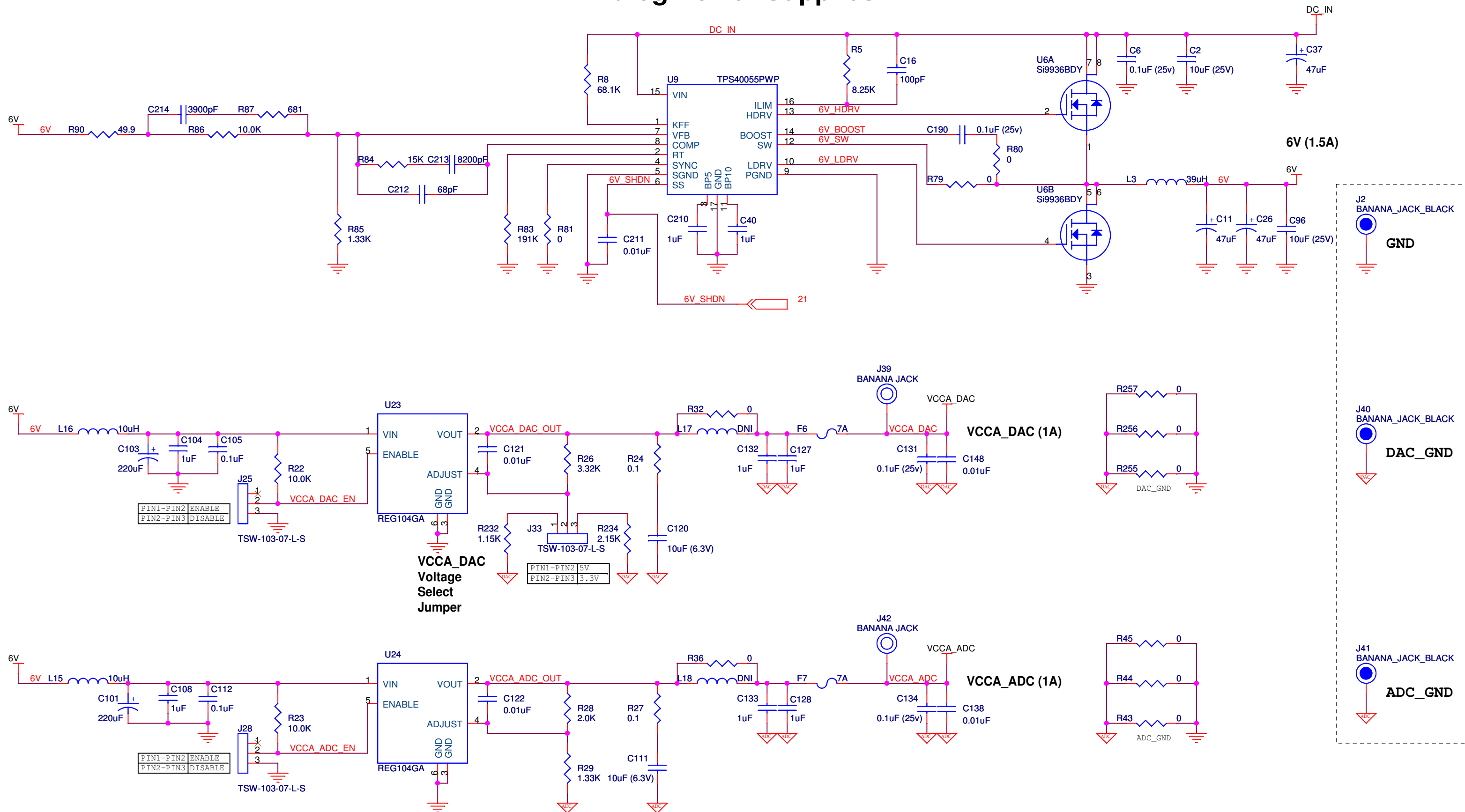
Digital Power Supplies

Main Power Switch



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title	Cyclone II DSP Board	
Size B	Document Number	Rev
	150-0310202-B1	B
Date:	Thursday, March 24, 2005	Sheet 21 of 22

Analog Power Supplies



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title		
Cyclone II DSP Board		
Size B	Document Number	Rev B
	150-0310202-B1	
Date:	Thursday, March 24, 2005	Sheet 22 of 22

