Viterbi Compiler v4.1.0

October 2004, ver. 1.0 Errata Sheet

Introduction

This document addresses known errata and documentation changes for version 4.1.0 of the Viterbi Compiler.

Errata are design functional defects or errors. Errata may cause the Viterbi Compiler to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated into the next version release of the Viterbi Compiler.

Viterbi Compiler 4.1.0 Issues

Altera has identified the following issues that affect the Viterbi Compiler v4.1.0:

1. Polynomials Fail to Update in IP Toolbench
2. Quartus II Warning Notice: A latch is being inferred in Viterbi Compiler
3. IP Toolbench allows invalid combinations of Constraint Length and the Number of ACS Units
4. IP Toolbench gives No Error Message when it cannot overwrite Simulation Data Files
5. IP Toolbench does not check the value of Number of Coded Bits (N) in TCM mode
6. Viterbi Compiler ignores eras_sym Input in Hybrid Architecture (with Node Synchronization Option)
7. Incorporating the Viterbi Compiler and the Reed-Solomon Compiler in the same Quartus II Project produces a conflict with the Source File LPM_pack.vhd

Polynomials Fail to Update in IP Toolbench

The polynomials GA through GG in the IP Toolbench Code Sets tab are not updated correctly to a valid set when other parameters are changed.

Affected Configurations

All configurations are affected.

Design Impact

The polynomial set may not represent a valid convolutional code, so the generated variation does not function as a valid Viterbi decoder.

Work-Around

Set the polynomials manually.

Select the base of the polynomials (decimal or octal) with the radio buttons.

Double click on the value window for each polynomial and replace the value present with the correct value. Press return in every box when you have finished editing the value.

Solution Status

This will be fixed in the next release of the Viterbi Compiler.

Quartus II Warning Notice: A latch is being inferred in Viterbi Compiler

Quartus® II synthesis for the hybrid configuration of the Viterbi Compiler reports the inference of a latch:

```
"Warning: Timing Analysis found one or more latches implemented as
combinational loops.
    Warning: Node
auk_vit_hyb_top_atl:auk_vit_hyb_top_atl_inst|auk_vit_hyb_trb_atl:tracebac
k|dav_shunt~143 is a latch"
```

Affected Configurations

Only the hybrid architecture is affected.

Design Impact

This warning notice can be safely ignored—the synthesized MegaCore® function operates correctly.

Work-Around

No work around is necessary.

Solution Status

This will be fixed in the next release of the Viterbi Compiler.

IP Toolbench allows invalid combinations of Constraint Length and the Number of ACS Units

IP Toolbench allows invalid combinations of the constraint length (`L`) and the number of ACS units parameters.

Affected Configurations

Only the hybrid architecture is affected when the largest value of `L` specified on the Code Sets tab is less than the constraint length specified on the Parameters tab, and the number of ACS units specified on the Parameters tab is too great for the largest value of `L` specified on the Code Sets tab.

Design Impact

Any variation generated with a faulty parameter combination fails to synthesize with the following message during Quartus II analysis and synthesis:

```
Error: Verilog HDL or VHDL error at
auk_vit_hyb_top_atl_arc_rtl.vhd(201): Unconverted
VHDL-1304: assertion always occurs : "Expresion L-2-
LOG2_ceil_table(ACS_units) must be at least 3. Either
reduce ACS_units or increase L"
```

Work-Around

Ensure that the constraint length specified on the Parameters tab is equal to 5 or the largest value of `L` specified on the Code Sets tab, whichever is greater.

Solution Status

This will be fixed in the next release of the Viterbi Compiler.

IP Toolbench gives No Error Message when it cannot overwrite Simulation Data Files

IP Toolbench generates simulation data files that are used by the testbench when simulating the custom variation. If it is unable to overwrite these files, it exits normally without displaying an error message. This situation can happen when a simulator has the previously generated files open while new files are being generated.

Affected Configurations

All configurations are affected.

Design Impact

Simulation results are unpredictable because of the use of incorrect data files. Simulation may generate unexpected results or the simulator may report an error.

Work-Around

Ensure that all simulation data files are writeable when running the Viterbi Compiler IP Toolbench. For example, close any previous simulations that may be using the files.

Solution Status

This will be fixed in the next release of the Viterbi Compiler.

IP Toolbench does not check the value of Number of Coded Bits (N) in TCM mode

The Viterbi Compiler only supports 2 coded bits (N = 2) in Trellis Coded Modulation (TCM) mode. IP Toolbench fails to check that N is always 2 in TCM mode.

Affected Configurations

All configurations using TCM mode are affected.

Design Impact

The generated variation will not perform any useful function.

Work-Around

Do not specify anything other than N = 2 when using TCM mode.

Solution Status

This will be fixed in the next release of the Viterbi Compiler.

Viterbi Compiler ignores eras_sym Input in Hybrid Architecture (with Node Synchronization Option)

When the node synchronization option is selected in the hybrid architecture of the Viterbi Compiler, the `eras_sym input` that indicates the presence of an erased symbol is ignored.

Affected Configurations

The hybrid architecture is affected when the node synchronization option is selected.

Design Impact

The generated variation will not operate correctly when the `eras_sym` input is used. Instead of ignoring the value of the `rr` input when `eras_sym` is asserted, the `rr` input will be treated as a valid input symbol. Erased symbols are used to implement de-puncturing, thus the generated variation operates correctly with unpunctured codes.

Simulation of an affected variation using the supplied pre-compiled ModelSim VHDL models results in the `numerr` output being unknown, whether `eras_sym` is asserted or not.

Work-Around

If you are using punctured codes and therefore using `eras_sym`, you must implement node synchronization (the rotation of the incoming symbols) externally.

If you are using the node synchronization option and not using `eras_sym`, you should simulate your design using the IP functional simulation models instead of the pre-compiled ModelSim VHDL models.

Solution Status

This will be fixed in the next release of the Viterbi Compiler.

Incorporating the Viterbi Compiler and the Reed-Solomon Compiler in the same Quartus II Project produces a conflict with the Source File LPM_pack.vhd

The file **LPM_pack.vhd** is present in the library of both the Viterbi Compiler and the Reed-Solomon Compiler.

Affected Configurations

All configurations are affected.

Design Impact

Quartus II will issue the following error during analysis and synthesis:

```
Error: VHDL package error at LPM_pack.vhd(188): package lpm_components
already exists
```

Work-Around

Remove whichever copy of **LPM_pack.vhd** is lower down on the list of design files in the Quartus II project.

Solution Status

This will be fixed in the next release of the Viterbi Compiler.

Contact Information

For further information, contact Altera's mySupport website at **www.mysupport.altera.com**.

Revision History

Table 1 shows the revision history.

Table 1. Revision History

Version	Date	Details of Change
1.0	September 2004	First release of the Viterbi Compiler errata sheet for version 4.1.0.

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