DSP Development Kit, Stratix II Edition

August 2005, Development Kit version 1.0.0 Errata Sheet

This document addresses known errata and documentation changes for the DSP Development Kit, Stratix® II Edition version 1.0.0.

Errata are design functional defects or errors. Errata may cause the board or designs in this DSP Development Kit, Stratix II Edition to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions, or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated into an upcoming release of the DSP Development Kit, Stratix II Edition.

DSP Development Kit, Stratix II Edition 1.0.0 Issues

Altera has identified the following issues that affect the DSP Development Kit, Stratix II Edition.

When Using Quartus II Software Version 4.2 or Later Versions, Programming Failure Is Reported During JTAG Programming on the 2S60 DSP Development Board

On the Stratix II DSP board, configuration of the FPGA via JTAG fails when you use the Quartus® II software version 4.2 or higher, if switch4 is set to the **Open** state on DIP switch SW2. The Quartus II software version 4.2 or higher incorrectly reports that the device programming was unsuccessful.

Affected Configurations

This failure is observed on all Stratix II DSP boards when you configure the FPGA via JTAG using the Quartus II software version 4.2 or later and switch4 on DIP switch SW2 is set to the **Open** state.

Design Impact

This error occurs because the expected user programming file is not loaded into the FPGA. The factory configuration is loaded into the FPGA instead of the user programming file.

Workaround

Set switch4 of DIP switch SW2 to the **Closed** position before programming the FPGA.

Solution Status

There are no planned changes for this problem.

The Write2Flash Utility, Referenced by the *Stratix II EP2S60 DSP Development Board Data Sheet*, Is Not on the Kit CD-ROM

In the Stratix II EP2S60 DSP Development Board Data Sheet, in the Non-Volatile Configuration section, the Write2Flash utility is mentioned as a tool you can use to download user configuration data into the on-board flash. The new method is to use the Nios® II Flash Programmer through the Nios II SDK Shell.

Affected Configurations

This Write2Flash utility is mentioned in versions 1.0 and 1.1 of the *Stratix II EP2S60 DSP Development Board Data Sheet*.

Design Impact

There is no design impact.

Workaround

Use the Nios II Flash Programmer from the Nios II SDK Shell to download configurations into the on-board flash. See the example instructions below.

Refer to the *Nios II Flash Programmer User Guid*e for more detailed instructions on using the Nios II Flash Programmer.

Example instructions for programming the 2S60 DSP board.

1. Generate a flash file to load into the flash device.
2. Run the Nios II SDK Shell.
3. Change directories to the project location.
4. Run the **sof2flash** utility:

   ```
   $ sof2flash --input=<project_name>.sof --output
   =<project_name>.flash --offset=0x00500000
   ```

   Use the offset switch to specify which configuration area of the flash will be loaded. Use `0x00500000` for `User 0` area, `0x00800000` for `User 1` area, or `0x00C00000` for `User 2` area.
5. Copy the flash file into the on-board flash device.
6. Move a copy of the flash programming **SOF** file to your project directory. The **SOF** file is in the directory:

   ```
   <NIOS_Install_Directory>\components
   \altera_nios_dev_board_stratix_2s60_es\system
   \altera_nios_dev_board_stratix_2s60_es.sof
   ```
7. Run the Nios II Flash Programmer (nios2-flash-programmer) utility:

   ```
    $ nios2-flash-programmer --base=0x01000000 input
   =<project_name>.flash -sof
   =altera_dsp_dev_board_stratix_2s60.sof --device=1
   ```

Solution Status

Future releases of this kit will correct the *Stratix II EP2S60 DSP Development Board Data Sheet*.

The FFT Co-Processor Reference Design Reports an Error When Compiling With the Quartus II Software Versions 4.2 or Later.

When compiling the FFT Co-processor in the Quartus II software versions 4.2 or later (with or without Service Pack 1), the compiler reports the following error:

```
Error: Verilog HDL error at atlantic_fifo.v(372):
variable "fifo_wr_mty" has mixed blocking and
nonblocking Procedural Assignments -- must be all
blocking or all nonblocking assignments
```

Affected Configurations

This failure is observed with the Quartus II software versions 4.2 or later. The Quartus II software version 4.1 Service Pack 2 does not report this error.

Design Impact

You cannot compile the FFT Co-processor demo with versions of the Quartus II software after version 4.1 Service Pack 2.

Workaround

Replace the **atlantic_fifo.v** file, which after you install the kit from the CD is in the directory:

```
<install_path>\Examples\HW\ReferenceDesigns
\emif_ref_design_FFT\example\source
```

You can download a replacement file from this FTP location:

```
ftp://ftp.altera.com/outgoing/devkit/DSP_DK_2S60
/DSP-2S60_FFT_fix_Q4p2.zip
```

Solution Status

Downloading the replacement file fixes the problem.

DACs are AC Coupled, Not DC Coupled as the Stratix II EP2S60 DSP Development Board Data Sheet Indicates

Figure 5, *On-Board Circuitry after D/A Converter*, in version 1.0.0 of the *Stratix II EP2S60 DSP Development Board Data Sheet* is incorrect. This circuit is AC coupled, not DC coupled.

Solution Status

This figure is correct in version 1.1.0 of the *Stratix II EP2S60 DSP Development Board Data Sheet*.

Stratix II EP2S60ES Devices Do Not Support MRAM Byte Enables

Stratix II EP2S60ES devices have a silicon problem that prevents the use of byte enables on MRAM blocks. For details, refer to the *Stratix II FPGA Family Errata Shee*t available on Errata page of the Altera world-wide web site (http://www.altera.com/literature/lit-es.jsp). This issue prevents the Quartus II software from allowing you to directly instantiate an MRAM block with byte enables in designs targeting EP2S60ES devices.

Affected Configurations

This issue affects designs with EP2S60ES devices.

Design Impact

No support exists for byte enables on MRAM blocks in designs using Stratix II EP2S60ES devices.

Workaround

Stratix II production devices (non-ES devices) support MRAM byte enables.

Solution Status

This issue is fixed in version 1.1.0 of the *Stratix II EP2S60 DSP Development Board Data Sheet*.

Typographical Error, J23 Pin 5 is Connected to P32, Not R32

Figure 11, *Expansion Protoytpe ConnecytorPin - J23, J24, J25* (page 46) in the *Stratix II EP2S60 DSP Development Board Data Sheet* shows J23 pin 5 is connected to pin R32 on the Stratix II device. The pin name in this figure is incorrectly labelled R32 instead of being correctly labelled P32. J23 pin 5 is connected to pin P32 on the Stratix II device.

Affected Configurations

Applies to all Stratix II DSP boards.

Design Impact

Ther eis no design impact. This problem is a documentation typographical error.

Workaround

Ensure that you assign the pin in your project to P32, not R32.

Solution Status

This will be fixed in the next revision of the data sheet.

Contact Information

For more information, contact Altera's mySupport web site at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the DSP Development Kit, Stratix II Edition version 1.0.0 errata sheet revision history.

Table 1. DSP Development Kit, Stratix II Edition Errata Sheet Revision History

Version	Date	Details of Change
1.0.0	April 2005	• "When Using Quartus II Software Version 4.2 or Later Versions, Programming Failure Is Reported During JTAG Programming on the 2S60 DSP Development Board" on page 2. • "The Write2Flash Utility, Referenced by the Stratix II EP2S60 DSP Development Board Data Sheet, Is Not on the Kit CD-ROM" on page 2. • "The FFT Co-Processor Reference Design Reports an Error When Compiling With the Quartus II Software Versions 4.2 or Later." on page 4. • "DACs are AC Coupled, Not DC Coupled as the Stratix II EP2S60 DSP Development Board Data Sheet Indicates" on page 5. • "Stratix II EP2S60ES Devices Do Not Support MRAM Byte Enables" on page 5. "Stratix II EP2S60ES Devices Do Not Support MRAM Byte Enables" on page 5
1.1.0	August 2005	Addtional Item: "Typographical Error, J23 Pin 5 is Connected to P32, Not R32" on page 6

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