SerialLite MegaCore Function

Introduction

This document addresses known errata and documentation changes for version 1.1.0 of the SerialLite MegaCore® function.

Errata are design functional defects or errors. Errata may cause the SerialLite MegaCore function to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated into an upcoming release of the SerialLite MegaCore function.

SerialLite MegaCore Function v1.1.0 Issues

Altera has identified the following issues that affect the SerialLite MegaCore function v1.1.0:

1. "The Quartus II Software Does Not Merge Transmit Phase-Lock Loops (PLLs) for Multiple Function Instantiations" on page 1.

2. "The Demonstration Testbench Fails in Unbalanced Configurations" on page 2.

The Quartus II Software Does Not Merge Transmit Phase-Lock Loops (PLLs) for Multiple Function Instantiations

The Quartus® II software reports a *no-fit* for designs where more than one SerialLite MegaCore function is instantiated in each quad bank of serial inputs and outputs (I/Os). The Quartus II software consumes one ALTGXB transmitter PLL per instantiation, and does not merge the transmit PLLs even if the same reference clock is connected to each instantiation.

Affected Configurations

This issue affects single-lane and dual-lane variations that include more instantiations than the device ALTGXB transmitter PLLs.

Design Impact

Only a single instantiation can be used per quad bank of serial I/Os.

Workaround

The SerialLite top-level file can be modified to instantiate multiple SerialLite protocol core engines connected to a single `ALTGXB` transmitter PLL. The `ALTGXB` transmitter PLL can be configured to match the desired number of lanes. Each protocol core instantiation then connects to the associated bits on the `ALTGXB` transmitter PLL. Submit a **mySupport** request for help with this workaround.

Solution Status

This issue will be fixed in the next release of the SerialLite MegaCore function, requiring the Quartus II software version 5.1.

The Demonstration Testbench Fails in Unbalanced Configurations

The Verilog HDL demonstration testbench included with the SerialLite MegaCore function loops the high-speed serial interface from the transmitter (`TX_OUT[]`) to the receiver instantiation (`RX_IN[]`). If the receiver and transmitter MegaCore functions do not have matching configurations (for example: CRC-32 payload protection for the transmitter, but no CRC payload protection for the receiver), the testbench fails.

Affected Configurations

This issue affects all variations of the MegaCore function.

Design Impact

The demonstration testbench reports an error, and indicates that the testbench has failed.

Workaround

No workaround is available for this issue. For unbalanced configurations, you must create an environment that uses two independent SerialLite MegaCore functions.

Solution Status

This issue will be fixed in the next release of the SerialLite MegaCore function.

Contact Information

For more information, go to Altera's mySupport website at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the revision history.

Table 1. Revision History

Version	Date	Details of Change
1.0	August 2005	First release of the SerialLite MegaCore Function errata sheet for v1.1.0.