This document addresses transceiver-related known errata for the Stratix® GX FPGA family production devices.

For more information on Stratix GX device errata, refer to the "Stratix Family Issues" section in the *Stratix FPGA Family Errata Sheet*.

Receiver Phase Compensation FIFO

Byte misalignment may happen in the double width mode (16-bit or 20-bit) on the received data in certain configurations of the gigabit transceiver block. On the transmit side, the byte ordering is specified to always shift the bits from the least significant byte to the most significant byte. On the receive side, this yields a possibility of two variations of the ordering, depending on where the comma falls in respect to when a clock recovery unit locks. These two variations are described in the *Stratix GX Transceiver User Guide*.

However, if a free running synchronous clock is connected to the `rx_coreclk` port and the gigabit transceiver block receiver is configured to be in double width mode, the byte ordering can have six possible combinations. The reordering happens when the receiver is coming out of the `rxdigitalreset`. Any byte misalignment that happens at this time will not subsequently change unless the reset is asserted again.

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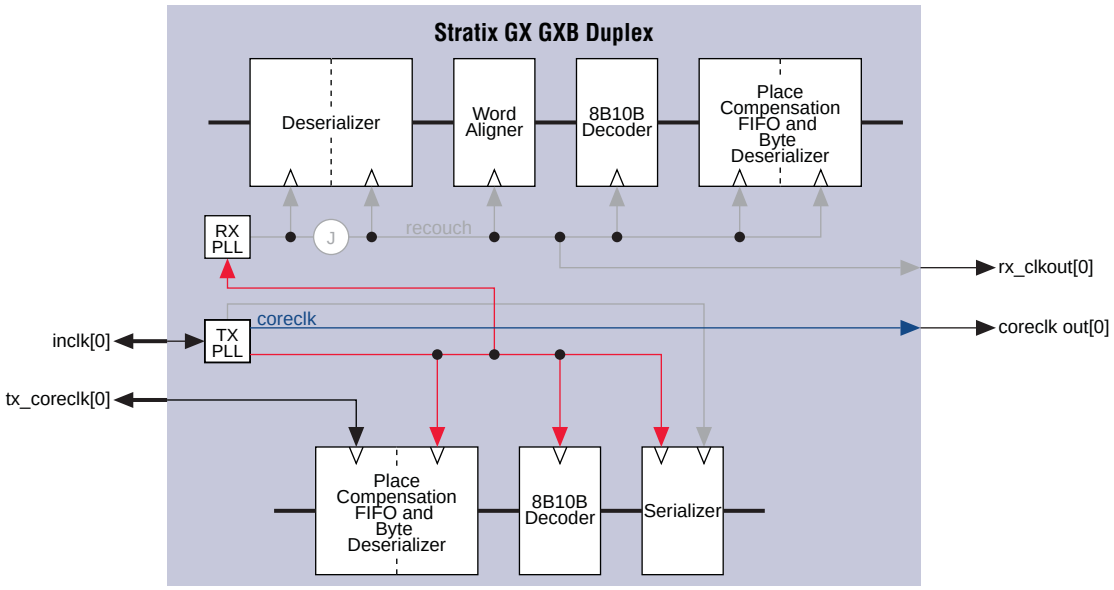
This problem only occurs if the read clock of the phase compensation FIFO of a channel is fed from a clock source other than its own recovered clock. For example, Figure 1 shows a clock configuration that avoids this problem.

Figure 1. Gigabit Transceiver Block Clock Configuration that Does Not Cause Byte Misalignment Problem



From Figure 1, the recovered clock (`rx_clkout[0]`) is fed to both the read and write clocks of the phase compensation FIFO. This is the default configuration of ALTGXB megafunction. The Quartus® II software automatically routes the clocks into both sides of the FIFO to ensure that proper timing is met.

Figure 2 and Figure 3 show clocking schemes with potential byte misalignment problems.

Figure 2. Gigabit Transceiver Block Clock Configuration that can Potentially Cause Byte Misalignment Problem, Example 1

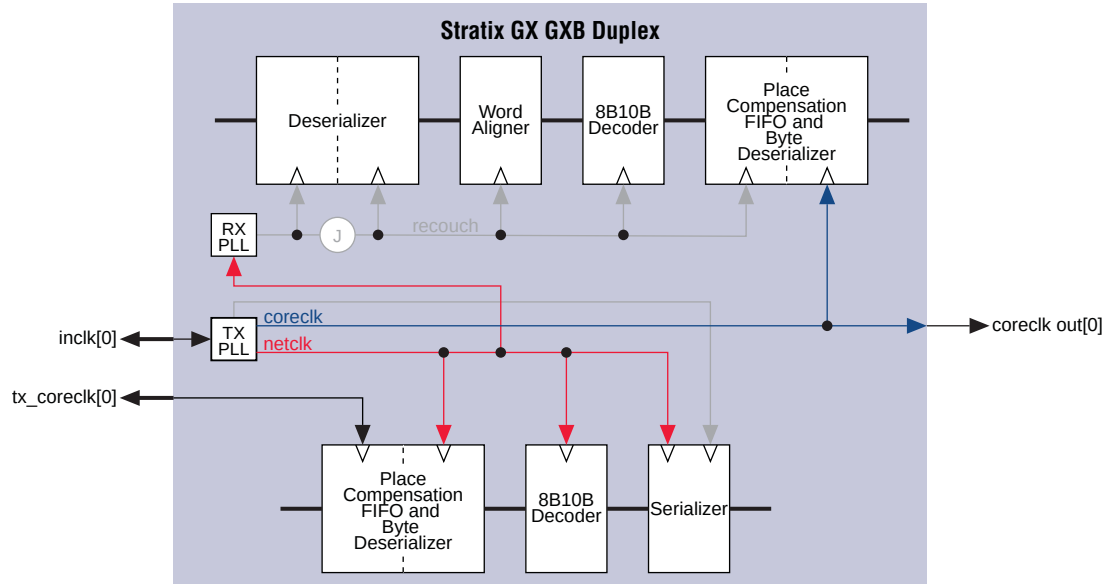
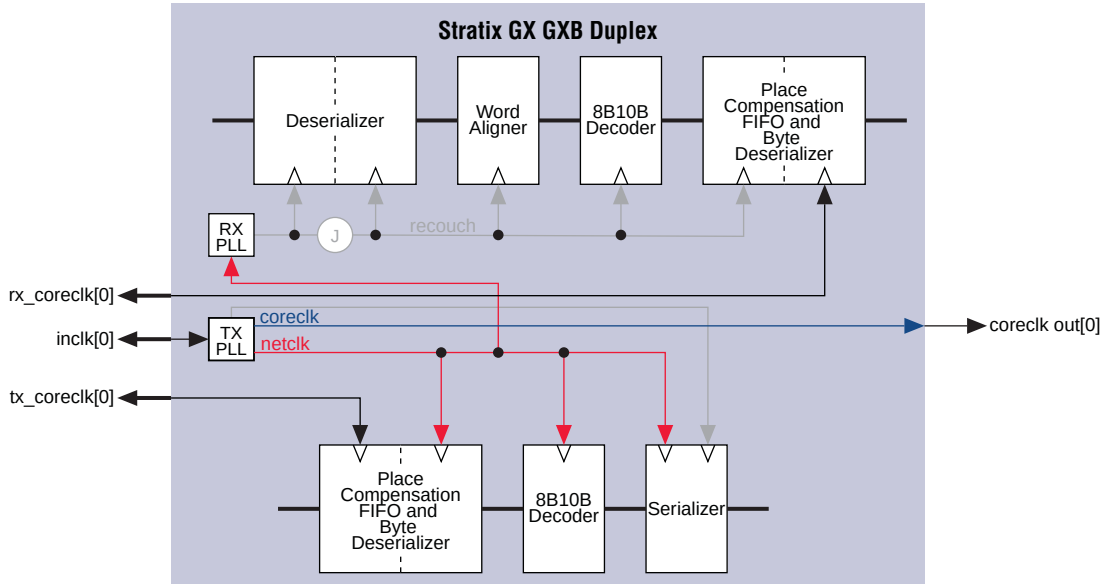


Figure 3. Gigabit Transceiver Block Clock Configuration that can Potentially Cause Byte Misalignment Problem, Example 2

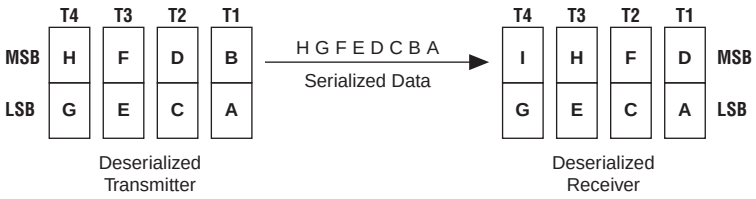


The clocking configurations in Figure 2 and Figure 3 can only work if both the read and write clocks to the phase compensation FIFOs are of the same frequency. Take proper precautions to ensure that there is no frequency variation anytime after the link has been initialized. This means that you must perform a receiver digital reset via the `rxdigitalreset` signal to ensure that the pointers within the receiver phase compensation FIFO are properly spaced.

If you are using these clocking configurations, you must be aware that, in these configurations, the output byte alignment can potentially vary between six different permutations. That is, after the de-assertion of the `rxdigitalreset` signal, the byte ordering can deviate from the previously explained two permutations.

If the transceiver is clocked by any of the methods other than the default method described above, there is a possibility of byte misalignment. Figure 4 provides an example of byte misalignment.

Figure 4. Byte Misalignment at the Receiver Interface

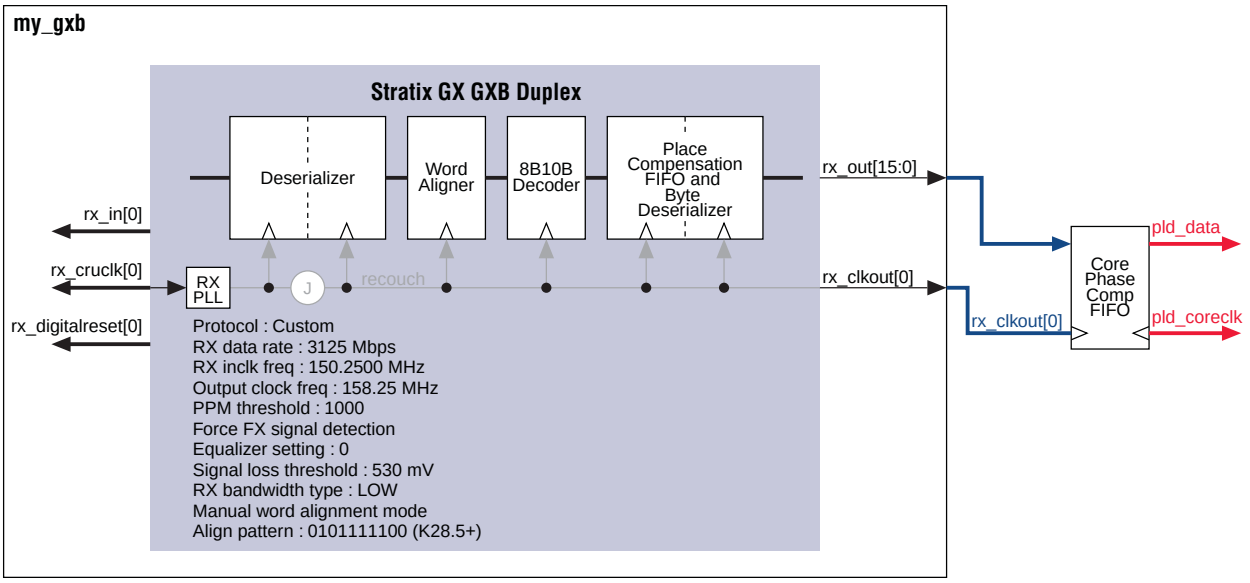


Workaround

The recommended workaround is to run the gigabit transceiver block in the default clocking scheme, as described above, and implement a phase compensation FIFO in the FPGA logic array. This configuration of the gigabit transceiver block will prevent byte misalignment. This would utilize additional resources and increase latency in the datapath. A phase compensation FIFO can be implemented in the FPGA logic array

using a Dual Port RAM, however you decide on the FIFO parameters to meet system specifications. Another thing to be aware of is the additional clock resources needed for this implementation. Each channel will require the use of a global, regional, or fast regional routing resource for the recovered clock (rx_clkout) to be routed out of the gigabit transceiver block. Figure 5 shows an example of this workaround.

Figure 5. Block Level Example of Byte Re-Alignment Logic



Another workaround that can be used in the basic and SONET modes is to run the gigabit transceiver block to PLD interface in single width. This configuration allows the use of rx_coreclk to the receive phase compensation FIFO.

Minimum Serial Data Rate

The specification of the serial data rate minimum is changed from 400 to 500 Mbps. This change improves manufacturing margin.

Transmitter and receiver maximum serial data rates remain unchanged. The serial data rate operating range by speed grade will change as shown in Table 1.

Table 1. Serial Data Rate Operating Range

Device Speed Grade	8B10B Encoding		Non 8B10B Encoding	
	Minimum	Maximum	Minimum	Maximum
-7	500 Mbps	2.5 Gbps	614 Mbps	2.5 Gbps
-6	500 Mbps	3.1875 Gbps	614 Mbps	3.1875 Gbps
-5	500 Mbps	3.1875 Gbps	614 Mbps	3.1875 Gbps

I/O Noise Coupling

Certain aggressor pins in banks 4 and 7 can cause the transmit jitter to increase. Switching of these pins was inducing noise into the RREFB pin. The bias current flowing through the RREFB pin is used as the reference for a lot of transceiver circuits including the transmit PLL circuit. The noise induced in the pin was affecting the bias current and causing the transmit PLL output to jitter. This was resulting in increased transmit jitter.

All Stratix GX devices were tested to identify the respective aggressor pins. Table 2 lists the aggressor pins for each Stratix GX device. It also has the information on the affected transceiver banks and any secondary function of the I/O pin.

Table 2. List of Aggressor Pins & Affected Transceiver Banks (Part 1 of 2)

Device	I/O Banks	Aggressor Pins	Affected Transceiver Banks	Secondary Function of I/O Pin
1,020-pin EP1SGX25	Bank 4	K7	Bank 13, Bank 14	—
		L8		—
	Bank 7	W10	Bank 16	—
672-pin EP1SGX25	Bank 7	V7	Bank 15	—
		AE4	Bank 14	DQS0B
	Bank 4	J7	Bank 14	DEV_OE
		K8		DATA2
672-pin EP1SGX10	Bank 7	V7	Bank 15	—
		AE4	Bank 14	DQS0B
	Bank 4	J7		DEV_OE
		K8		DATA2

Table 2. List of Aggressor Pins & Affected Transceiver Banks (Part 2 of 2)

Device	I/O Banks	Aggressor Pins	Affected Transceiver Banks	Secondary Function of I/O Pin
1,020-pin EP1SGX40	Bank 4	H7	Bank 13	—
		H8		DQ0T6
		J8		DQ0T1
		M10	Bank 14	—
		L8		—
		L9		DQ0T7
		N10		—
		P10		—
		R10		—
	Bank 7	AD8	Bank 16	DQ0B2
		AD7		DQ0B4
		AC8		—
		W10	Bank 15	—
		W11		—
		V10 *(1)*		—

Note to Table 2:

(1) This pin is disabled in the Quartus II software version 5.1.

The Quartus II software version 4.2 and later disables pins from the table depending on the transceiver bank that is being used. Only the pins that can affect the selected transceiver bank will be disabled. The pins will be set to Outputs Driving Ground by the Quartus II software.

Transceiver Modes

The modes supported by the transceiver were revisited following the phase compensation FIFO finding. The transceiver will continue to support the Basic, GIGE, SONET, and XAUI modes of operation. There have been some changes made to the clocking schemes that can be configured within these modes. The changes are made to the clocking schemes available for clocking the transmit and receive phase compensation FIFO buffers.

Table 3 through Table 5 list the functional modes along with the clocking schemes that will be supported by the Quartus II software version 4.2.

Table 3. Functional Modes

Mode	Block	PLD Interface
Basic	Transmitter	Single/Double
	Receiver	Single/Double
GIGE	Transmitter	Single
	Receiver	Single
XAUI	Transmitter	Double
	Receiver	Double

Table 3. Functional Modes

Mode	Block	PLD Interface
SONET	Transmitter	Single/Double
	Receiver	Single/Double

In addition to this, Table 4 lists the clocking schemes for the receiver phase compensation FIFO supported by Stratix GX devices.

Table 4. Receive Phase Compensation FIFO Clocking

Mode	PLD Interface	Phase Compensation FIFO Clocking	
		Write	Read
Basic	Single	rx_clkout	rx_coreclk
	Single/double	rx_clkout	rx_clkout
GIGE	Single	refclk	coreclk (from same quadrant) *(1)*
XAUI	Double	refclk	coreclk (from same quadrant) *(1)*
SONET	Single	rx_clkout	rx_coreclk
	Single/double	rx_clkout	rx_clkout

Note to Table 4:

(1) This signal comes out on the coreclk_out port in the MegaWizard® Plug-In Manager.

Table 5 lists the supported clocking schemes for the transmitter phase compensation FIFO.

Table 5. Transmit Phase Compensation FIFO Clocking

Mode	PLD Interface	Phase Compensation FIFO Clocking	
		Write	Read
Basic	Single/double	tx_coreclk	refclk
	Single/double	coreclk *(1)*	refclk
GIGE	Single	coreclk *(1)*	refclk
	Single	tx_coreclk	refclk
XAUI	Double	coreclk *(1)*	refclk
	Double	tx_coreclk	refclk
SONET	Single/double	tx_coreclk	refclk
	Single/double	coreclk *(1)*	refclk

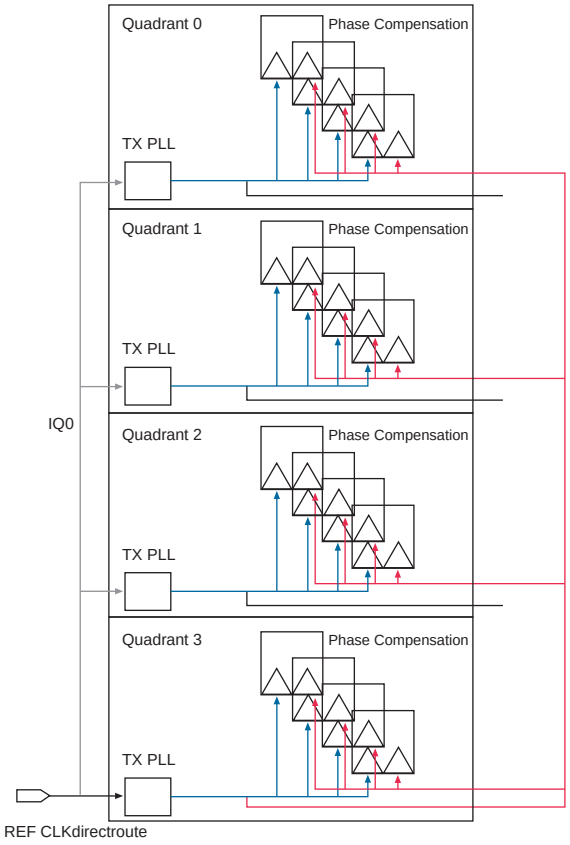
Note to Table 5:

(1) This signal comes out on the coreclk_out port in the MegaWizard Plug-In Manager.

Multi-Quadrant Configurations

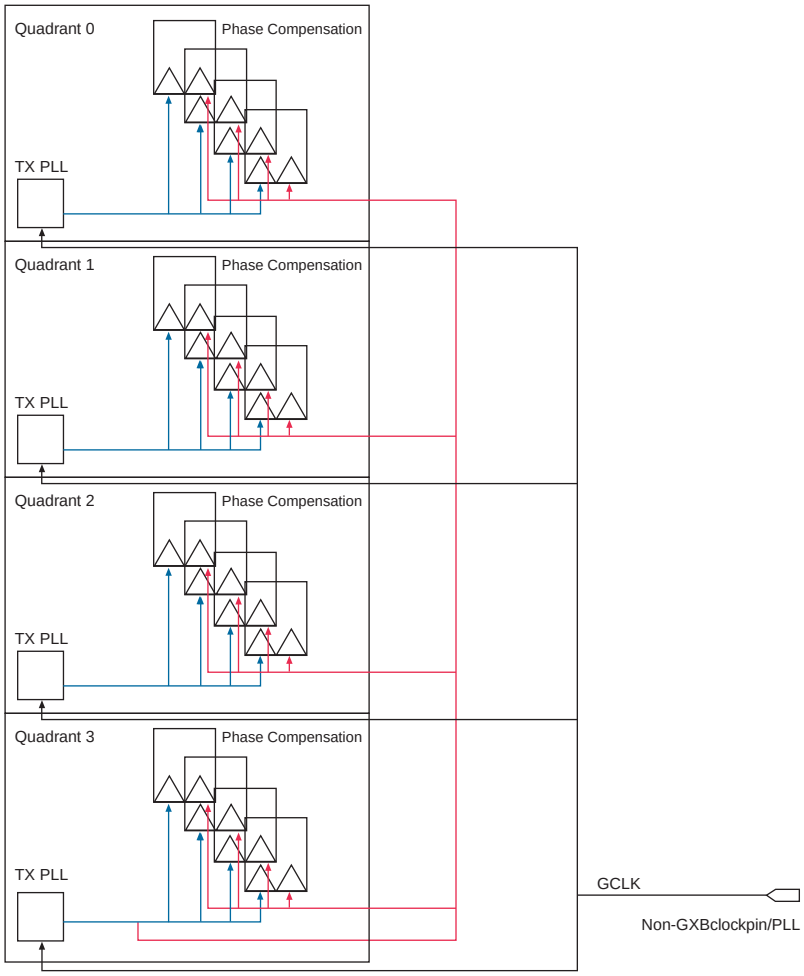
Figure 6 and Figure 7 show the clocking schemes allowed for transmit phase compensation.

Figure 6. Transmit Phase Compensation FIFO Clocking Across Quadrants over IQ Lines



FIFOs that share a transmitter PLL `refclk` output from one transceiver block across transceiver blocks. Figure 6 shows IQ routing used for the `refclk` output across quads. Figure 7 shows global clock routing being utilized.

Figure 7. Transmit Phase Compensation FIFO Clocking Across Quadrants using Global Lines



Loopback Modes

The gigabit transceiver block supports the following loopback modes:

- Serial loopback (serial loopback from the transmitter serializer output to the receiver deserializer input)
- Reverse serial loopback (loopback from the receiver CRU to the transmitter output pin)
- Parallel loopback (loopback from before the transmitter serializer to the receiver word aligner in single-width)

These modes are described in more detail in the *Stratix GX Transceiver User Guide*.

Signal Detect

The signal detect circuit is intended to detect if the signal at the receive pins of the Stratix GX transceiver exceeds a certain voltage threshold. If the V_{ID} (differential input voltage) exceeds this detect threshold, then the signal detect port from the gigabit transceiver block into the FPGA logic array is asserted. If the V_{ID} is below the signal loss threshold, then the signal detect port into the FPGA logic array is de-asserted.

Altera has learned that the signal detect circuit does not function according to the data sheet specifications. The signal detect may trigger at V_{ID} values above and below the specified value, resulting in unpredictable behavior. Hence, Signal Detect is removed and no longer available as a feature in all Stratix GX devices, and support for this feature will be removed from Quartus II software.

Quartus II Software Change, Version 4.2 SP1

The Quartus II software version 4.2 SP1 will not provide the option of variable Signal Detect Settings (Detect and Loss Thresholds). The default will be "Force Signal Detection."

Altera will provide a Quartus Settings File (**.qsf**) variable to enable the use of this feature for existing designs.

PLL Reconfiguration

Certain instances of PLL reconfiguration cause the `scandataout` signal to become stuck in the high position. The following cases explain when this incorrect device operation will occur. These sections also provide work arounds for the issue.

Reconfiguring Post-Scale Counters

When reconfiguring just the post-scale (G, L, and E) counters, after all the `scandata` bits are loaded into the scan chain, any changes to the post-scale counters (time delay or count value) are updated automatically and correctly. However, the `scandataout` signal will remain high. To work around this problem, after the `scandataout` signal goes high, you must reset the PLL for at least 500 ns using the PLL's `areset` signal to ensure that the `scandataout` signal goes back low.

If the `scandataout` signal is not being used as a control signal in your design, and if you are reconfiguring just the post-scale counters, then no changes are required in your design.

Reconfiguring N or M Counters

When reconfiguring the N or M counters, after all the `scandata` bits are loaded into the scan chain, any changes to the time delay or count value of N or M counters will not be updated, and the `scandataout` signal will remain high. To work around this problem, after the `scandataout` signal goes high, you must reset the PLL for at least 500 ns using the PLL's `areset` signal to ensure that `scandataout` signal goes back low and new (N,M) counter and delay settings are updated successfully.

rx_freqlocked Deassertion in Automatic Lock Mode

This section describes the correct operation of rx_freqlocked signals.

rx_freqlocked Signal

In the automatic lock mode of operation for Stratix GX transceivers, the rx_freqlocked signal asserts indicating that the device has switched from "lock to reference" mode to "lock to data" mode. The rx_freqlocked signal asserts when the following conditions are met:

- The CRU PLL output and the CRU reference clock must be within the prescribed parts per million (PPM) frequency detector threshold setting (125, 250, 500 or 1000 PPM) that you selected
- CRU reference clock and CRU PLL output are phase matched (phases are within 0.08UI)

In the automatic lock mode, the CRU exits "lock to data" mode if the CRU PLL output and the CRU reference clock are not within the selected PPM frequency threshold detector setting. The rx_freqlocked signal deasserts under these conditions and the CRU PLL enters "lock to reference" mode.

rx_freqlocked Issue

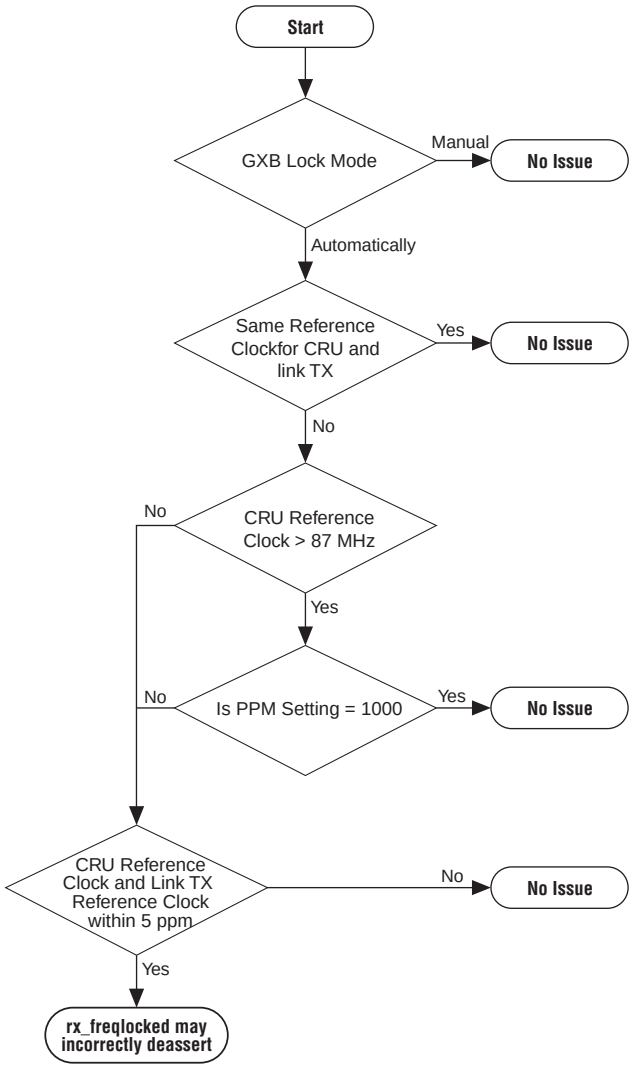
Under certain conditions, the rx_freqlocked signal has an issue in the automatic lock mode. The rx_freqlocked signal might incorrectly deassert even if the CRU PLL and the CRU reference clock are within the selected PPM frequency threshold detector setting.

The rx_freqlocked signal can demonstrate incorrect behavior if:

- The CRU reference clock and the link TX clock are not from the same source AND
- The PPM difference between the CRU reference clock and the recovered clock is less than 5 PPM AND
- Input reference clock is between 25 MHz and 87 MHz

Figure 8 shows a flow chart that helps you determine if your Stratix GX design is affected.

Figure 8. Determine if the Stratix GX Design is Affected



The probability of this situation happening is extremely low because it requires for the CRU reference clock and the reference clock for the link TX to be within 5 PPM of each other.

Of the hundreds of customers who have used Stratix GX devices since production started in November 2003, only 2 have reported experiencing this issue.

Workaround

Altera recommends using the manual lock mode for the transceivers. Design the PPM frequency threshold detector in the PLD fabric. A design example for implementing the PPM frequency threshold detector can be found at:

ftp://ftp.altera.com/outgoing/hsio_apps_patches/stratixgx_patches/StratixGX_Manual_Lock_Reference_Design.zip

The PPM detector in Stratix II GX devices work as intended and are not subject to this issue.

Stratix GX Receiver Unlock Issue

The receiver CDR in Stratix GX devices may lock up when the input serial link to it is tri-stated or hot-socketed. Lock-up condition can be identified when both `rx_locked` and `rx_freqlocked` signals are de-asserted for greater than 50 µs in lock-to-reference mode. When the CDR locks up, it can neither lock to the incoming data in lock-to-data mode, nor the reference clock in lock-to-reference mode. This failure is highly intermittent in nature. Your design is affected only if the receiver CDR is not reset in case of a tri-state or a hot-socket condition (`rx_analogreset` not asserted) at the receiver input port.

Affected Devices

The following Stratix GX devices are affected:

- EP1SGX40
- EP1SGX25
- EP1SGX10

Workaround

Altera recommends you use the CDR reset soft IP. The soft IP continuously monitors the receiver CDR lock status. If the soft IP detects the deassertion of the `rx_locked` and `rx_freqlocked` signals for more than 50 µs, it toggles the `rx_analogreset` (power down signal to the receiver) to re-initialize the receiver. This workaround involves an RTL change and requires recompilation and re-validation of your design.

The CDR reset soft IP module includes the CDR reset soft IP in Verilog HDL format and a **Readme.txt** file with details about using the workaround module. You can downloaded the module at:

http://www.altera.com/support/kdb/downloads/rd09092009_534/watchdog_module.zip

Revision History

The information contained in the version 1.8 of this document supersedes information published in previous versions.

Version 1.8

Updated link in "Workaround" of "Stratix GX Receiver Unlock Issue".

Version 1.7

Added "Stratix GX Receiver Unlock Issue" on page 13.

Version 1.6

Added “rx_freqlocked Deassertion in Automatic Lock Mode” on page 12.

Version 1.5

The introduction has been updated in version 1.5 of the Stratix GX FPGA Errata Sheet.

Version 1.4

The following change has been made to version 1.4 of the Stratix GX FPGA Errata Sheet: updated Table 2 on page 5.

Version 1.3

The following change has been made to version 1.3 of the Stratix GX FPGA Errata Sheet: added the “PLL Reconfiguration” section.