POS-PHY Level 4 MegaCore Function

November 2004, MegaCore Version 2.2.2 Errata Sheet

Introduction

This document addresses known errata and documentation changes for version v2.2.2 of the POS-PHY Level 4 MegaCore® function.

Errata are design functional defects or errors. Errata may cause the POS-PHY Level 4 MegaCore function to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated into a future release of the POS-PHY Level 4 MegaCore function.

POS-PHY Level 4 MegaCore Function v2.2.2 Issues

Altera has identified the following issues that affect the POS-PHY Level 4 MegaCore function v2.2.2:

1. "The atxdav Signal May Be Deasserted One Clock Cycle Early".
2. "The Status Is Set to Satisfied When the ctl_a0_extstat_val Signal Is Deasserted".
3. "The Intermediate FIFO Buffer Overflows When the Atlantic Port 0 Clock Is Slower Than the Receive Reference Clock".
4. "Under Certain Conditions, the Receiver MegaCore Function Detects Errors, but Fails to Report the Source/Cause".
5. "The err_rr_eightn Signal Is not Asserted, as Expected, When Bursts Are Terminated With Reserved Control Words".
6. "Quartus II Warning Message: "Megafunction altlvds_tx Is Expecting Device Logic Family Stratix.""
7. "Quartus II Warning Message: "Device Family Cyclone Does not Have M512 Blocks.""
8. "When a Parameter Is Changed, IP Toolbench Sets Subsequent Parameters to Their Default Values".

9. "The run_modelsim_verilog & run_modelsim_vhdl Scripts Are not Executable".

10. "IP Toolbench Prevents Dynamic Phase Alignment (DPA) at Less Than 415 Mbps".

The atxdav Signal May Be Deasserted One Clock Cycle Early

The `atxdav` signal is deasserted when the unused space in the buffer is less than, or equal to, the FIFO threshold high (FTH) value. It should only be deasserted when the remaining space is less than FTH.

Affected Configurations

All transmitter variations of the MegaCore function are affected.

Design Impact

The `atxdav` may be deasserted one cycle early, leading to overflows in the transmit buffer.

Workaround

When parameterizing your MegaCore function, set the value of FTH to be one level higher than your required value.

Solution Status

This issue is to be fixed in the next release of the POS-PHY Level 4 MegaCore function.

The Status Is Set to Satisfied When the ctl_a0_extstat_val Signal Is Deasserted

When using the user-controlled status source option in the receiver MegaCore function, the `ctl_a0_extstat_val` signal is asserted to write the user-provided status into memory for the user-provided port number. When the `ctl_a0_extstat_val` signal is deasserted, a status of satisfied is incorrectly written into the memory for the user-provided port number, where there should be no status update.

Affected Configurations

All receiver variations of the MegaCore function that use the user-controlled status source option are affected.

Design Impact

The receiver MegaCore function may backpressure the transmitter for ports that should be able to send data.

Workaround

When using the user-controlled status source option, never deassert the `ctl_a0_extstat_val` signal. Instead, always provide valid status updates to the receiver MegaCore function.

Solution Status

This issue is to be fixed in the next release of the POS-PHY Level 4 MegaCore function.

The Intermediate FIFO Buffer Overflows When the Atlantic Port 0 Clock Is Slower Than the Receive Reference Clock

The MegaCore function allows you to operate the Atlantic™ interface at a frequency lower than the MegaCore function's internal frequency. This allows you to read data out of the buffer with a lower bandwidth than the SPI-4.2 link, for applications using a high-bandwidth link for low-bandwidth traffic.

For this variation, the data is read from the intermediate first-in first-out (FIFO) buffer, and is written into the individual buffers using port 0's Atlantic clock. When a high data rate burst occurs in the MegaCore function, the intermediate FIFO buffer may overflow if the port 0 Atlantic clock is not fast enough, and the `err_rr_rxintfifo_oflw` signal may be asserted.

Affected Configurations

All receiver variations of the MegaCore function that use the individual buffers mode, and for which `a0_arxclk` is slower than `rrefclk`, are affected.

Design Impact

Buffer overflows may occur, and data may be lost.

Workaround

Modify the wrapper file (**mycore_aot1169_wrapper_concat.v**) so that the `rrefclk`, not the `a0_rxclk`, drives the read clock from the intermediate FIFO buffer (intfifo), the write clock to each Atlantic FIFO buffer, and the int_arxena_d1 register.

After you have modified the wrapper file and core top-level file, use *Application Note 360: Updating Simulation Models for the POS-PHY Level 4 MegaCore Function* and the applicable script, available from **www.altera.com/products/ip/communications/pos_phy/m-alt-posphy4.html**, to update your simulation models with the changes you have made to the source files.

Solution Status

This issue is to be fixed in the next release of the POS-PHY Level 4 MegaCore function.

Under Certain Conditions, the Receiver MegaCore Function Detects Errors, but Fails to Report the Source/Cause

When the receiver MegaCore function receives an EOP abort, or receives an end-of-packet (EOP) marker for an odd-sized packet, and the high-byte of the SPI-4.2 data bus is non-zero, the MegaCore function detects the error, and correctly marks the data as errored on the Atlantic interface. However, the MegaCore function does not provide any signal to indicate why the data was errored.

Affected Configurations

All receiver variations of the MegaCore function are affected.

Design Impact

It is impossible to differentiate between a reserved control word error that ends a burst prematurely, and an error that does not affect data. Errored data is always marked as errored, regardless.

Workaround

To access the EOP-abort indication, you must modify the wrapper file (**mycore_aot1169_wrapper_concat.v**). Find the instantiation of the **my_rx_core_aot1169_posphy4** module within the wrapper file. The signals `eop_abort_mark` and `eop_bytenz` are asserted when an EOP-abort condition and a non-zero unused byte condition are detected, respectively. Modify the wrapper file to connect these signals to signals

that become outputs from the wrapper file. Modify the top-level core file (**mycore.v**) to ensure that these new wrapper outputs are available to the user logic.

After you have modified the wrapper file and core top-level file, use *Application Note 360: Updating Simulation Models for the POS-PHY Level 4 MegaCore Function* and the applicable script, available from **www.altera.com/products/ip/communications/pos_phy/m-alt-posphy4.html**, to update your simulation models with the changes you have made to the source files.

Solution Status

This issue is to be fixed in the next release of the POS-PHY Level 4 MegaCore function.

The err_rr_eightn Signal Is not Asserted, as Expected, When Bursts Are Terminated With Reserved Control Words

All SPI-4.2 bursts should be multiples of 16 bytes, unless an EOP marker follows a burst. When the receiver MegaCore function receives a burst that is not a multiple of 16 bytes and is followed by an IDLE character, a training control word, or a payload control word, the `err_rr_eightn` signal is asserted and the packet is aborted. This is the expected and correct behavior. However, when the burst is followed by a reserved control word, the `stat_rr_rsv_cw` signal is asserted, but the `err_rr_eightn` signal is not asserted and the packet is not aborted.

Affected Configurations

All receiver variations of the MegaCore function are affected.

Design Impact

Bursts improperly terminated by reserved control words are not detected and aborted.

Workaround

No workaround is available for this issue.

Solution Status

This issue is to be fixed in a future release of the POS-PHY Level 4 MegaCore function.

Quartus II Warning Message: "Megafunction altlvds_tx Is Expecting Device Logic Family Stratix."

When a MegaCore function targeting the Stratix® II family is being compiled, the following Quartus® II warning message is displayed: *"Megafunction altlvds_tx is expecting device logic family Stratix but is being compiled for Stratix II"*.

Affected Configurations

All Stratix II variations of the MegaCore function are affected.

Design Impact

This issue does not impact the MegaCore function. This warning can be safely ignored.

Solution Status

This issue is to be fixed in a future release of the POS-PHY Level 4 MegaCore function.

Quartus II Warning Message: "Device Family Cyclone Does not Have M512 Blocks."

When a MegaCore function targeting the Cyclone™ family is being compiled, the following Quartus II warning message is displayed: *"Assertion warning: Device family Cyclone does not have M512 blocks — using available memory blocks"*.

Affected Configurations

All Cyclone variations of the MegaCore function are affected.

Design Impact

This issue does not impact the MegaCore function. This warning can be safely ignored.

Solution Status

This issue is to be fixed in the next release of the POS-PHY Level 4 MegaCore function.

When a Parameter Is Changed, IP Toolbench Sets Subsequent Parameters to Their Default Values

When a parameter is changed, IP Toolbench may set subsequent parameters to their default values, even if you have already set those parameters.

Affected Configurations

All variations of the MegaCore function are affected.

Design Impact

If you are not aware that by changing a parameter you may cause subsequent parameters to revert to their default values, the MegaCore function variation that is generated may not have your desired parameter set.

Workaround

Set the parameters in the order that they are presented in IP Toolbench; or if you change a parameter, verify any subsequent parameters for changes.

Solution Status

This issue is to be fixed in the next release of the POS-PHY Level 4 MegaCore function.

The run_modelsim_verilog & run_modelsim_vhdl Scripts Are not Executable

The **run_modelsim_verilog** and **run_modelsim_vhdl** scripts included with the MegaCore function, and used to execute the demonstration testbenches, are not executable files.

Affected Configurations

All variations of the MegaCore function that are generated using the Linux or Solaris operating system are affected.

Design Impact

The demonstration testbench cannot be executed until the workaround is implemented.

Workaround

Use the command `chmod 777 <filename>` on each script file to make it executable.

Solution Status

This issue is to be fixed in a future release of the POS-PHY Level 4 MegaCore function.

IP Toolbench Prevents Dynamic Phase Alignment (DPA) at Less Than 415 Mbps

IP Toolbench prevents the DPA parameter to be selected at less than 415 Mbps, even though the Stratix GX and Stratix II device families support DPA for rates as low as 311 Mbps.

Affected Configurations

All receiver variations of the MegaCore function that require DPA are affected.

Design Impact

IP Toolbench prevents DPA-enabled designs with data rates of less than 415 Mbps per LVDS pair.

Workaround

The high-speed serial interface (HSSI) file named **<*MegaCore_name*>_aot1169_hssi_concat.v** or **<*MegaCore_name*>_aot1169_hssi_concat.vhd** contains two constants. The constant MW_INCLOCK_PERIOD_ap162 defines the period of the LVDS block in picoseconds, and the constant MW_INPUT_DATA_RATE_ap162 defines the data rate in Mbps per LVDS pair. Modify these constants to reflect the desired data rates.

Example: for a data rate of 400 Mbps, set the MW_INPUT_DATA_RATE_ap162 constant to `400`, and the MW_INCLOCK_PERIOD_ap162 constant to `5000`.

Solution Status

This issue is to be fixed in the next release of the POS-PHY Level 4 MegaCore function.

Contact Information

For more information, go to Altera's mySupport website at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the revision history.

Table 1. Revision History

Version	Date	Details of Change
1.0	November 2004	First release of the POS-PHY Level 4 MegaCore Function errata sheet for v2.2.2.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com